
Contribution ID: **68** Type: **Oral**

# Redundant SAR ADC architecture and circuit techniques for ATLAS LAr Phase-II upgrade

*Thursday, 1 October 2015 14:50 (25 minutes)*

We present the architecture and circuit techniques of a 14-bit 80-MS/s split-SAR ADC in 65-nm CMOS with preliminary simulation results. By exploiting redundancy, SEE-related conversion errors can be efficiently detected and corrected at the architectural level by the added SEE-detection circuitry. The digital calibration also makes the overall ADC performance insensitive to transistor parameter variations, thus providing inherent TID immunity. The initial transistor-level simulation results revealed a ≥75-dB SNDR and a ≥90-dB SFDR, with a total power consumption of ≤30 mW.

## Summary

The development of SAR ADCs in the past decade makes it a suitable candidate for digitizing calorimeter readout signals of the ATLAS experiment. Our previous work of a two-step redundant SAR ADC with digital calibration proved its benign property for TID tolerance. This paper is focused on the techniques to address the SEE-related conversion errors in a 14-bit 80-MS/s split-SAR ADC prototype to be fabricated in a 65-nm CMOS.

At the system level, if SEE occurs in one of the two split-ADCs, the two digital outcomes will differ from each other (the probability of both being hit simultaneously is extremely low and will not be considered). By observing the output of the SEE detection circuits embedded in both ADCs, the digital outcome from the ADC which is hit by an ionizing particle will be discarded and the outcome from the other will be retained as the final output. For normal conversion cycles, the two outcomes will be averaged, leading to a 3-dB gain in SNR (i.e., no extra power or area cost occurs).

The ADC is partitioned as a (9b + 7b) two-step structure with two-bit inter-stage redundancy. Digital calibration is implemented based on the split-ADC architecture to correct the capacitor mismatch and amplifier gain error.

The proposed SEE detection circuits and/or detection techniques are outlined as follows.

1. Summing nodes. If the switches connected to the summing nodes are hit during the bit cycles, the total charge on the DAC will be altered, leading to potentially a large conversion error. Circuits are designed to detect the substrate current, which flows from the summing node to the substrate when switches are hit.
2. First-stage SAR loop. If the circuits inside the first-stage SAR loop are hit and an out-of-range residue error occurs, the second stage will overflow, which can be detected by observing its output code.
3. Second-stage SAR loop. If the circuits inside the second stage SAR loop are hit, the residual voltage on the summing nodes after all the bit cycles are finished may be larger than one LSB. This can be detected by adding one redundant bit cycle and comparing the last two bits.
4. Data latches. A parity bit is generated for the serial comparator outputs during bit cycles and stored. Any SEE error in the SAR data latches can be detected by checking the parity bit offline.

The transistor-level simulation of the ADC with thermal noise included shows a 76.4-dB SNDR and a 93.3-dB SFDR for each split-ADC. The SNDR and SFDR increase to 79.1 dB and 95.3 dB, respectively, after averaging (for normal conversions). Assuming that 20% of the samples are corrupted by SEE and the corresponding

digital outcomes are taken from one of the split-ADCs without averaging, the SNDR drops by 0.8 dB. The total power consumption is slightly less than 30 mW.

**Primary authors:** XU, Hongda (The University of Texas at Dallas); DU, Ling (The University of Texas at Dallas); CHIU, Yun (UT Dallas)

**Co-authors:** GONG, Datao (Southern Methodist Univeristy); YE, Jingbo (Southern Methodist University, Department of Physics)

**Presenter:** CHIU, Yun (UT Dallas)

**Session Classification:** ASICs

**Track Classification:** ASICs