The Clock and Control System for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade

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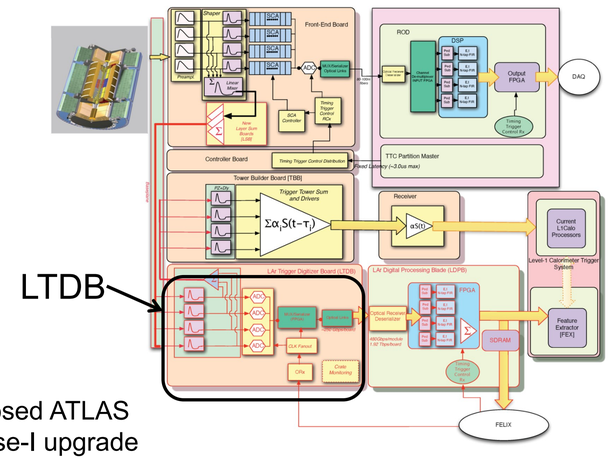
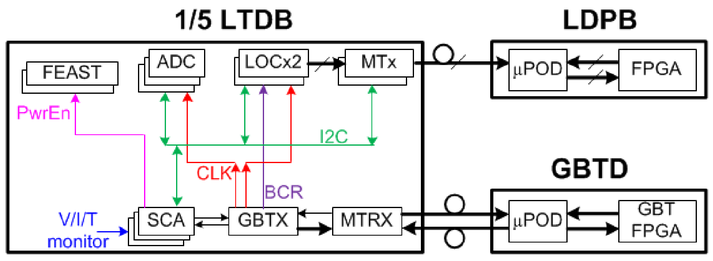
Introduction

- A Liquid Argon Calorimeter (LAr) Trigger Digitizer Board (LTDB) is being developed to upgrade the ATLAS LAr trigger electronics, which will be commissioned in 2017-2018 [1].
- Each LTDB includes 320-channel analog amplifiers, 80 12-bit, 40-MS/s Analog-to-Digital converter (ADCs), 20 serial-data transmitters (LOCx2's), and 20 optical transmitter modules (MTx's).
- The ADC and LOCx2 each need a 40-MHz clock signal that is synchronized to the LHC bunch-crossing clock.
- The ADC, LOCx2, and MTx each need to be configured remotely.
- The operational status of LTDB needs to be monitored.
- It is critical to design a clock and control system for the LTDB.
- In this paper, we present the design and the evaluation of the clock and control system of the LTDB.



The architecture of the proposed ATLAS LAr trigger electronics in Phase-I upgrade

Design Overview

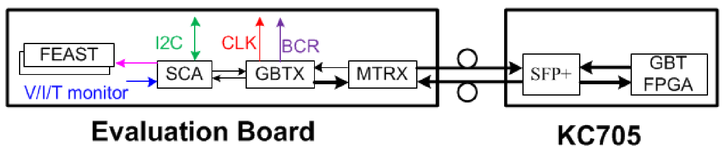


The overall clock and control system

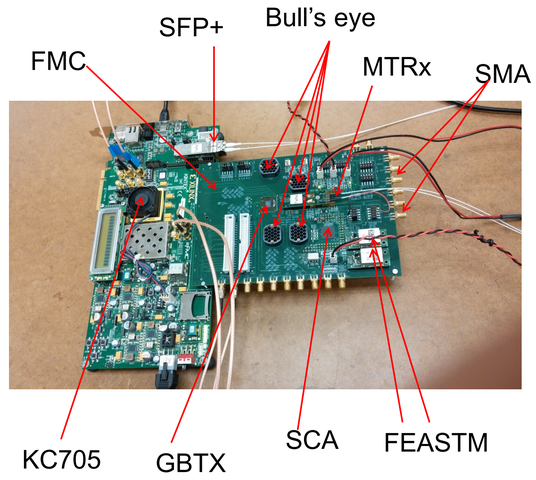
- The clock and control system uses four duplex optical links between each LTDB at the front end and the GBT Driver (GBTD) board at the back end.
- Each duplex link, which serves 1/5-slice LTDB, includes an optical transceiver module MTRx, a transceiver ASIC GBTX [2], and a GBT Slow Control Adapter (SCA) [3] on the LTDB.
- The optical links use commercial multi-channel optical transceivers and Multi-Gigabit-Transceiver-embedded FPGAs on the GBTD.

Evaluation System Design

The block diagram of the evaluation system

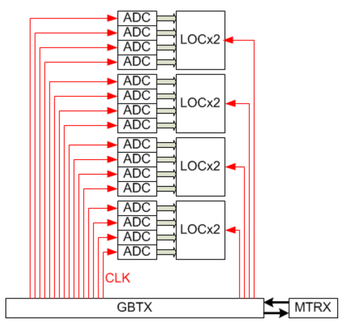


- An evaluation board, including an MTRx, a GBTX, and a GBT SCA, has been developed to evaluate the clock and control system.
- The evaluation board works together with a Xilinx Kintex FPGA board KC705, which emulates the GBTD operating on the back-end.



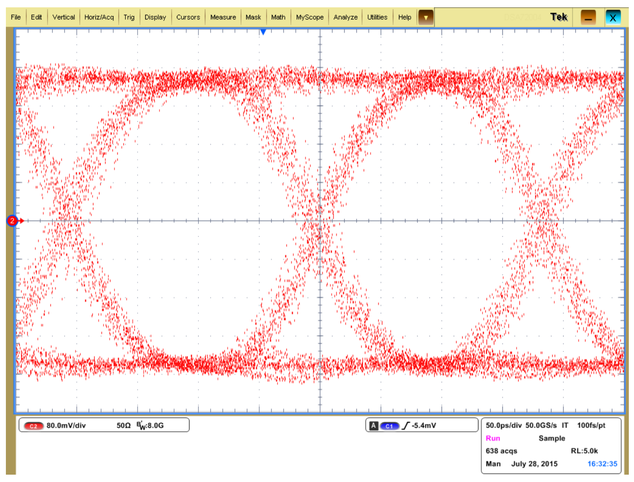
A picture of the evaluation board

Clock distribution: design and evaluation



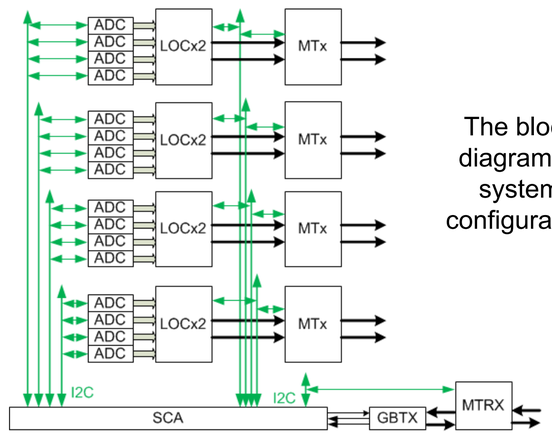
The block diagram of the clock distribution

- Each GBTX has 48 clock outputs which can be used by 20 ADCs and 5 LOCx2's.
- Both the ADC and LOCx2 are sensitive to clock jitter.
- The evaluation to use the GBTX recovered clock for the ADC is still under study.
- The GBTX recovered clock is fed into a LOCx2 and the eye diagram and jitter were measured.
- The clock skew were measured to be less than 580 ps, acceptable from the system view.



Eye diagram of LOCx2 with DCLK17 as the ref clock

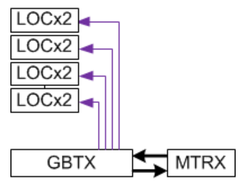
Configuration: design and evaluation



The block diagram of system configuration

- The ADC, LOCx2, MTx (LOCId2), and MTRx (LOCId1) are configured through GBT SCA after each power cycle.
- Each GBT SCA has 16 I²C master modules.
- Four ADCs share an I2C master. One LOCx2 and one MTx shared an I2C master. MTRx (LOCId1) is configured through an extra I2C master.
- The ADC is powered at 1.2 V, whereas GBT SCA is powered at 1.5 V. The I²C interface of the ADC can tolerate 1.5 V.
- The I²C interfaces of LOCx2, MTx and MTRx are powered at 2.5 V. It is guaranteed from the design and confirmed in the test that GBT SCA can interface correctly with LOCx2, MTx and MTRx.
- It has been confirmed that GBT SCA can configured MTRx when the uplink is not ready.

Bunch Crossing Reset: design and evaluation

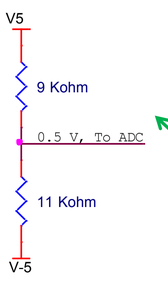


The block diagram of Bunch crossing reset

- Each LOCx2 implements a bunch cross identification (BCID).
- BCID needs to a common reset signal, bunch crossing reset (BCR), for the alignment of all channels.
- BCR repeats every 3564 LHC clock cycles and lasts one clock cycle.
- An e-port data output is used to provide BCR to each LOCx2.
- It is confirmed that GBTX can generate such a BCR signal which meets our requirements.

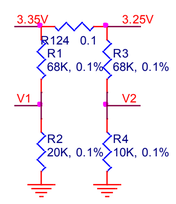
Power Enable and V/I/T Monitor: design and evaluation

Schematic of voltage monitoring



- FEASTMP can be turned off by a general purpose output of GBT SCA and the PowerGood signal of FEASTMP can be monitored by a general purpose input pin of GBT SCA. FEASTMN cannot be controlled or monitored in the same way.
- We use the ADCs inside the GBT SCA to monitor the power voltages. For the voltages higher than 1.0 V or negative, we must use resistors to lower the voltages down into the ADC input range (0 - 1 V). Confirmed in the test.

Schematic of current monitoring



- We monitor the currents by measuring the voltages on the two ends of a sensing resistor. GBT SCA cannot measure differential voltage directly. Confirmed in the test.
- We use thermistors to monitor the temperatures at various location of LTDB. Confirmed in the test.

Conclusion

- A clock and control system, which uses ASICs including GBTX and GBT SCA at the front end, commercial components at the back end, and optical links between the front end and the back end, is being developed.
- A prototype of the clock and control system has been evaluated.

Acknowledgments

This work is supported by US-ATLAS R&D program for the upgrade of the LHC, the US Department of Energy Grant DE-FG02-04ER1299. The authors would like to express the deepest appreciation to Drs. Paulo Moreira, Pedro Leitao, Kostas Kloukinas, Alessandro Caratelli, Francois Vasey, Jan Troska for kindly help.

References

[1] ATLAS Collaboration, *ATLAS liquid argon calorimeter Phase-I upgrade technical design report*, CERN-LHCC-2013-017 and ATLAS-TDR-022, September 20, 2013.
[2] P. Leitao *et al.*, Test bench development for the radiation Hard GBTX ASIC, 2015 *JINST* 10 C01038.
[3] A. Caratelli *et al.*, The GBT-SCA, a Radiation Tolerant ASIC for Detector Control and Monitoring Applications in HEP Experiments, 2015 *JINST* 10 C03034.

TWEPP 2015 - Topical Workshop on Electronics for Particle Physics,
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