AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Development of a low power PLL and DLL in 130nm CMOS technology

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Agenda

- Motivation
- Specifications for PLL and DLL in CMOS 130 nm
- PLL Architecture and Design in process A and B
- DLL Architecture and Design in process A and B
- Prototype ASIC Board and Measurement Setup
- PLL measurements results in process A and B
- DLL measurements results in process A and B
- Summary

Motivation

- Main motivation - Silicon ASIC for LHCb Tracking (SALT) at LHC collider
  - Phase -Locked Loop (PLL) for data serialization and transmission
  - Delay-Locked Loop (DLL) for clock phase alignment for ADC sampling
- Additional motivation - both PLL, DLL are designed with additional features allowing their use as general purpose blocks
  - ultra-low power
  - low jitter
  - multiphase outputs

Specifications

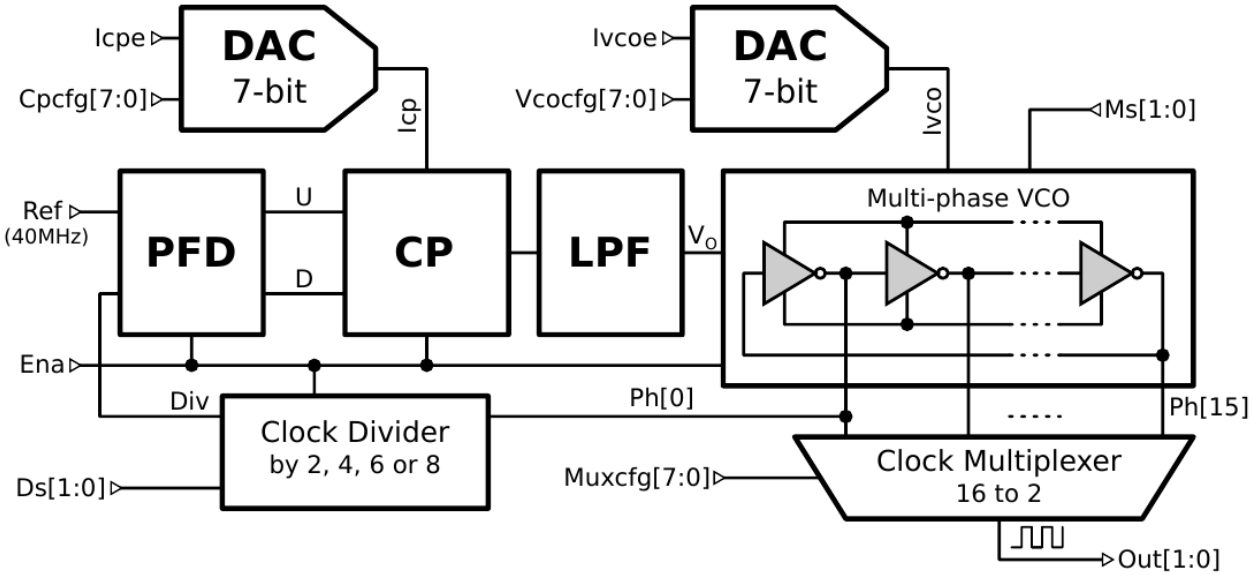
Phase-Locked Loop (PLL)

- Operating frequencies: 80MHz, 160MHz, 240MHz, and 320MHz
- Dividers by: 2, 4, 6, and 8
- Default reference frequency 40 MHz and output 160MHz
- Multi-phase clock output
- Power consumption < 2mW @ 160MHz
- Jitter < 10ps @ 160MHz

Delay-Locked Loop (DLL)

- Operating frequency: 40MHz
- 64 clock phases
- Power consumption < 2mW @ 40MHz
- Jitter < 15 ps @ 40MHz

Phase-Locked Loop Architecture and Design in CMOS 130 nm process A and B



Differences

Process A:

- Single-ended VCO
- External VCO bias

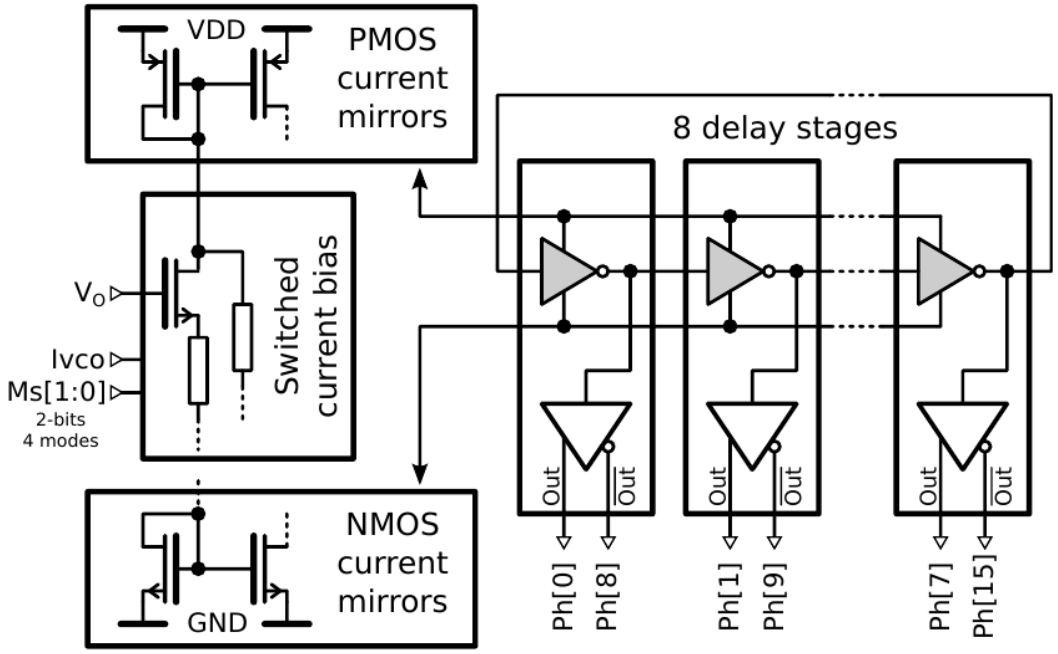
Process B:

- Differential VCO
- External/Internal DAC

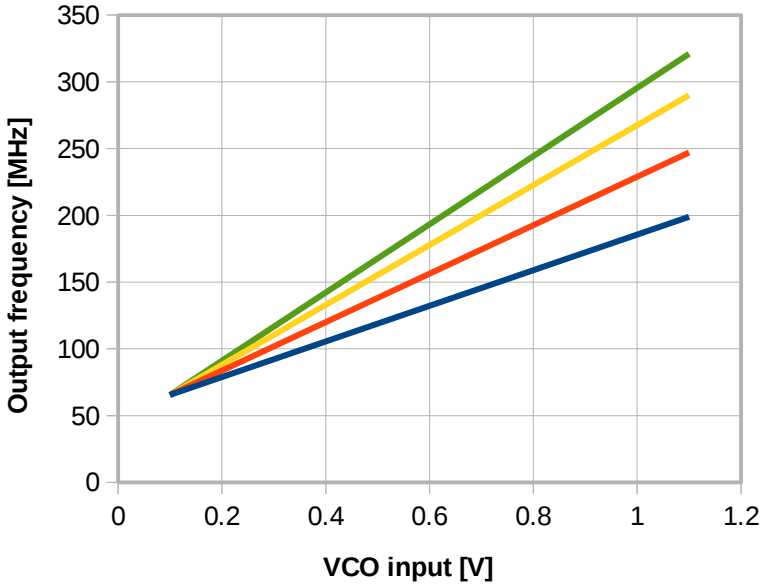
- VCO - core block of PLL - generates 16 output square waves
- PFD compares VCO signal (divided by **N**) to reference signal
- PFD output signals, after processing in CP and filtering, give negative feedback to control VCO frequency
- Output wave (**N** times faster) is synchronized with reference clock

PLL Architecture and Design
Voltage Controlled Oscillator (VCO)

VCO block diagram in process A and B



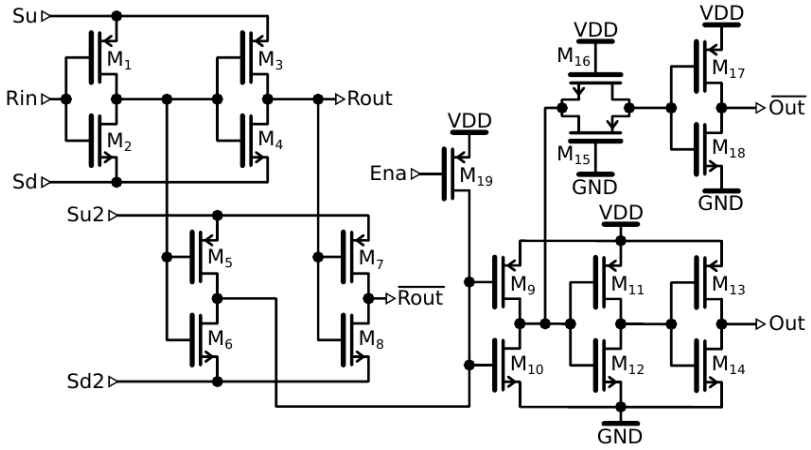
Example simulation



- Common PMOS/NMOS current sources for all delay stages
- Switched current bias – four different VCO gains available

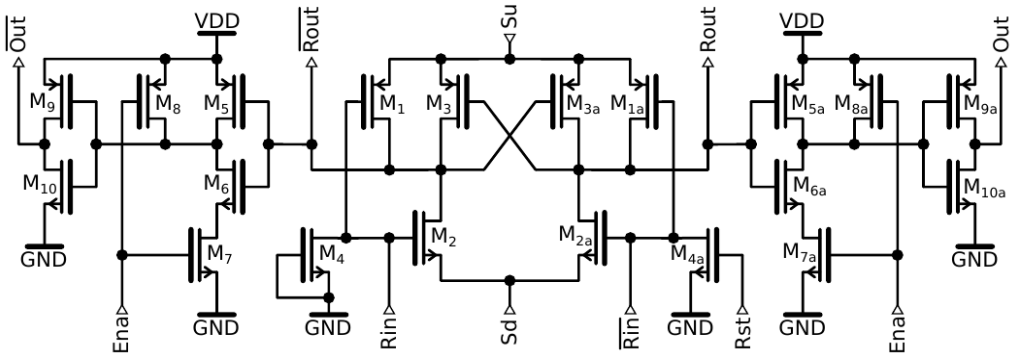
PLL Architecture and Design
VCO delay stages

Process A



- Single-ended delay cell
- Delay of complementary output compensated by transmission gate
- Enable/Disable provided by M_{19}

Process B



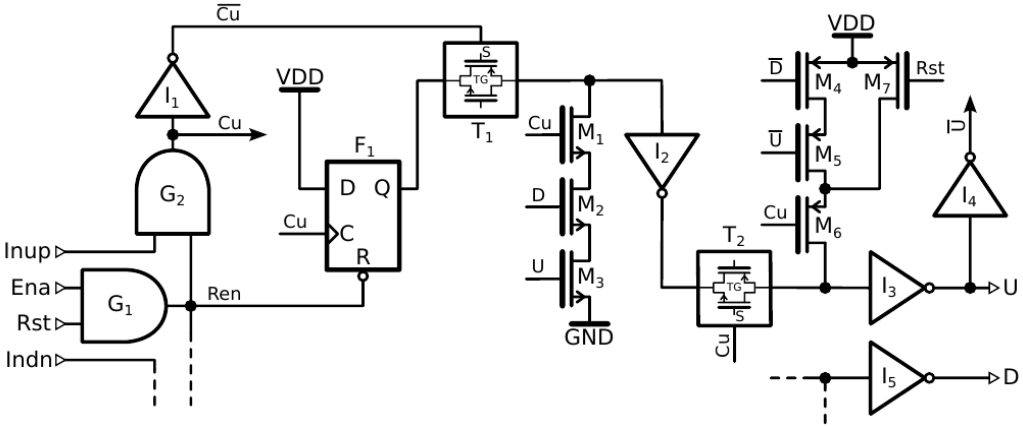
- Differential delay cell
- Complementary output given by differential design
- Enable/Disable provided by $M_{5(a)}$ – $M_{8(a)}$

PLL (DLL) Architecture and Design

PFD and CP

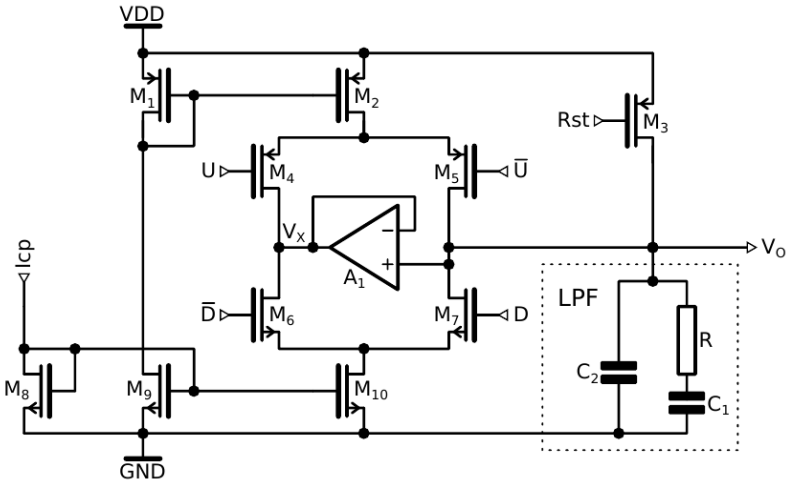
Phase and Frequency Detector (PFD)

(only half of PFD is shown)



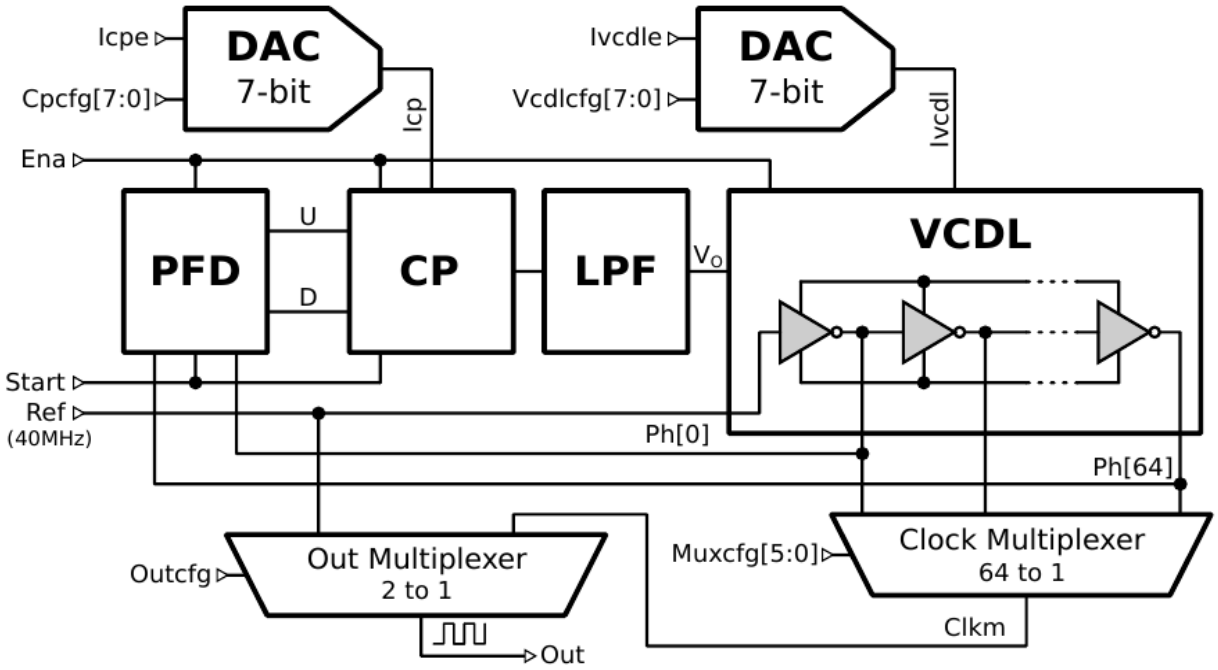
- The same PFD for PLL and DLL in process A and B
- Very simple architecture based on two flip-flops and one NAND gate
- Dynamic flip-flops are used to improve switching speed
- NAND gate integrated inside flip-flop structure

Charge Pump (CP)



- The same CP for PLL and DLL in process A and B
- Typical CP architecture with two current mirrors and four switches
- Additional transistor M_3 to precharge LPF to VDD at the beginning – needed for DLL

Delay-Locked Loop (DLL) Architecture and Design in CMOS 130 nm process A and B



Differences

Process A:

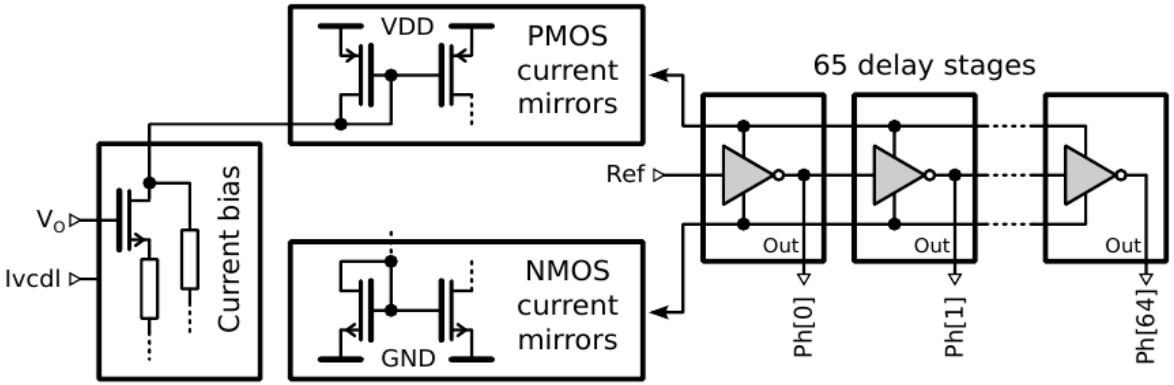
- External bias

Process B:

- External/Internal DAC
- Additional Output Multiplexer

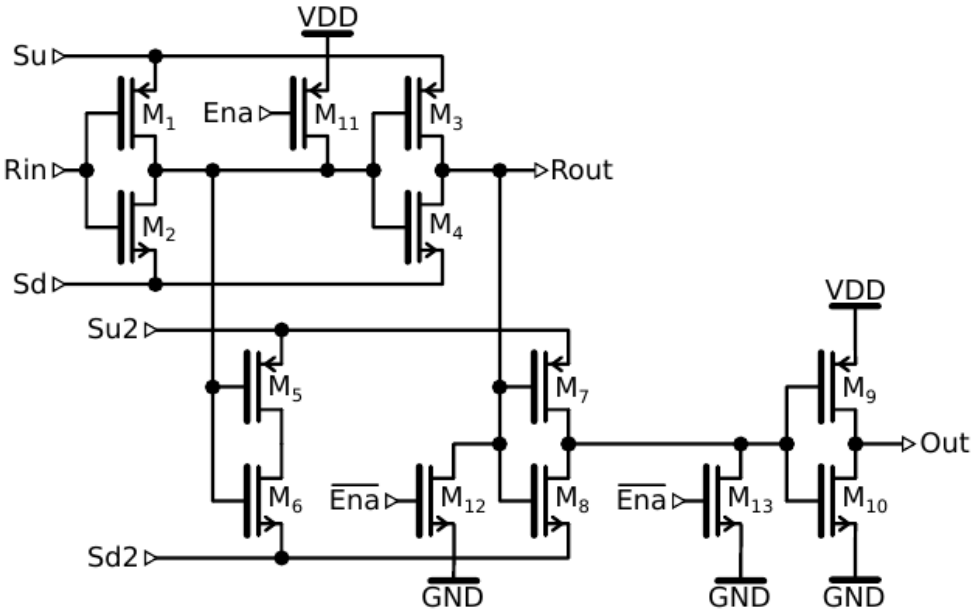
- Single-ended VCDL provides 64 output clock phases
- PFD compares two VCDL output signals (Ph[0] and Ph[64])
- PFD output signals, after processing in CP and filtering, give negative feedback to control VCDL delay
- Output clock phase selected by multiplexer

DLL Architecture and Design
Voltage Controlled Delay Line (VCDL)



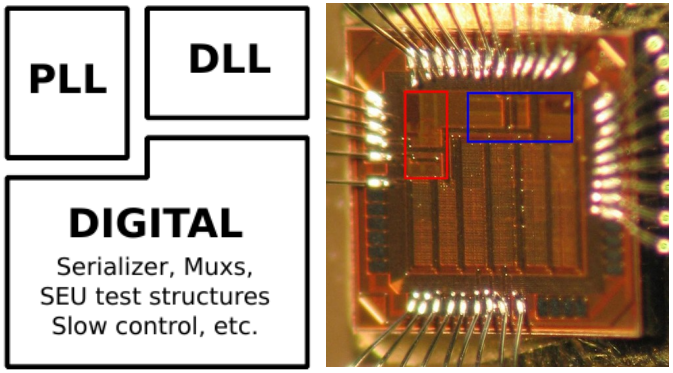
- The same VCDL in process A and B
- 65 delay stages
  - 64 outputs
  - extra output for PFD

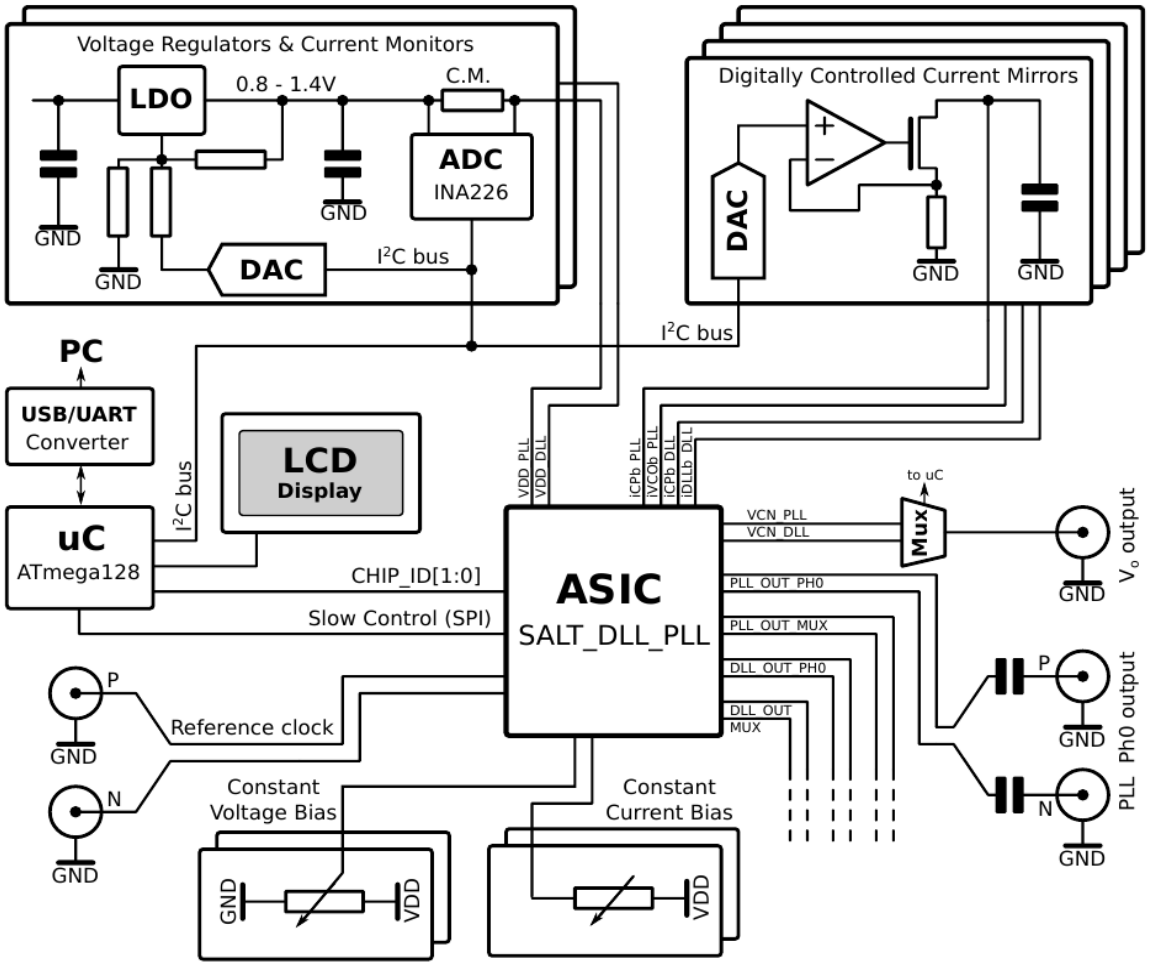
- Single-ended delay cell
- Additional pair of current-starved inverters works as signal buffer – improves PSRR
- Enable/Disable provided by M_{11} – M_{13}



Prototype ASIC board and Measurement Setup

ASIC Floorplan and prototype PCB





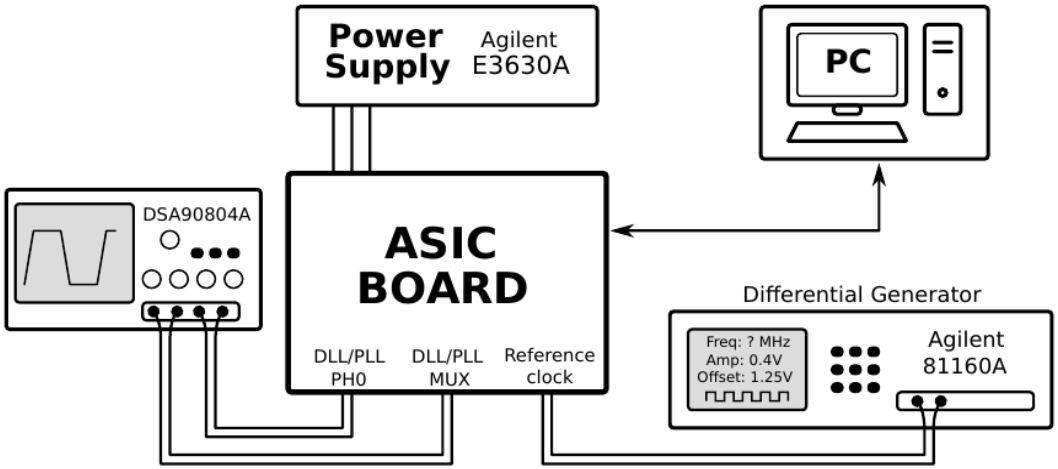
Main features:

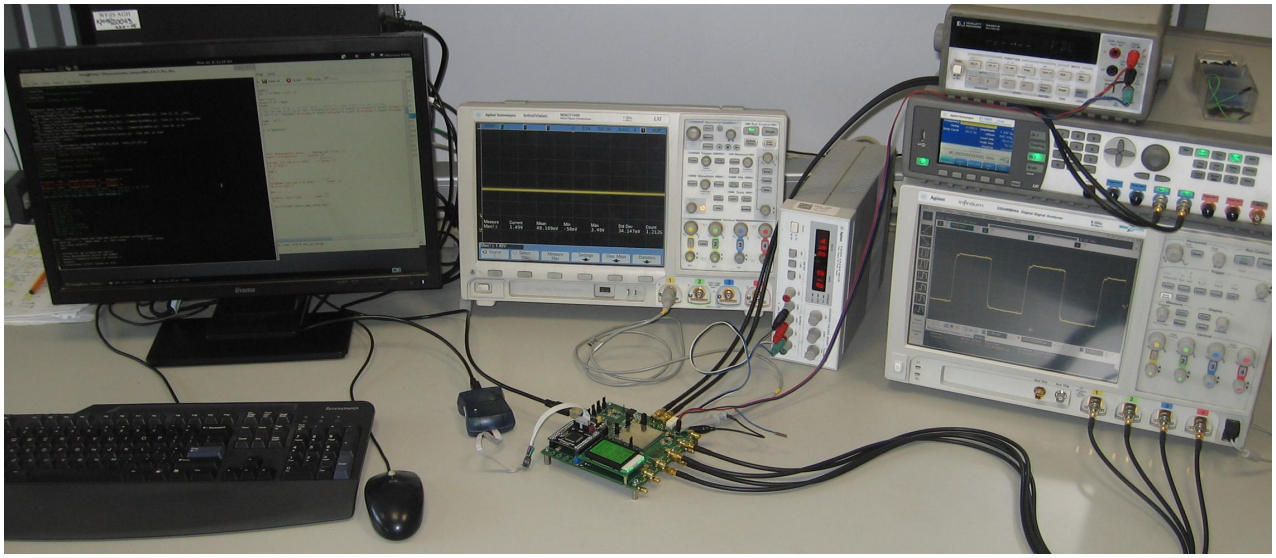
- Digitally controlled Voltage Regulators
- Current/Voltage monitoring
- Digitally controlled current mirrors
- Board controlled by uC
- Communication with PC via USB/UART

Prototype ASIC board and Measurements Setup
Laboratory equipment

Instrumentation:

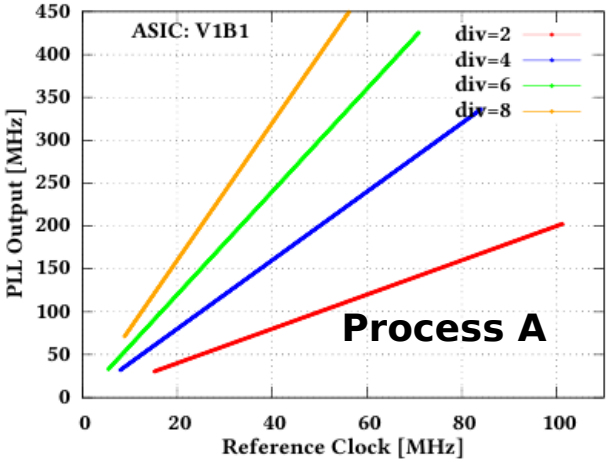
- Power supply (E3630A)
- Differential Generator (81160A)
- 40GS/s scope (DSA90804A)
- PC computer

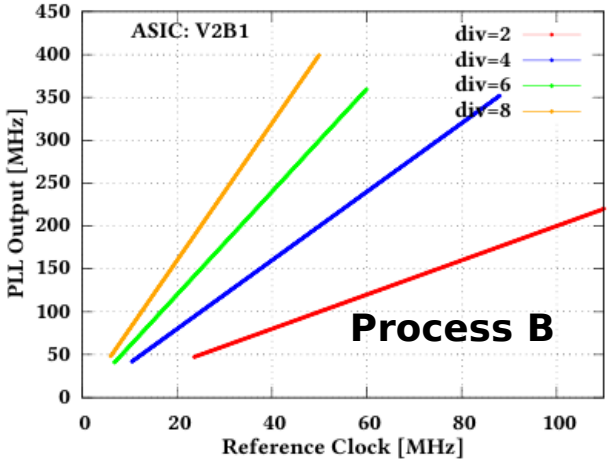




Laboratory equipment and ASIC board are controlled by dedicated software

PLL Measurements results in process A and B
Transfer function and Power consumption





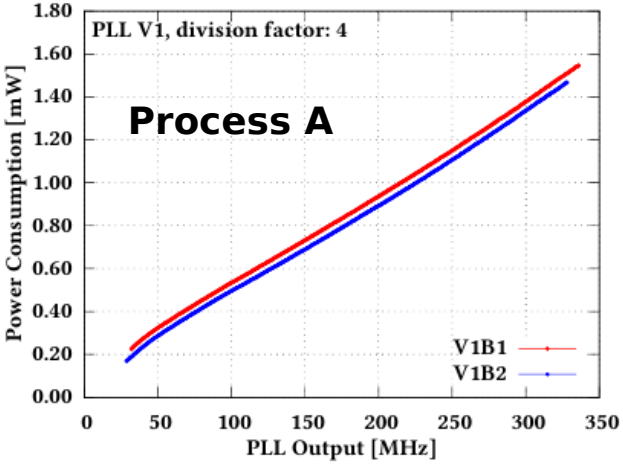
Transfer function

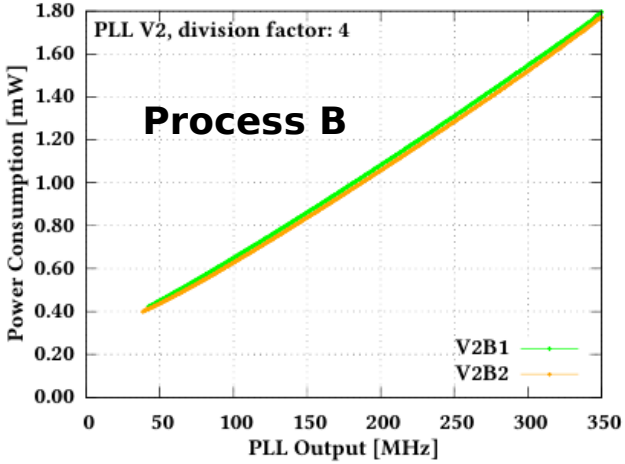
Process A:

30 – 450 MHz
Dividers: 2, 4, 6, and 8

Process B:

40 – 400 MHz
Dividers: 2, 4, 6, and 8





Power consumption

Process A:

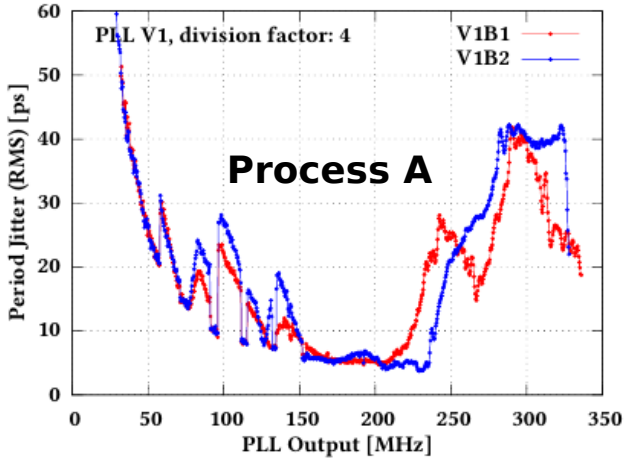
0.8mW @ 160MHz

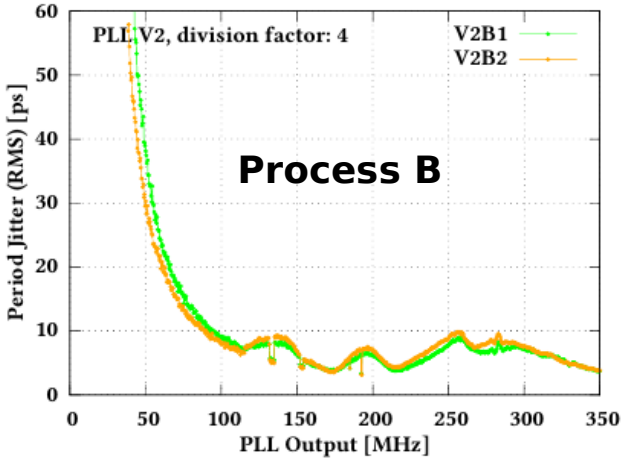
Process B:

0.95mW @ 160MHz

Both PLLs consume very low power and work well in wide frequency range

PLL Measurements results in process A and B
Period Jitter





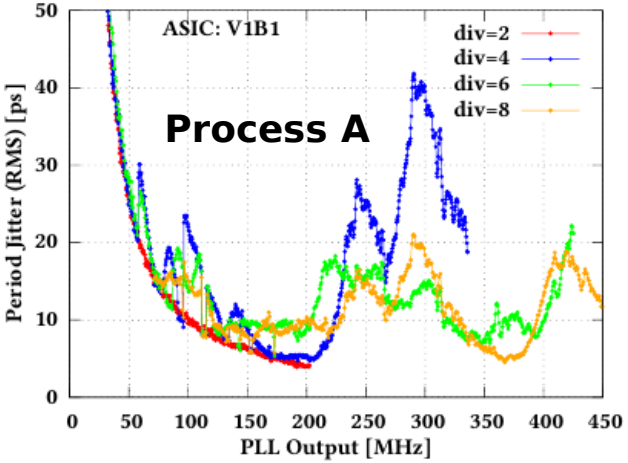
Period Jitter RMS

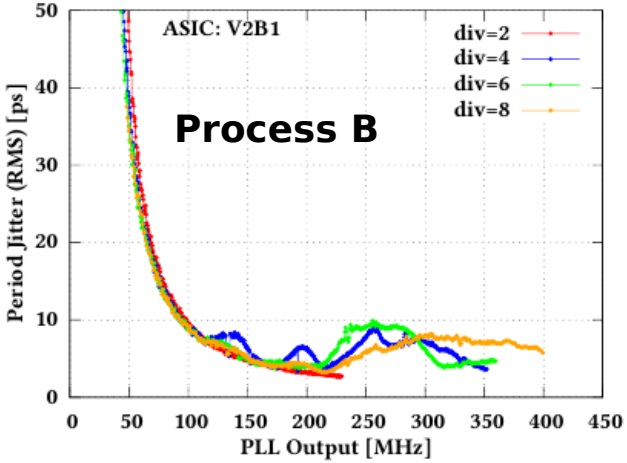
Process A:

<10ps @ 150 – 220MHz

Process B:

<10ps @ 100 – 350MHz





Jitter vs Divider

Process A:

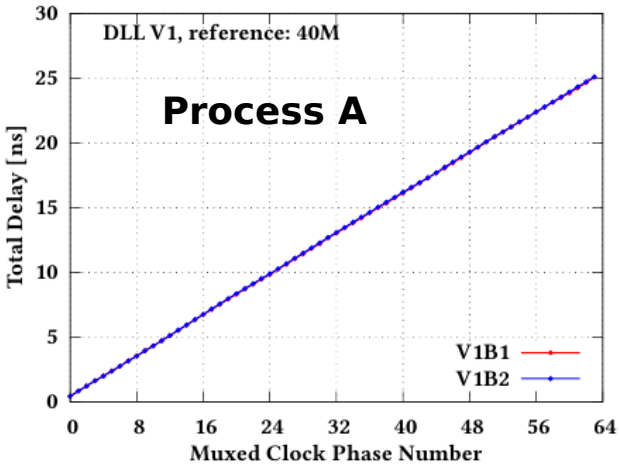
Jitter fluctuates and depends on selected PLL divider

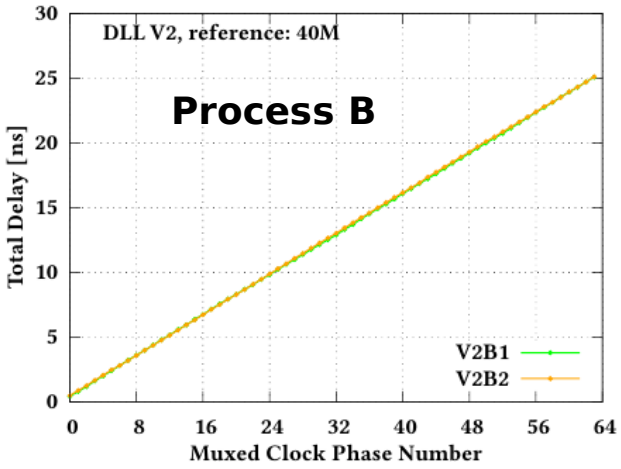
Process B:

Jitter smaller, stable, and weakly depends on divider

Low jitter in wide frequency range – for process B lower and more stable

DLL Measurements Results in process A and B
Transfer function and Power consumption





Transfer function

Process A:

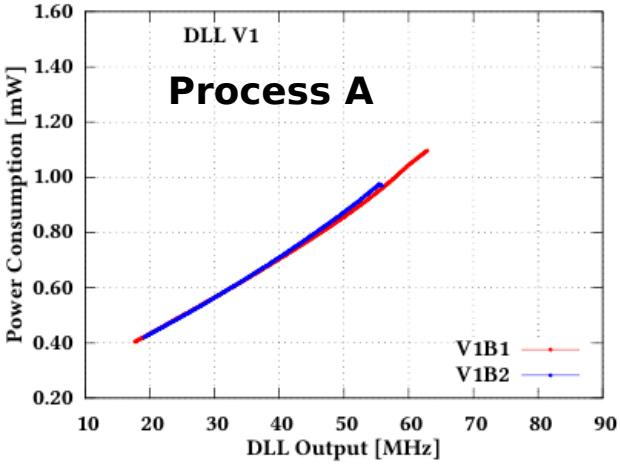
Frequency range: 18 - 62 MHz

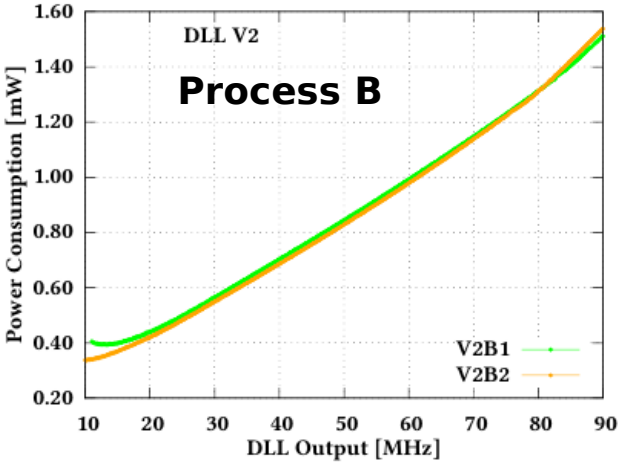
64 phases, delay: 355 – 445 ps

Process B:

Frequency range: 10 - 90 MHz

64 phases, delay: 350 – 448 ps



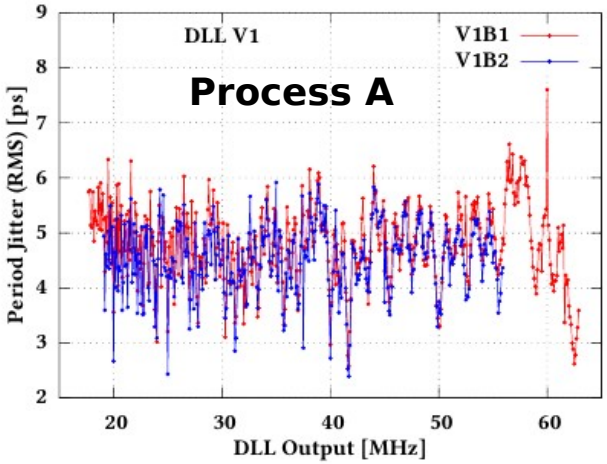


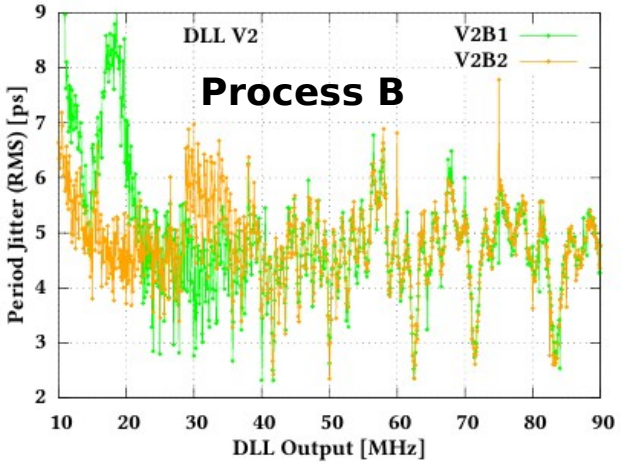
Power Consumption

- Similar for process A and B
- Scales linearly with frequency

Very good linearity and very small power consumption

DLL Measurements Results in process A and B
Period Jitter





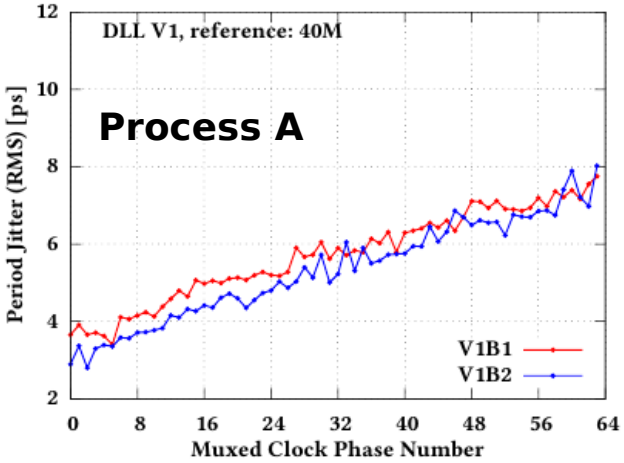
Jitter at phase 0

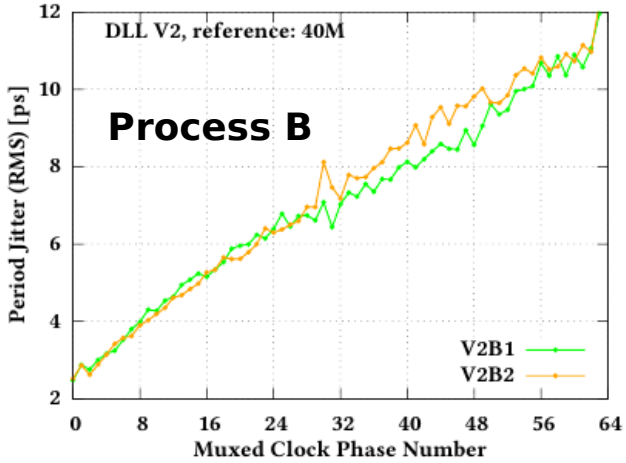
Process A:

<7 ps @ 18 – 62 MHz

Process B:

<7 ps @ 18 – 90 MHz





Jitter vs phase

Process A:

Period jitter: 3.8 – 7.8 ps

Process B:

Period jitter: 2.5 – 12.1 ps

Very low jitter, grows with selected clock phase

Summary

	Parameter	Process A	Process B
PLL	Frequency	30 – 450 MHz	40 – 400 MHz
	Dividers	2, 4, 6, and 8	2, 4, 6, and 8
	Power consumption	0.8 mW @ 160 MHz	0.95mW @ 160MHz
	Jitter (RMS)	<10 ps @ 150 – 220 MHz	<10ps @ 100 – 350MHz
	Clock phases	16	16 (fully uniform)
	Area	450 × 260 um^2	300 × 210 um^2
DLL	Phase delay	355 – 445 ps	350 – 448 ps
	Clock phases	64	64
	Power consumption	0.7 mW @ 40 MHz	0.7 mW @ 40 MHz
	Jitter vs phase	3.8 – 7.8 ps @ 40 MHz	2.5 – 12.1 ps @ 40 MHz
	Jitter Ph0 (RMS)	<7 ps @ 18 – 62 MHz	<7 ps @ 18 – 90 MHz
	Area	680 x 210 um^2	430 x 190 um^2

Ultra-low power, small area, PLL and DLL for SALT and other (general purpose) applications designed, fabricated, and successfully tested

AGH

Thank You for your attention