Contribution ID: **186** Type: **Oral**

A Novel Approach for Pulse Width Measurements in an FPGA

Tuesday 29 September 2015 10:15 (25 minutes)

High precision time measurements are a crucial element in particle identification experiments, which likewise require pulse width information for charge and Time-over-Threshold (ToT) measurements. In almost all of the FPGA-based TDC applications, pulse width measurements are implemented using two of the TDC channels for leading and trailing edge time measurements individually. This method however, requires double the number of resources and therefore this paper presents a novel way of measuring pulse width using a single TDC channel, while still achieving high precision (as low as 12ps RMS).

Summary

High precision time measurements are fundamental to particle identification experiments. While in some experiments charge measurement of a particle is necessary, in the others, Time-over-Threshold (ToT) information may be required for time-walk correction. Both measurements can be done by encoding the charge and ToT information in a digital pulse, through either integrating or discriminating an analogue signal from a detector. Subsequently, the pulse width of the digital signal can be measured by an FPGA-based-TDC, a factor of increasing importance in recent development. In conventional FPGA TDCs the leading and trailing edge time information of a digital pulse are measured in two separate channels by splitting the pulse internally. Although this method is straightforward and relatively simple to implement, it requires double the number of resources. The method outlined in this paper addresses this problem in a unique way by using the internal routing resources of the FPGA.

Measuring the width of a pulse larger than the dead time of a TDC channel (20ns) is possible by simply inverting the input pulse after the successful measurement of the leading edge to measure the trailing edge. However, in experiments the pulses are often differ by a few nanoseconds in width. In order to measure both edges of a pulse shorter than the dead time of a TDC channel, the trailing edge has to be delayed longer than the dead time of the TDC channel. In this approach, the delay is achieved by stretching the pulse asynchronously in the FPGA using the routing interconnections between the logic elements. After the successful measurement of the leading edge time, the delayed trailing edge is directed back to the channel in order to measure the trailing edge time. The type of the measured edge is marked in the data with a single bit.

The calculated time difference between the leading and the trailing edges - pulse width - contains a channel offset caused by the delay circuit, which needs to be calculated and subtracted from the result to find the real pulse width value. The offset is different for each channel as the routing cannot be controlled precisely. However, this offset can be calculated by applying an external pulse to the TDC inputs with a fixed width and subtracting this fixed value from the measured width. As this is not possible in experimental setups, a pulse with a fixed width of 30ns is generated internally and is sent to each channel to measure the offset value. The same generated pulse is also used to calibrate the channels.

Current tests elicit measurement of 9ps (RMS) and 12ps (RMS) on the leading edge and trailing edge respectively. Essentially, this innovative approach has halved the number of resources required by traditional approaches while still maintaining high precision.

Author: UGUR, Cahit (GSI - Helmholtzzentrum fur Schwerionenforschung GmbH (DE))

Co-authors: MICHEL, Jan (Goethe University Frankfurt); TRAXLER, Michael (GSI Helmholtzzentrum für Schwerionenforschung GmbH)

Presenter: UGUR, Cahit (GSI - Helmholtzzentrum fur Schwerionenforschung GmbH (DE))

Session Classification: Programmable Logic, design tools and methods

Track Classification: Logic