A 12b Rad-Hard Digital Calibrated Single Slope ADC for LHC environment

T. Vergine[1,2], M. De Matteis[2,3], A. Caratelli[4,5], A. Marchioro[4], K. Kloukinas[4], A. Baschirotto[2]

[1] University of Pavia – Italy. Department of Electrical Computer and Biomedical Engineering.
[2] Univesity of Milano Bicocca – Italy. Department of Physics G. Occhialini.
[3] Univesity of Salento – Italy. Department of Innovation Engineering.
[4] CERN, 1211 Genève 23, Switzerland.
[5] Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland.

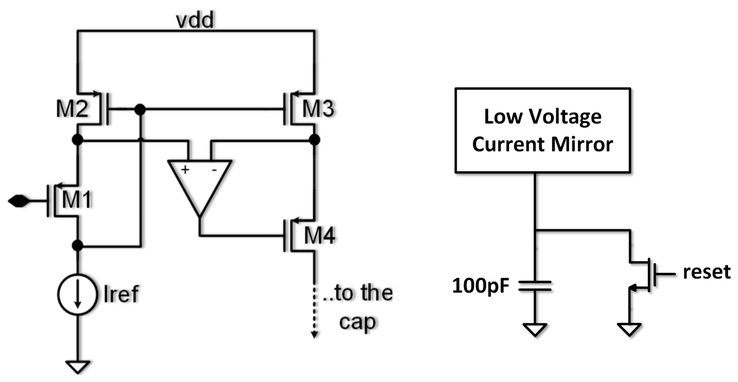
Abstract

The presented 12bit single slope ADC is part of a system (called GBT-SCA), aimed to sense and monitor electrical/physical parameters in the LHC experiments. Measurement accuracy has been achieved by the combination of an analog accurate ramp generation and a digital correction for offset and gain errors. Moreover, both analog and digital solutions have been adopted to guarantee rad-hard performance. A prototype has been fabricated in a 130nm CMOS technology and exhibits a maximum DNL/INL of 0.259 LSB and 1.87 LSB, respectively, for a power consumption of 800uW from 1.5V supply.

Ramp Generator

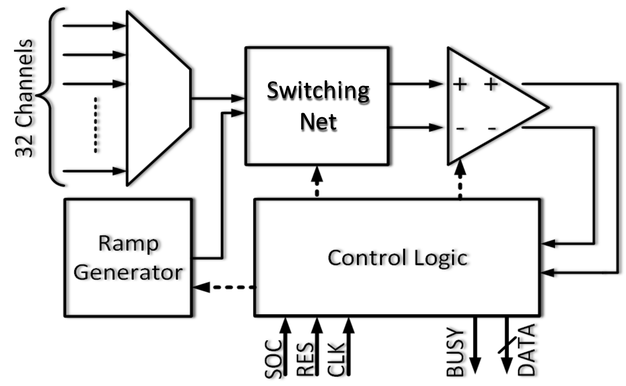
- The ramp signal is obtained charging a 100 pF grounded capacitor with a very accurate current
- A low-voltage regulated cascode current-mirror has been designed (6GΩ output resistance)
- Two working phases:
  - Reset
  - Charge

- Reducing non-linear parasitic caps at the ramp generator output is mandatory
  - Comparator's offset voltage vs. Comparator's input parasitic capacitance



Regulated Cascode and Ramp Generator

ADC Architecture



Wilkinson ADC block scheme

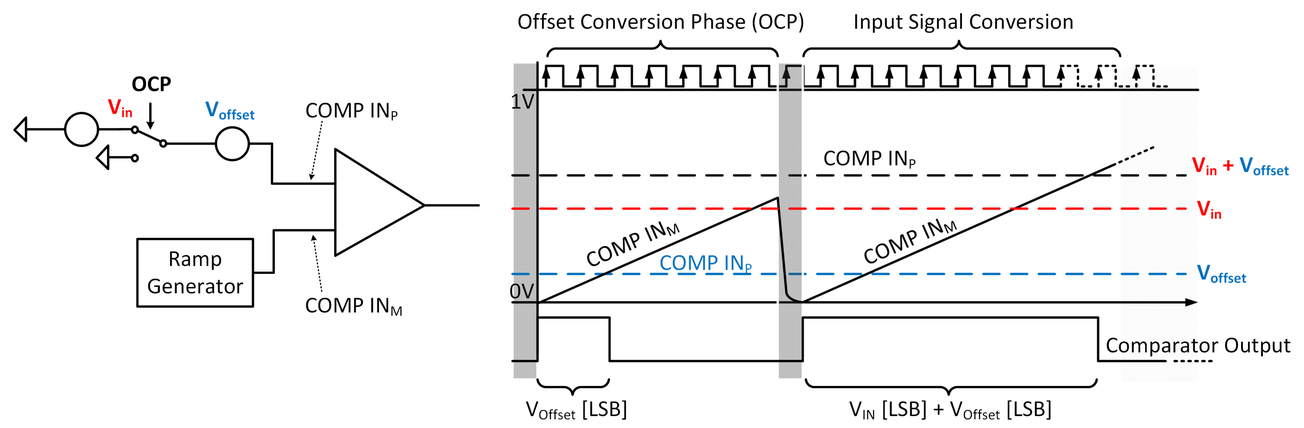
- The conversion is performed comparing the input signal with a ramp signal, in a kind of voltage-time conversion
- The conversion is proportional to $T_{conv} = C \cdot \frac{(V_{in} - V_{start})}{I_{charge}}$
- The main contributors to ADC performance are:
  - Ramp Linearity
  - Ramp Slope (→ ADC Gain Error)
  - Comparator Offset Voltage (→ ADC Offset Error)

…The aim of the introduced digital calibration is to compensate the offset and gain errors directly into the digital domain…

Offset Correction

The offset and its sign is digitized with the same Single-Slope conversion algorithm

- The (constant) offset voltage can be modeled as a DC voltage source in series with one comparator's input, according with its sign.
- The control logic starts the offset conversion assuming a positive offset (as shown in figure below)
- A negative offset implies an additional conversion phase with the comparator inputs polarity swapped
- Acting on the switching net is possible to obtain V_{in}[LSB]+V_{offset}[LSB] as input signal conversion result
  - The offset contribution can be subtracted in the digital domain



Offset Conversion vs. Input signal conversion

Gain Correction

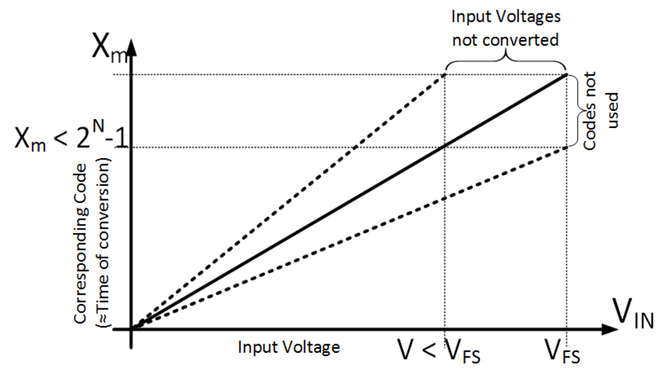
Mapping the actual set of measured results on the ideal one, using a simple operation as a digital multiplication

- The integrated capacitor and the charging current can vary of ±20%
  - The ramp slope has a wide variability
- Larger slope → lower conversion result
- Smaller slope → larger conversion result (suitable for calibration)
- The N bit calibrated result $X_{cal}^{[N]}$ is given by:

$$X_{cal}^{[N]} = \left(R^{[N]} \cdot X_{meas}^{[N]}\right)/2^N$$
$$R^{[N]} = (X_{ideal}/X_{meas}) \cdot 2^N$$

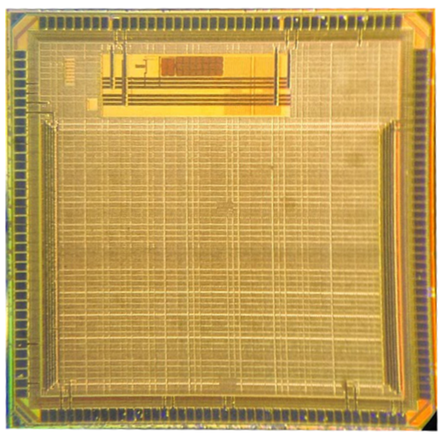
where the superscript represents the digital registers size, $X_{meas}^{[N]}$ is the N-bit measured conversion result, X_{ideal} is the ideal expected result and $R^{[N]}$ is a correcting factor, evaluated off-line

- To guarantee the best precision in the approximation with discrete numbers it's preferable to compute the R calculation with a test input signal close to the ADC full-scale

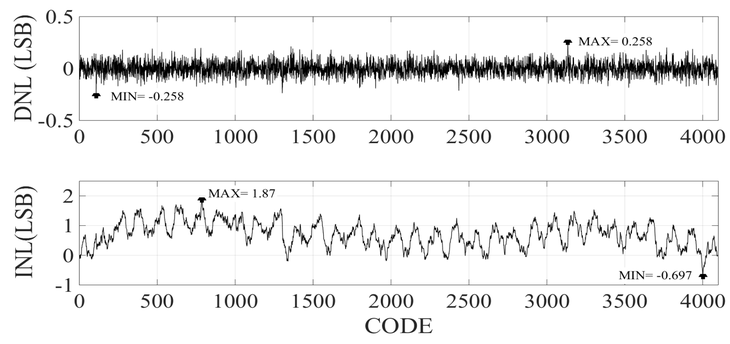


ADC characteristic vs ramp slope

Measurements

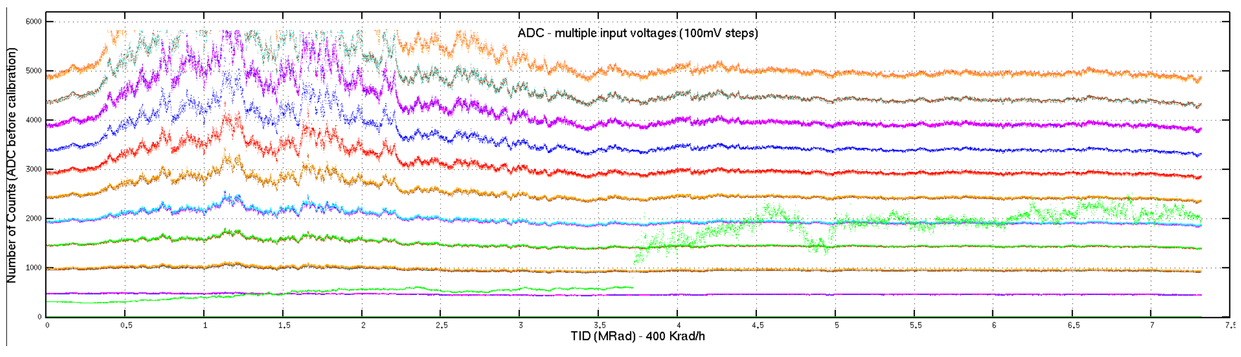


Chip Die and Measurements



	This work*	[2]*	[10]**	[11]*	[12]***
Process (CMOS)	0,13 µm	-	0,13 µm	0,35 µm	0,35 µm
Resolution (Bit)	12	12	9	12	10
Dyn. Range (V)	1	1,25	2,7	2	-
f_{clk} (MHz)	20	40	25	100	50
Conv. Time (s)	700 µ	< 1m	20,48 µ	400 n	42 µ
DNL (LSB)	< 0,3	0,1	< 0,065	< 0,58	< 0,5
INL (LSB)	< 1,9	1	< 0,95	< 0,63	< 1
Power (W)	< 800 µ	< 40m	631 µ	24,3 m	4,8 m

* Measurement Results, ** Post-Layout Simulations, *** Simulation Results



Radiation Effects

- The ADC has been measured with a 400kRad/h exposure rate
- The input signal has been incremented by 100mV step at time
- The greater is the input signal the greater is the deviation in the converted result in the range 0.5Mrad ÷ 3.5Mrad

Design Weak Point:

- The reset transistor in the ramp generator circuit