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A 12b Rad-Hard Digital Calibrated Single Slope ADC for LHC environment

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The presented 12bit single slope ADC is part of a system (called GBT-SCA), aimed to sense and monitor electrical/physical parameters in the LHC experiments. Measurement accuracy has been achieved by the combination of an analog accurate ramp generation and a digital correction for offset and gain errors. Moreover, both analog and digital solutions have been adopted to guarantee rad-hard performance. A prototype has been fabricated in a 130nm CMOS technology and exhibits a maximum DNL/INL of 0.259 LSB and 1.87 LSB, respectively, for a power consumption of 800uW from 1.5V supply.

Summary

Integrated microelectronic circuits are more and more used in high-energy physics experiments, like that inside the LHC (Large Hadron Collider) environment. They bring several advantages like a closer allocation to the detectors, cost reduction, performance improvement and better immunity to parasitic capacitance and EMI. The detector read-out circuits are very important inside the LHC experiments; they enable the collection of the huge amount of data, generated by collisions. Unfortunately, they are exposed to very high radiation levels, as it happens for detectors themselves. For this reason, in the CMS (Compact Muon Solenoid) central tracker, a dedicated monitoring system, called GBT-SCA (Giga Bit Transceiver - Slow Controller ASIC), has been implemented in order to provide real-time information about the status of silicon detectors, increasing lifetime and performance of the integrated circuits. This information is collected and converted into the digital domain by a Wilkinson (or single-slope) A-to-D converter. In a Wilkinson ADC, the conversion is performed comparing the input signal with a ramp signal (simply obtained integrating a charging current on a grounded capacitor), in a kind of voltage-to-time conversion. The longer is the time needed by the ramp to overcome the input signal, the higher will be the conversion result. The quite long conversion time, generally required by this kind of converter, does not represent an issue for this application because supply voltages, temperature and leakage currents variations are slower than the required conversion time. Although, in this application, the conversion time is not critical, the conversion accuracy, in terms of linearity, gain and offset are mandatory. This is because in this measurement path there is no control-loop for gain and offset errors. In this topology, the performance is strongly affected by ramp signal imperfections. There are mainly three contributors to the ADC performance: the afore-mentioned ramp signal linearity and slope (causing poor DNL/INL and a gain errors) and any residual reset error for the ramp signal or the offset voltage of the comparator (leading to an offset error). The ramp slope and the comparator offset voltage are often compensated in the analog domain: tuning the external current or modifying the value of the integrating capacitance for the first and using the chopper or auto-zeroing techniques for the second. Although these are relatively simple solutions, it could be the non-optimal choice for a scenario like that inside the LHC environment. Implementing the calibration in the digital domain can represent the solution, reducing the more radiation-susceptible analog circuitries. The ADC analog part has been designed with an ad-hoc sizing (based on measurements carried out on testing devices) and custom layouts, for reducing the radiation effects at the device level whereas the ADC digital part has been implemented adopting physical redundancy, as triplication and voting systems. The measured DNL (0.259LSB)and INL(1.87LSB) show how the digital calibration, here proposed, allows to mitigate the ADC non idealities keeping very good performance.

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