

Mu2e CRV Electronics

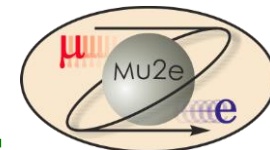
Sten Hansen/Paul Rubinov (speaker)

Mu2e CRV FE Electronics

9/30/2015



Mu2e Experiment @ Fermilab



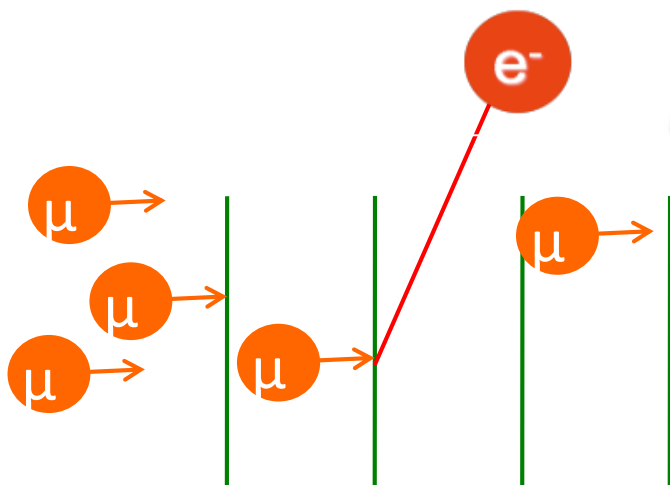
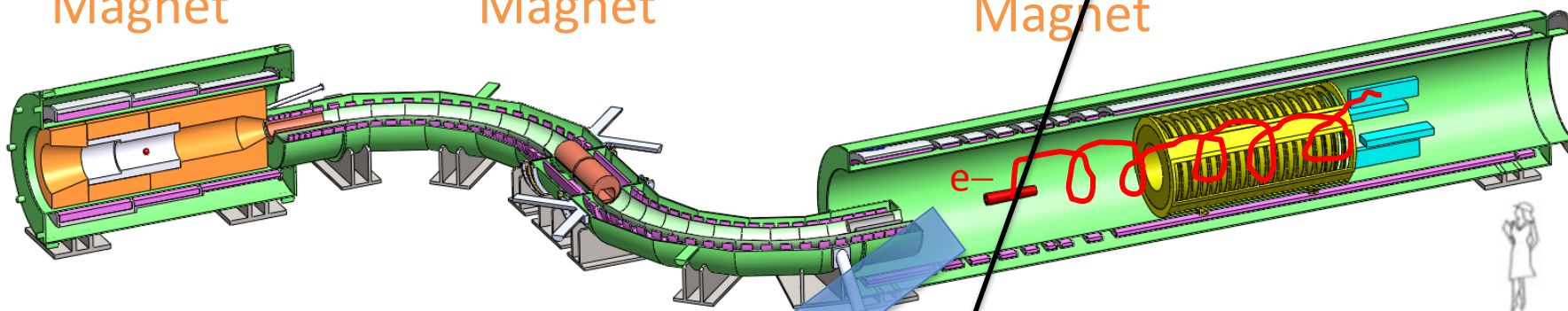
Designed to detect direct conversion of muons to electrons

Credit: Glenzinski
Kutschke

Production
Magnet

Transport
Magnet

Detector
Magnet



we look for evidence $\mu N \rightarrow e N$
1E-17 sensitivity = a few events in 3yr run

~500 signal like events
from cosmic rays in 3yr run



Mu2e Cosmic Ray Veto



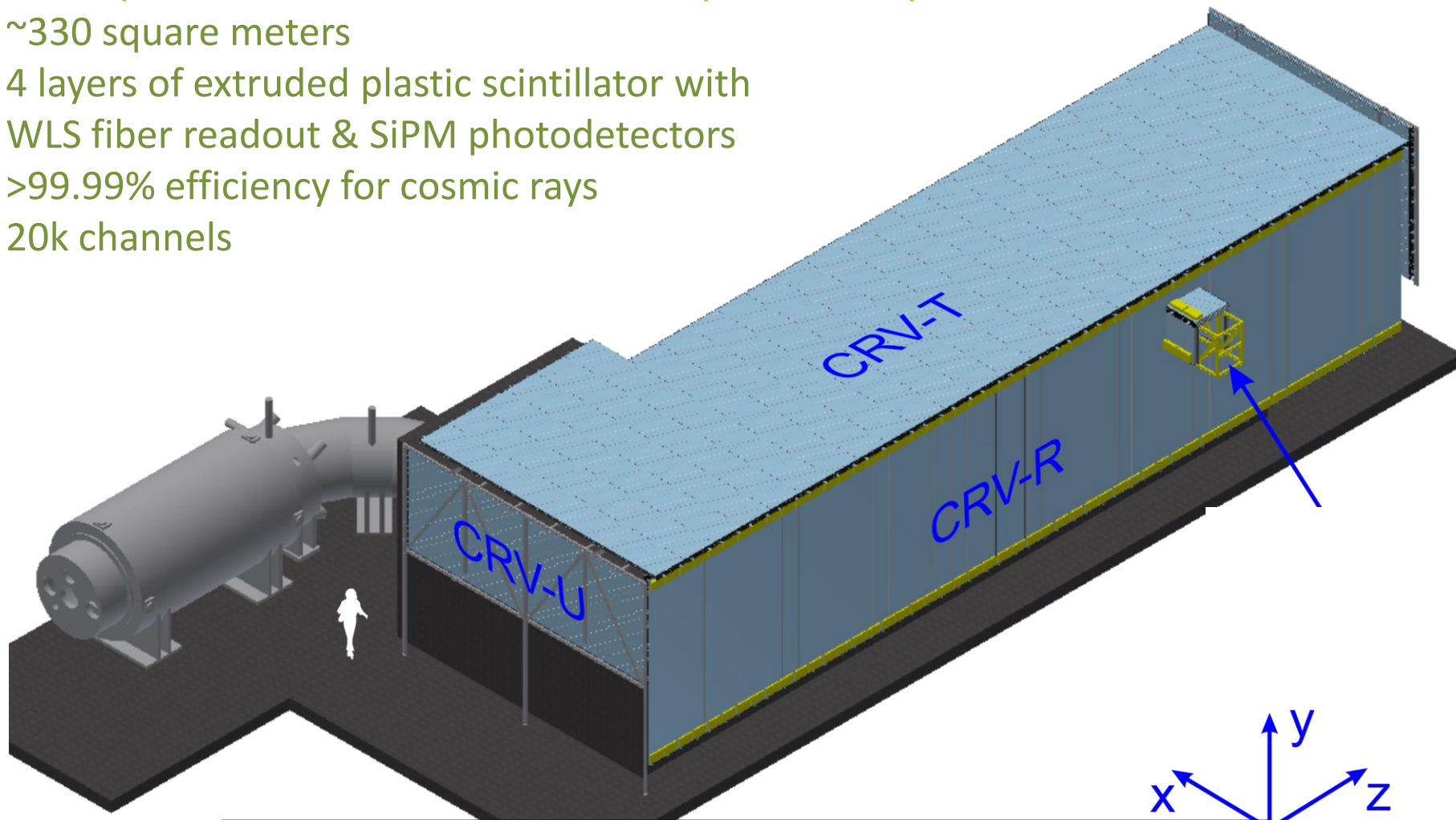
The experiment is covered on all sides by Cosmic Ray Veto

~330 square meters

4 layers of extruded plastic scintillator with
WLS fiber readout & SiPM photodetectors

>99.99% efficiency for cosmic rays

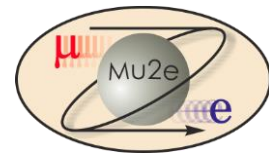
20k channels



Reduces the background from cosmic rays to less than
0.10 events over the course of the run



Design of CRV electronics

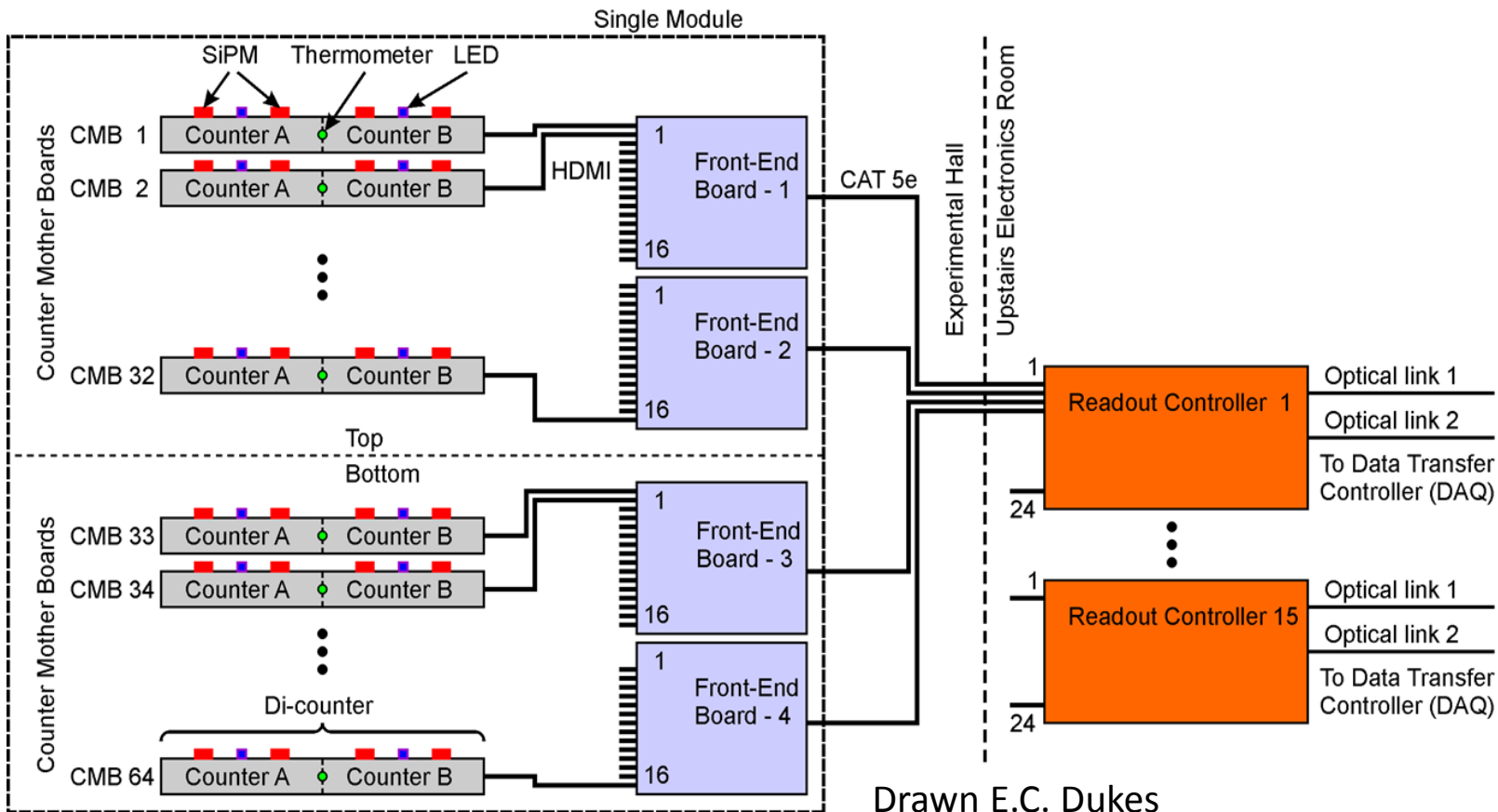
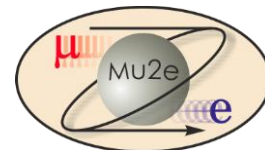


There are three board types in the system:

1. Counter Mother Board (CMB)
holds 4 SiPMs, flasher LEDs, temperature sensor
2. Front End Board (FEB)
digitizes the signals from 64 SiPMs
3. A Readout Controller (ROC)
gathers data and supplies power to 24 FEB over Cat-6
interfaces to the DAQ/timing/control system.

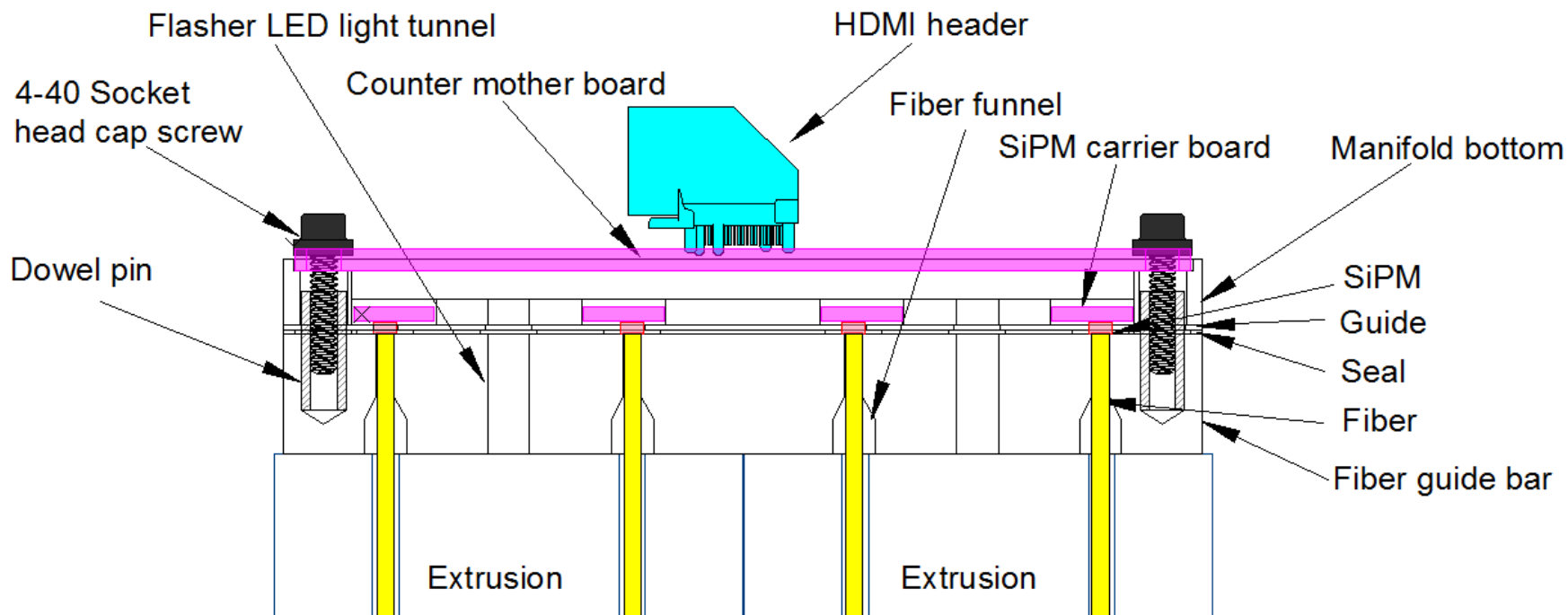
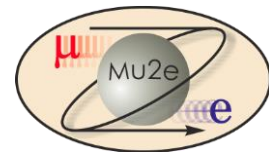


System Diagram





CMB sits at the end of the counters



Key points:

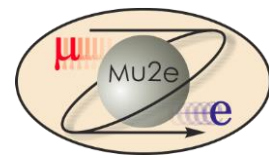
pole-zero compensation for SiPM

temp sensor

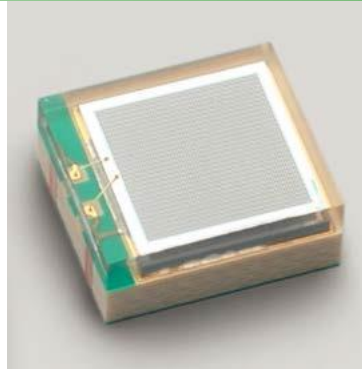
LED flasher



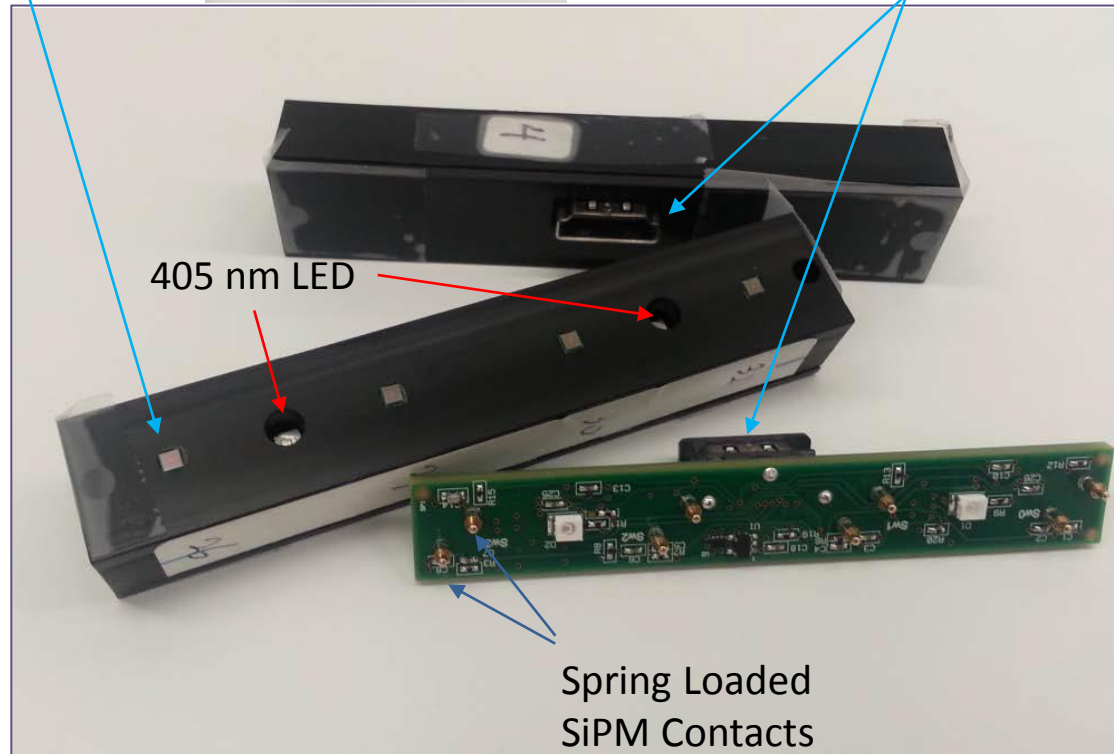
Counter Mother Board



2x2mm SiPM



HDMI Header

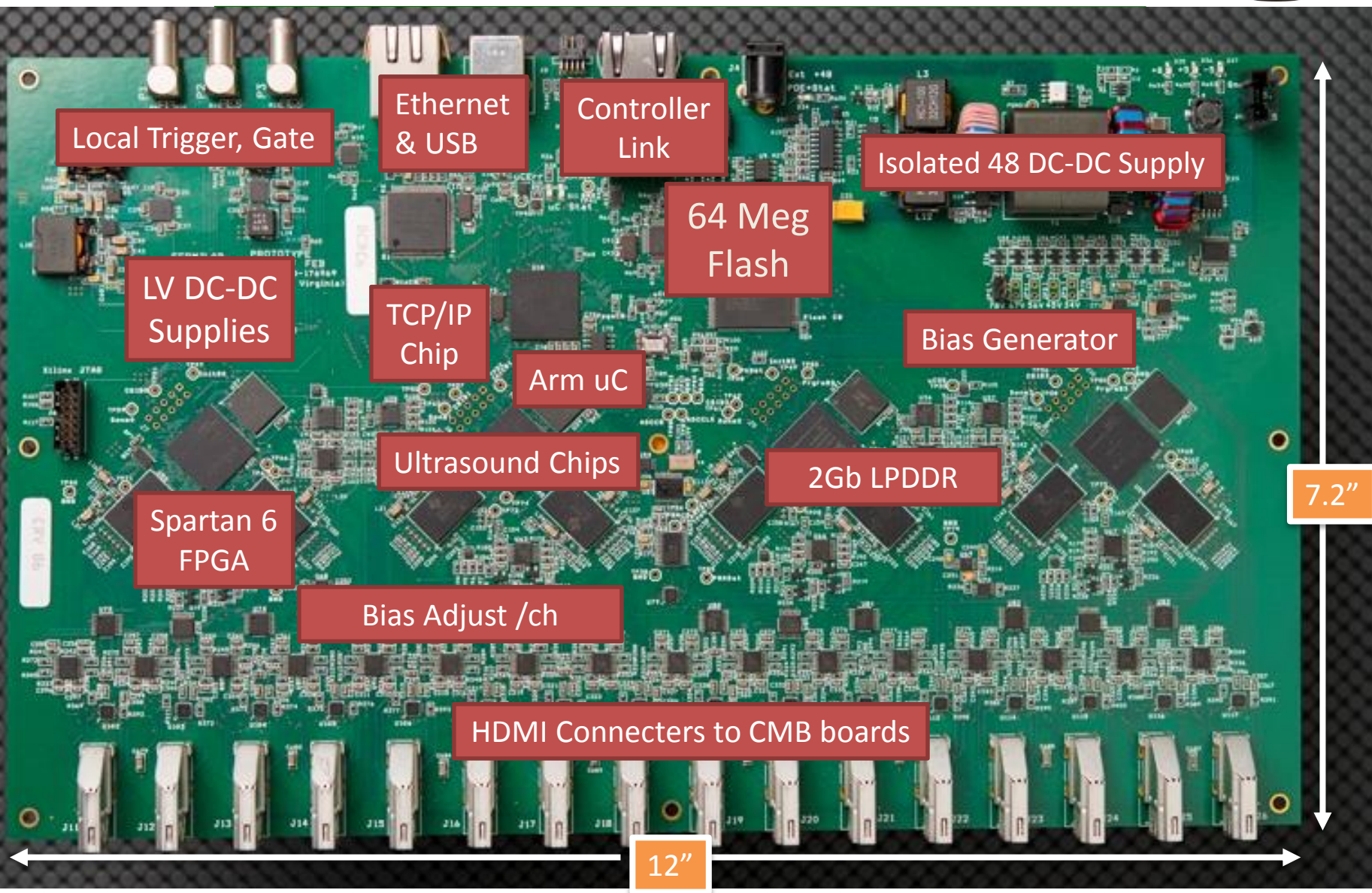


405 nm LED

Spring Loaded
SiPM Contacts

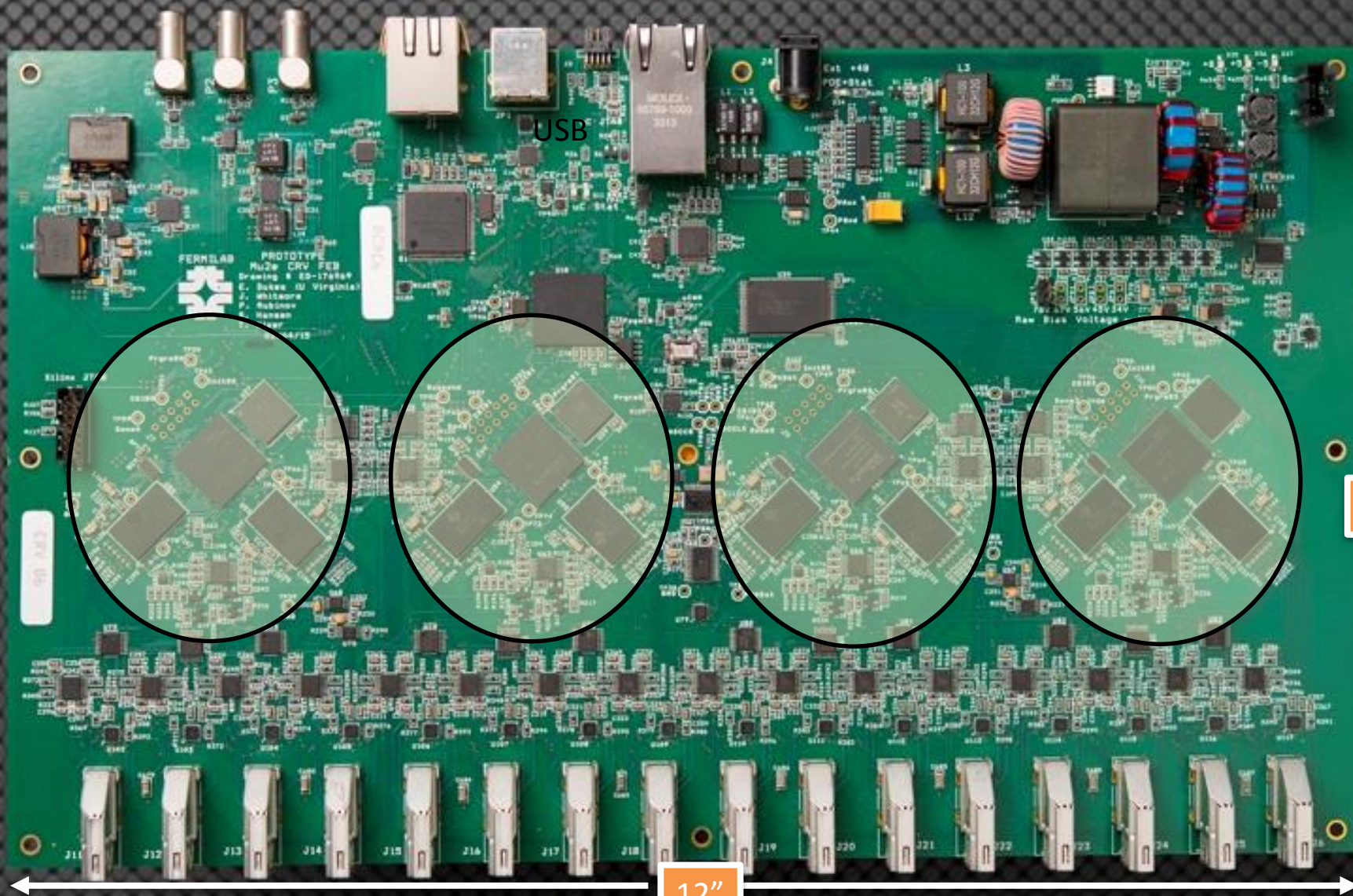
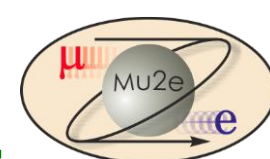


Front End Board





Front End Board



USB

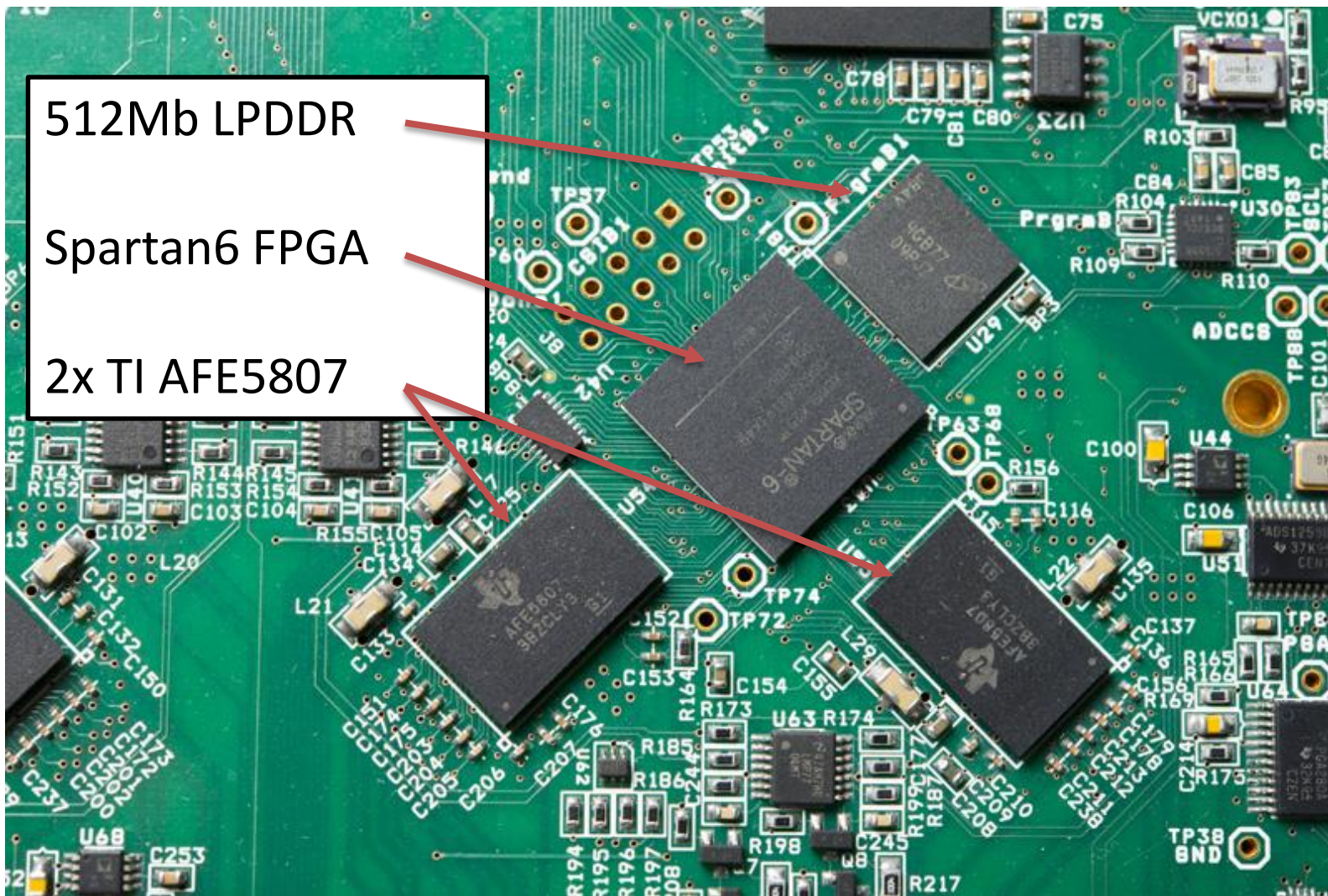
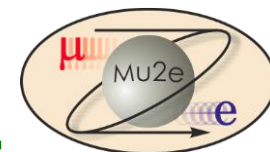
FERMLAB PROTOTYPE
Mu2e CRV FEB
Drawing # 65-176649
E. Suter (U Virginia)
J. Whitmore
P. Subramanyam
Hansen

7.2"

12"



Digitizer Block



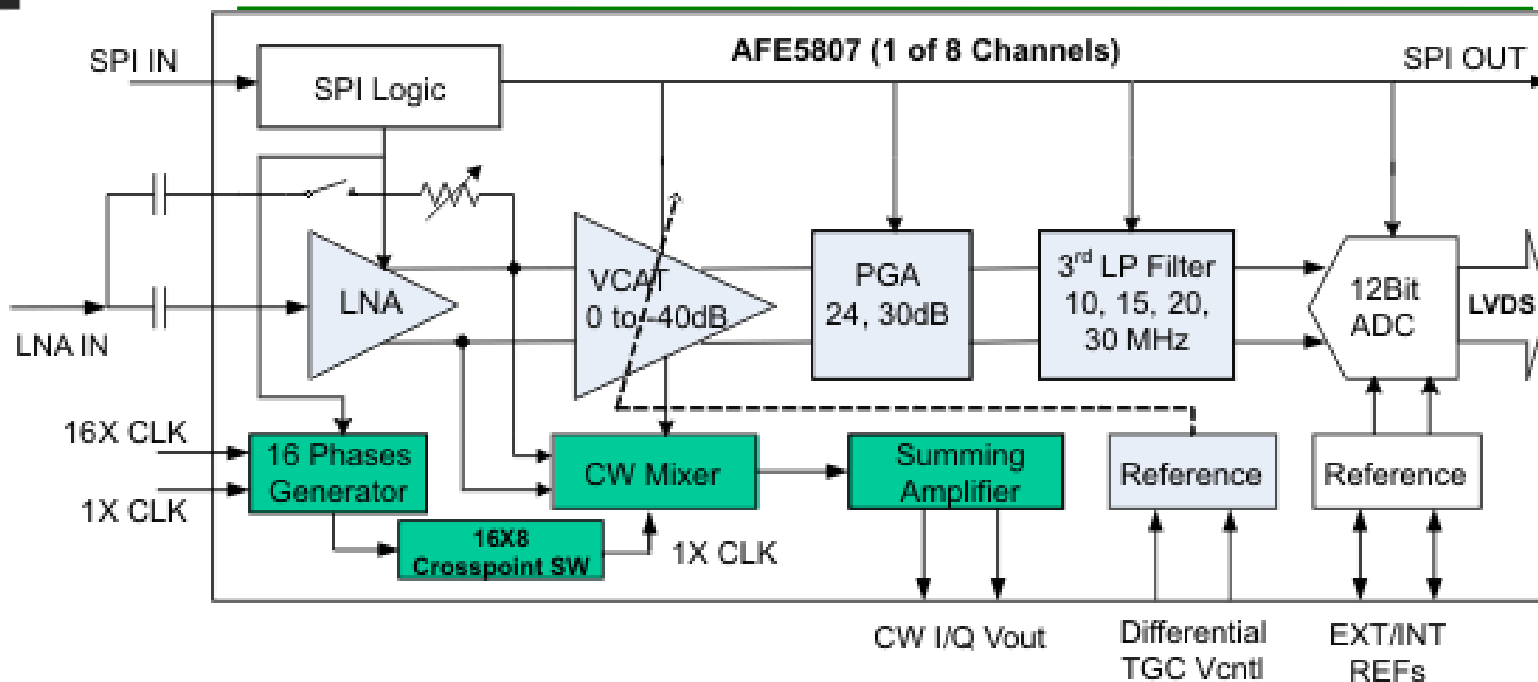
512Mb LPDDR

Spartan6 FPGA

2x TI AFE5807



TI AFE5807 Octal Ultrasound Digitizer Chip



8 Channels

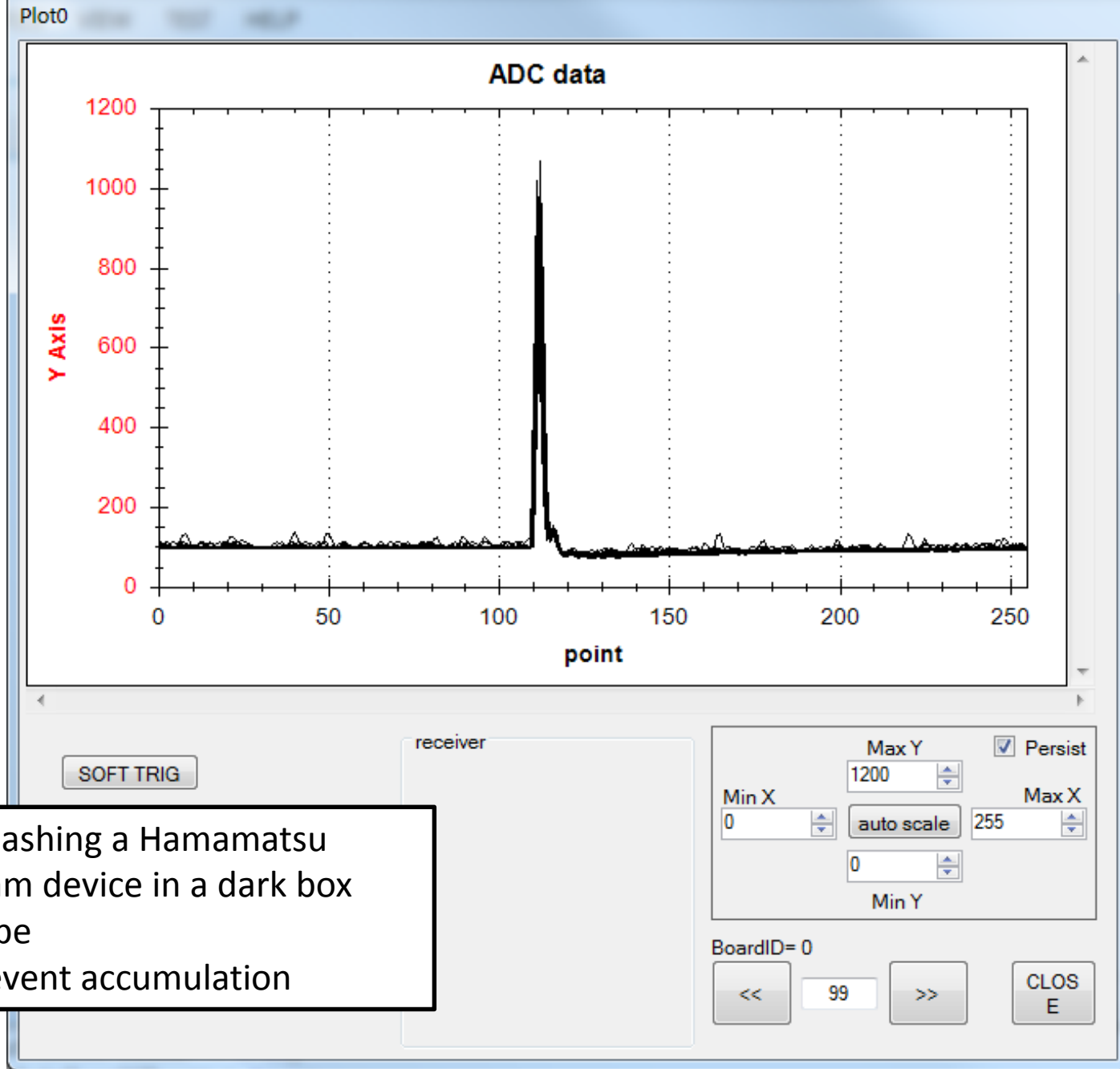
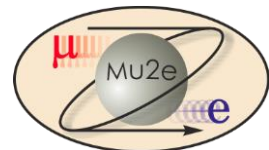
Low noise amp + Programmable gain amp + Anti-alias filter + 80msps 12 bit ADC

$1\text{nV}/\sqrt{\text{Hz}}$ input noise level

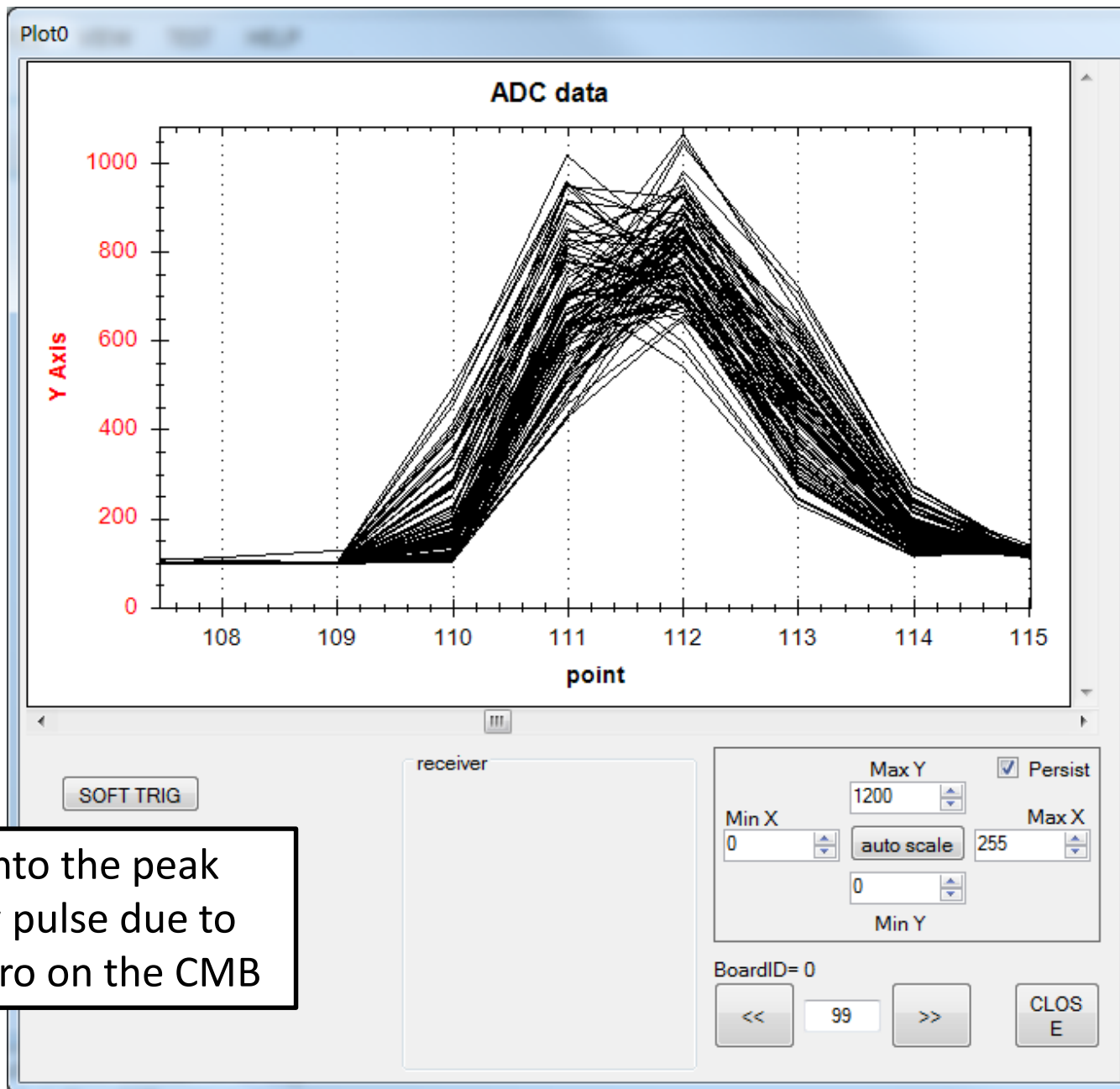
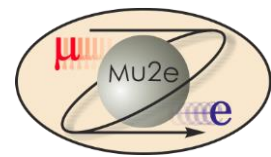
125 mW/channel (including ADC and LVDS drivers)

\$7 per channel

(We don't use the beam forming hardware (green squares) – disabled to save power)



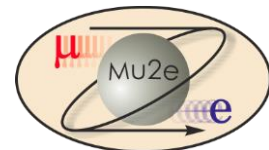
Led flashing a Hamamatsu
2x2mm device in a dark box
~ 75 pe
100 event accumulation



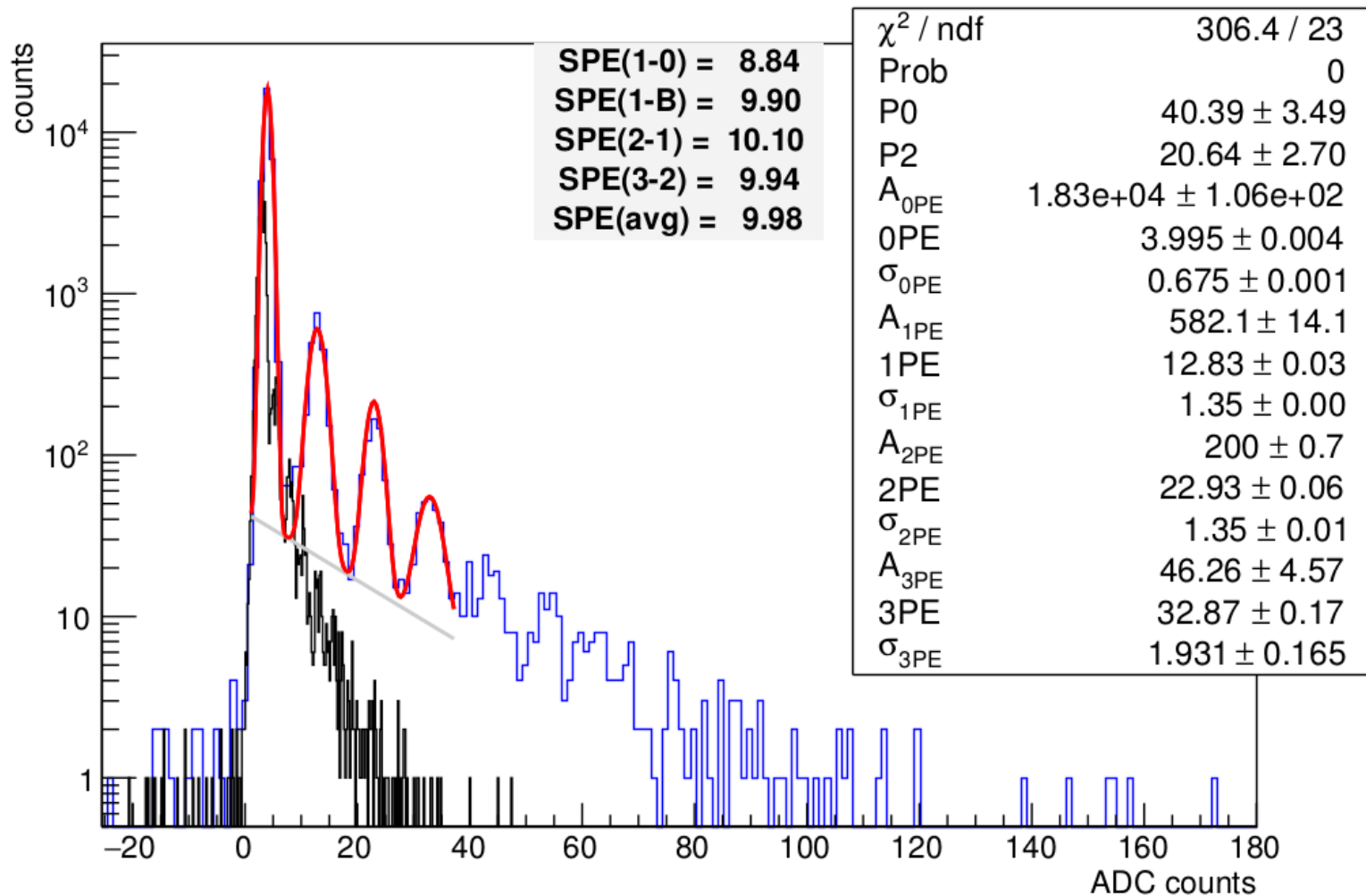
Zoom into the peak
Narrow pulse due to
pole-zero on the CMB



Allows easy calibration of gain

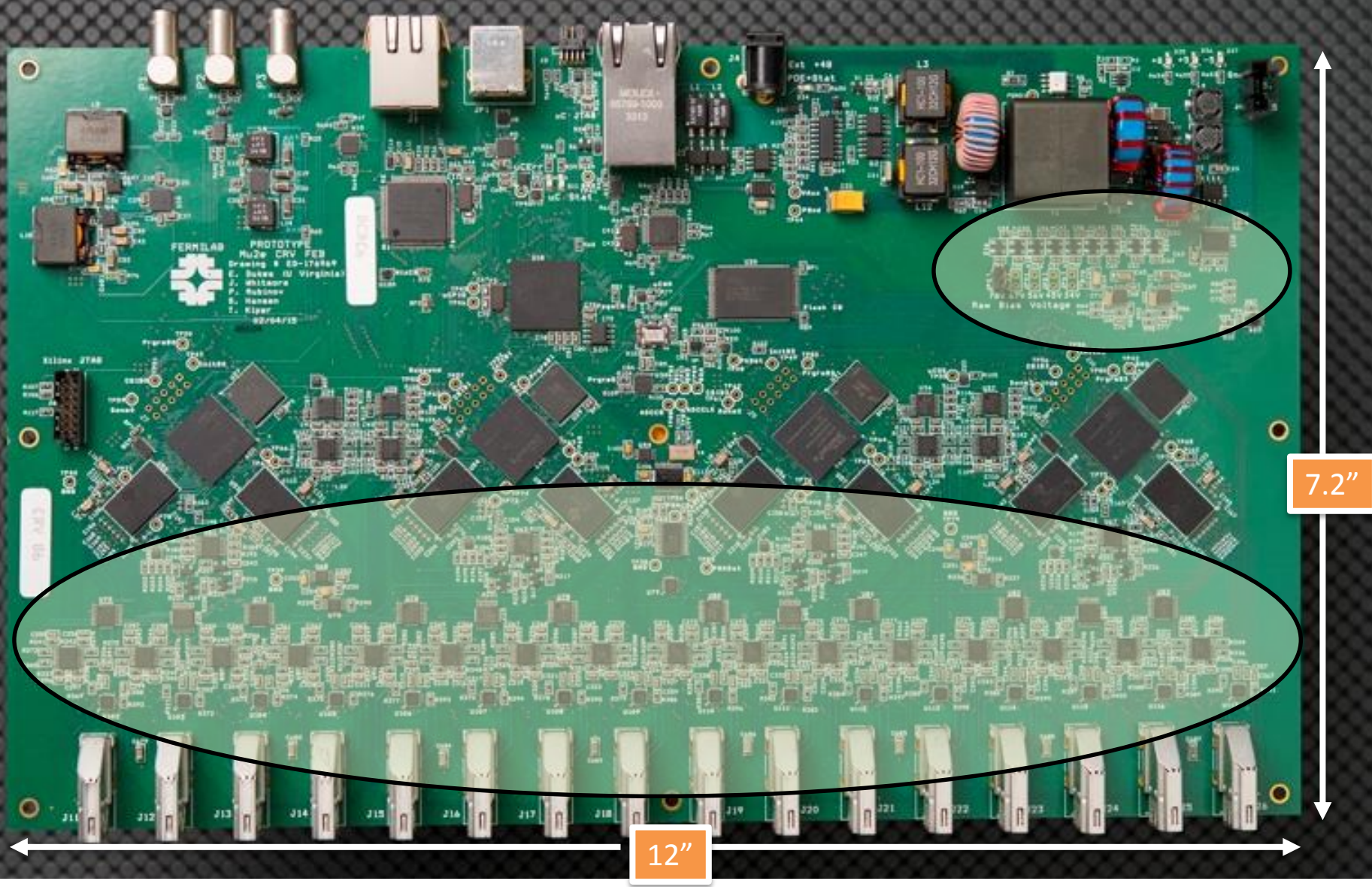
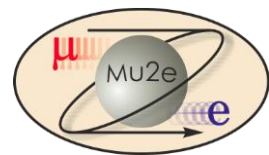


FEB2 Chan3 Calibration



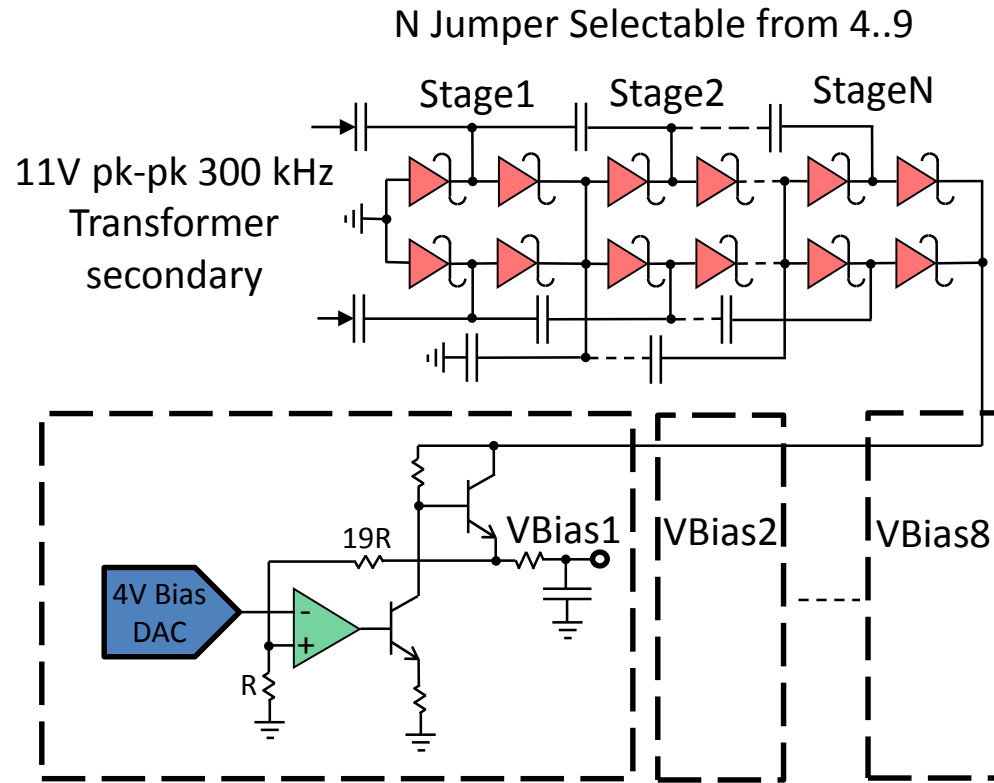
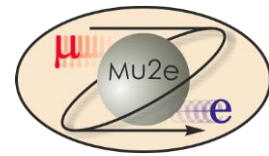


Front End Board- bias





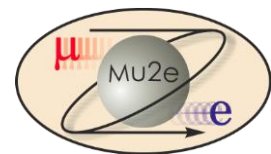
Bias generation



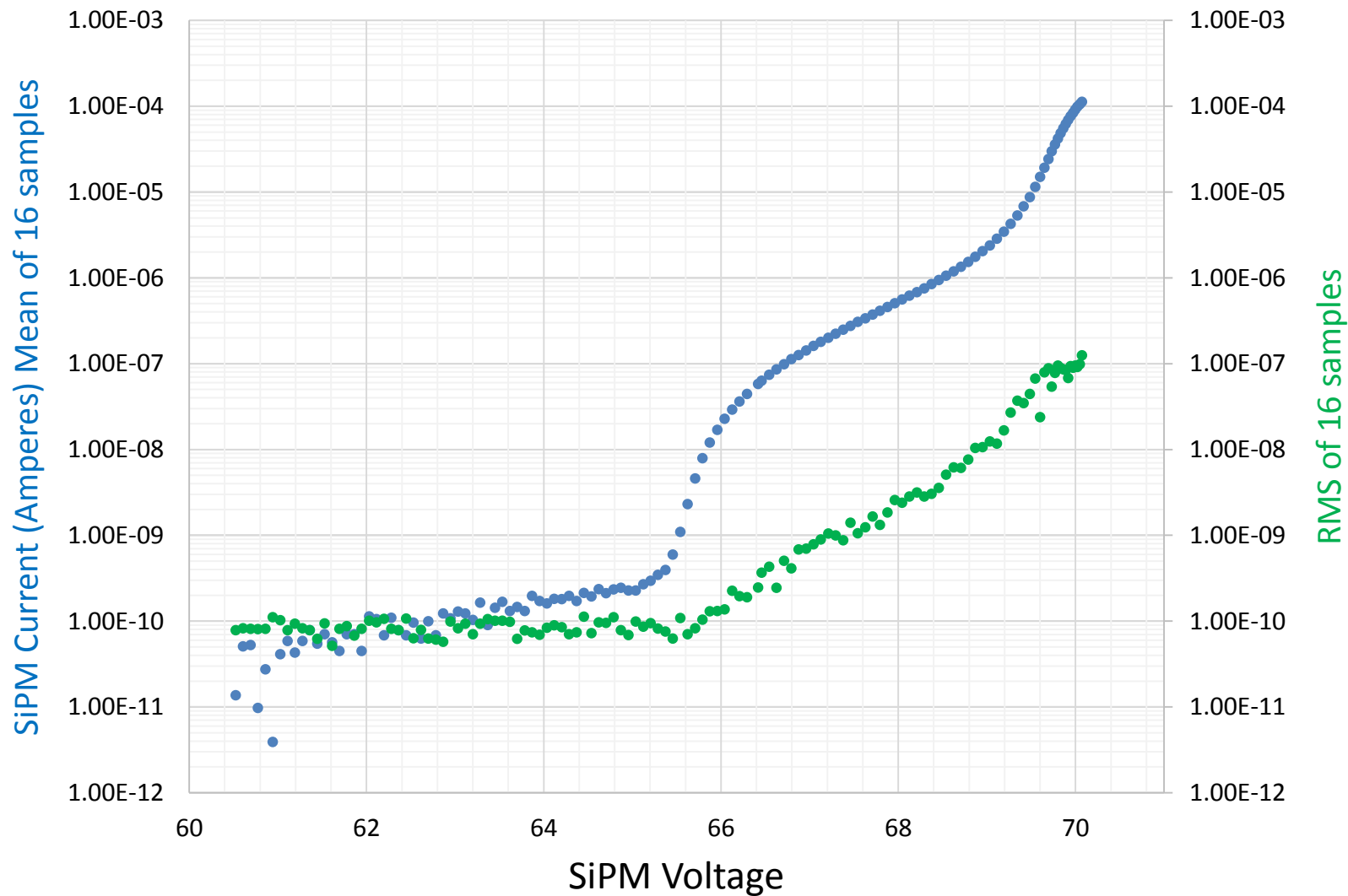
- Plus individual bias 12bit DAC (+-4V) on each channel applying offset on the low side of the SiPM across 4k
- Measure the voltage drop across the resistor to get current...



Current measurement/bias adjustment

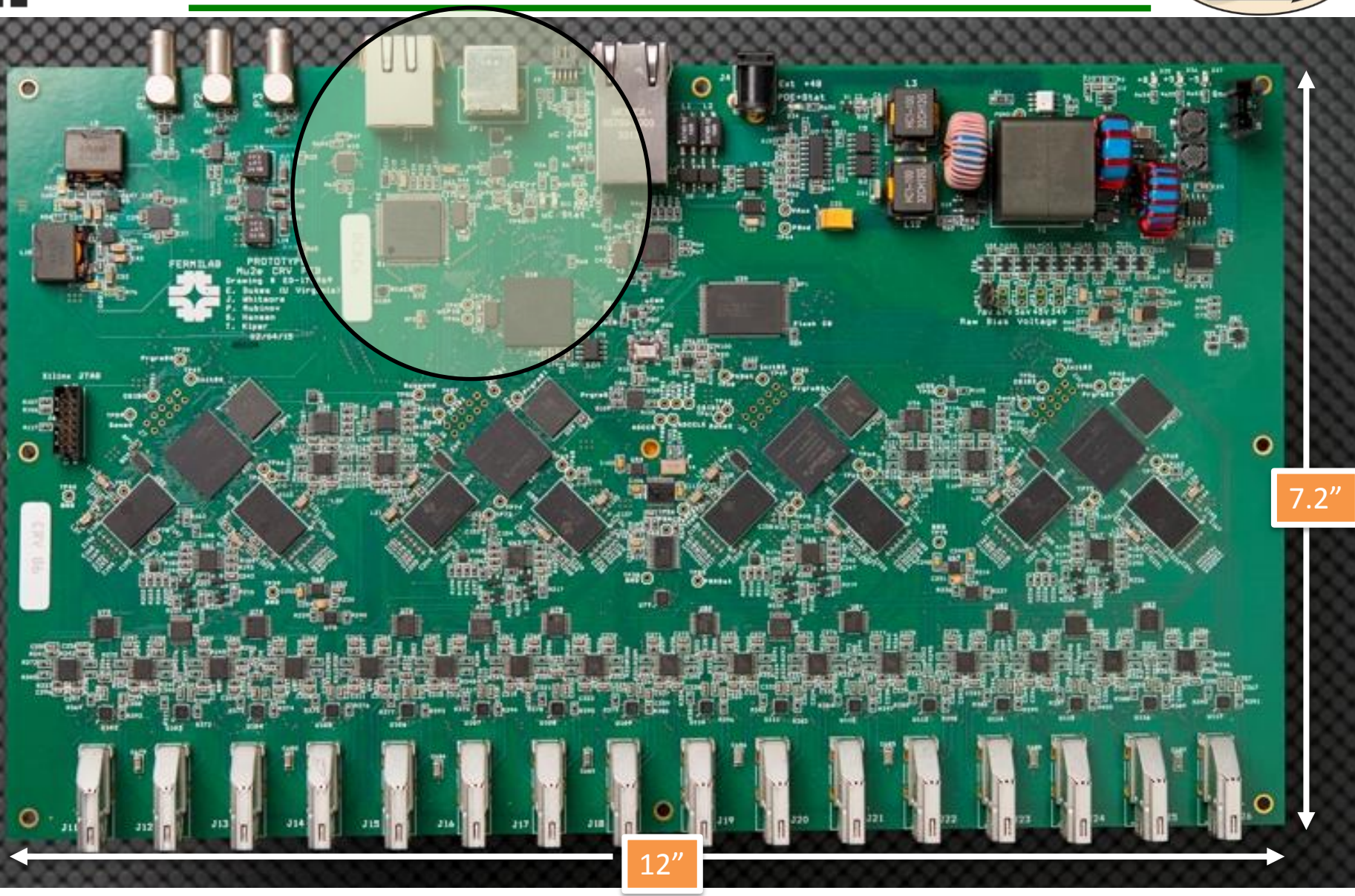
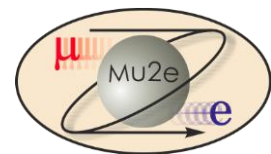


Hamamatsu 2x2mm IV Curve



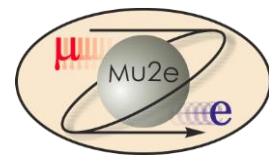


Front End Board - diagnostics





Simple but powerful diagnostics



```
C:\Windows\system32\cmd.exe - utelnet -n dcrc6 -e 5001
OS time: 20:47:35:143
Client connecting to: dcrc6.FNAL.GOV
Network_Thread_Start      uTelnet Session
help
←
- Mu2E CRV Front End Board V2, (Help= HE,H1,H2) -
Read
RDB WCnt r  Read Spill Data(16bit BINARY), WCnt(H)= # words to rd
            if r=1 data read ptrs unmodified, default 0=reset ptrs
            1st Sends 8 word Control Header then Data
            if no WrdCnt RDB returns WrdCnt= Last Spills Word Cnt
            if WrdCnt=0, Stop any Active Req, WrdCnt=9-0x20000000 Max
            if Spill Gate is Open, returns only 8 word NULL Header
RD a        FPGA Addr(Hex), a=A16, returns=Data16
RDI adr c   FPGA Read/and Incr, Addr(H), c=WrdCnt(D) Default=16
RDM adr c   FPGA Read/NoIncr FPGA Addr(H),c=WrdCnt(D)
Write
WR a d      Write Addr16(H), Data16(H)
AFE Chips
AFERD f a c Read AFE Reg, f=fpga(1-4), addr=(0x100...), c=WordCnt
AFEWR f a d Write AFE Reg, f=fpga(1-4), addr=(0x100...), d=Data16
AFERESET f  Soft Reset on AFE chips per fpga, f=(1-4,5=all)
PWR n       Power Enable AFE5807 per FPGA, 0=off, 1,2,3,4 (5=all on)
Misc
ADC n       uC ADC, temperature and ADC channels, n=1=noText
A0 n        ADC_ads1259, read data n times(default=1)
GAIN g r    PGA280 Gain= 1,2,4,8,16,32,64,128 (r=1 to reset chip)
HDR         Spill Header, last stored by RDB readout Cmd
LINK s      RJ45 LVDS Link direction, 0=REC, 1=XMIT
MUX f       Mux select on ADG1609 differential input, f=fpga(0-3)
STB f       Status Data(ASC), 22_Words_uC + 38_WordsPerFPGA, f=1-4 (def=1)
TRIG s      External Input Source, 0=RJ45(CLK/TRIG), 1=LEM0(TRIG)
TT          Test trigger pattern setup, RJ45CLK, 1-FPGA(2 AFE5807)
Save Setup
DSAV        Save Device Setup registers to Flash
DREC p      Recall/load Device Setup Regs from Flash, p=0(default setup)
FDUMP adr   Display FRAM (128 word block), fpga(1-4) adr=0,100,200,300
SDram       See Help Page 1 'H1' for SDram testing
Socket
SET         Network Setup Registers
SOCK        Display Network Socket Status
QUIT s      Close Network Socket, s=socket 0-3, Default= this connection
FRAM
FRD a       FRAM, Read a=addr(13bit) def=0, rtns data16 'FRS'=Chip Status
FWR a d     FRAM, Write a=addr(13bit), d=16bit(hex),note FDUMP cmd under Save
Flash
```

You can telnet to the board and ask it for help

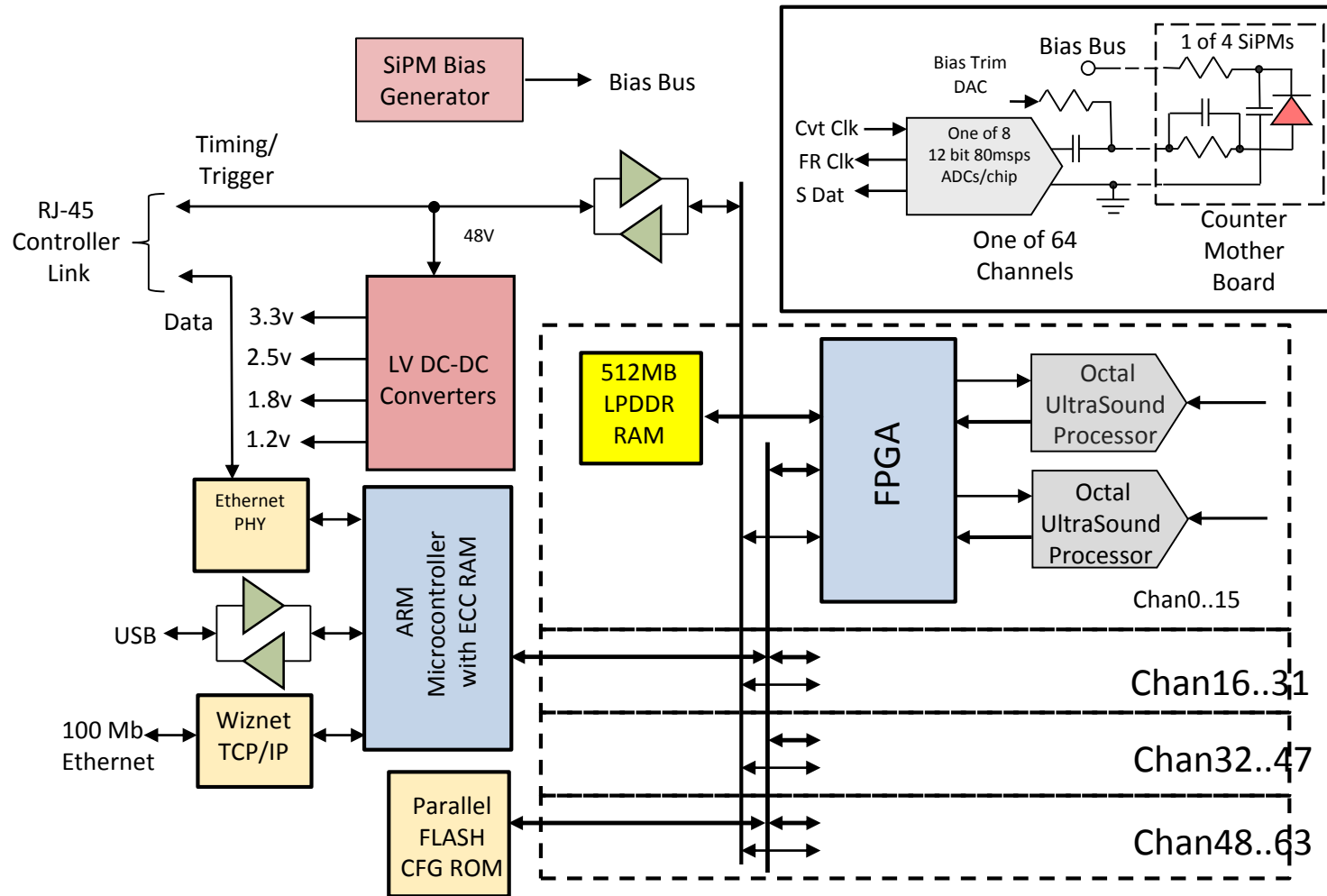
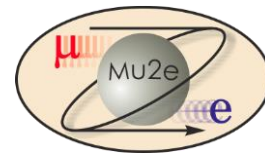
FLASH stores all parameters

uP restores all values (as desired)

Can also connect via USB (serial port)



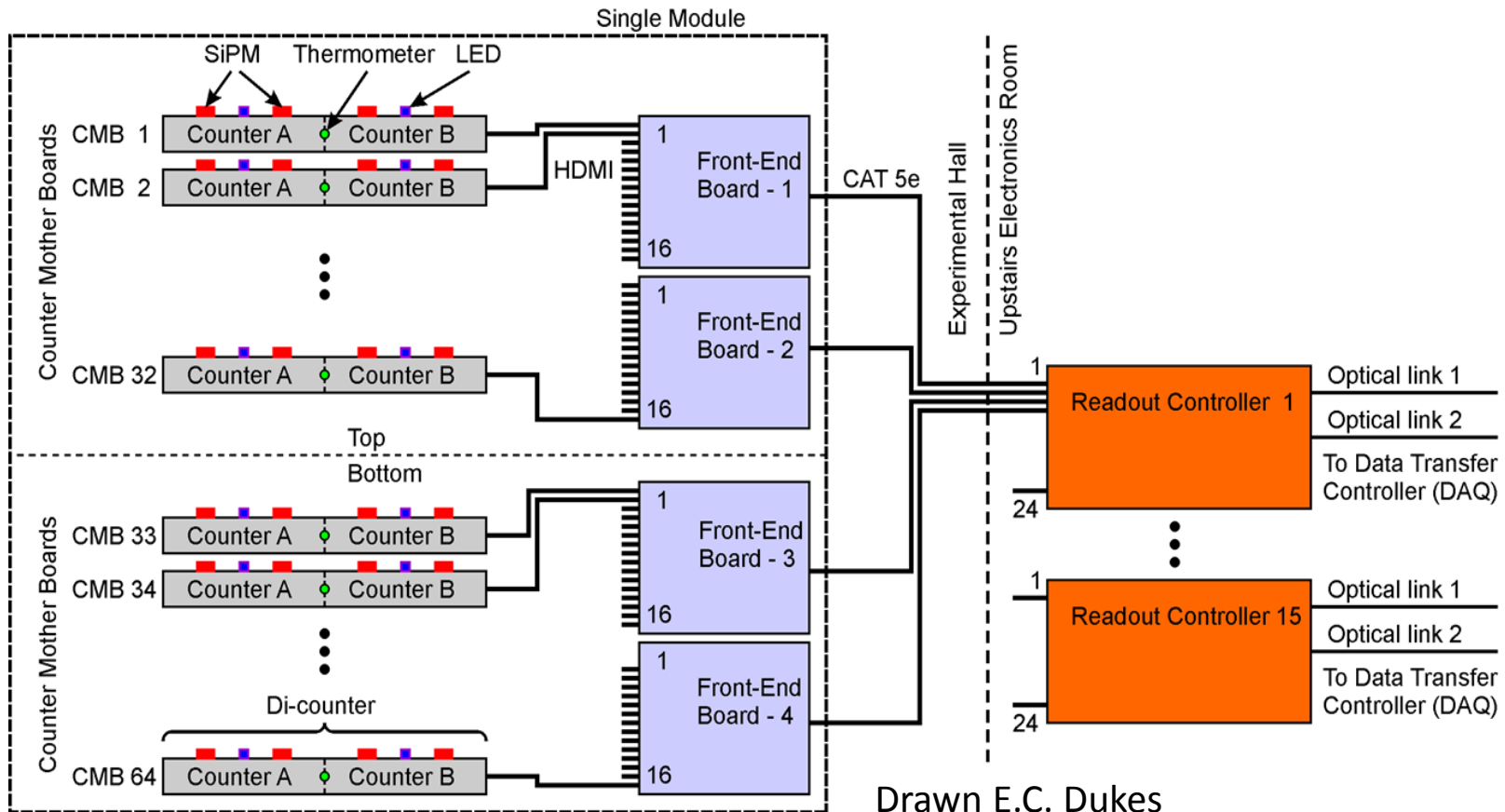
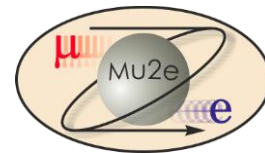
FEB block diagram



20W total power

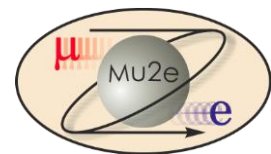


Connection to controller

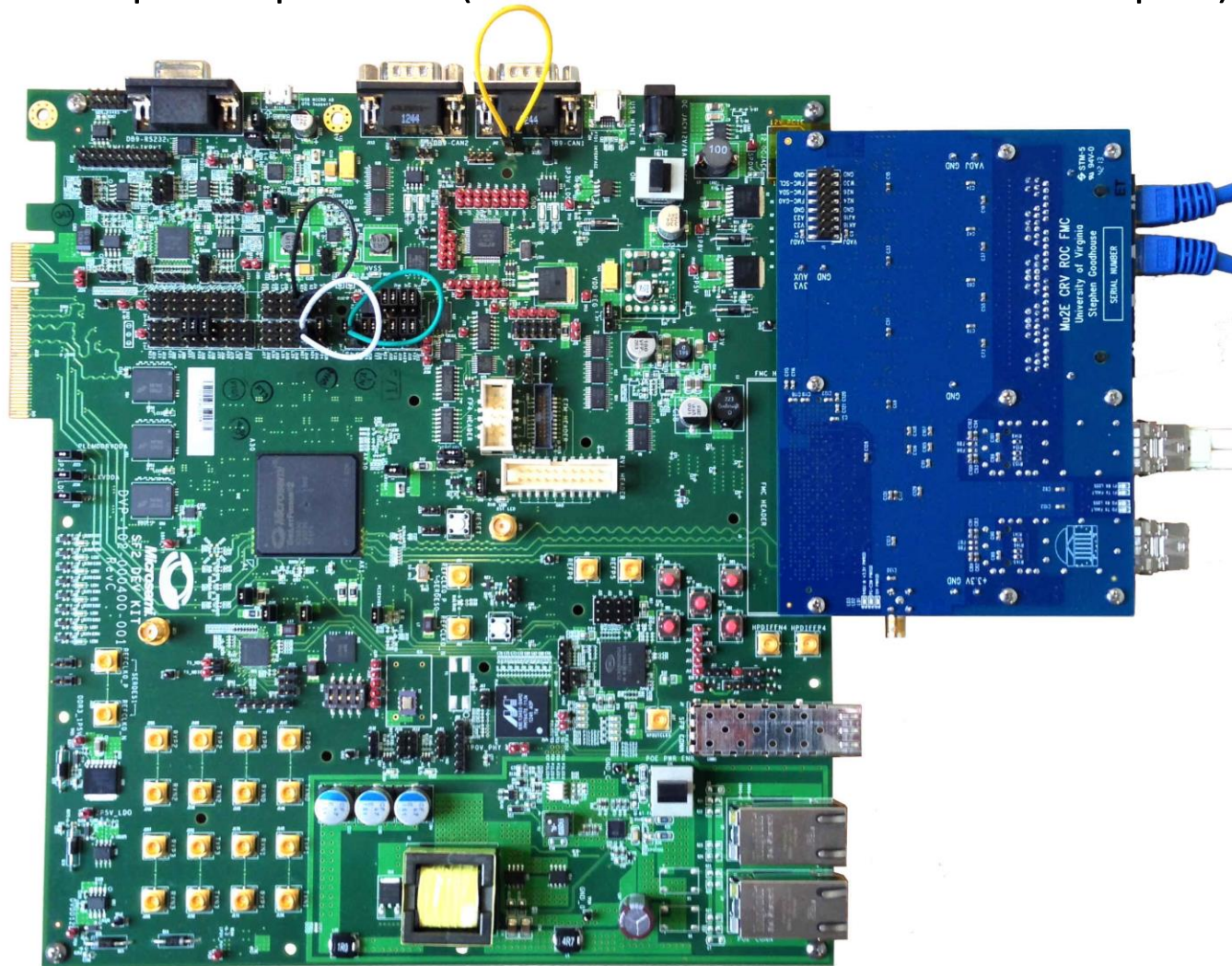




Readout controller

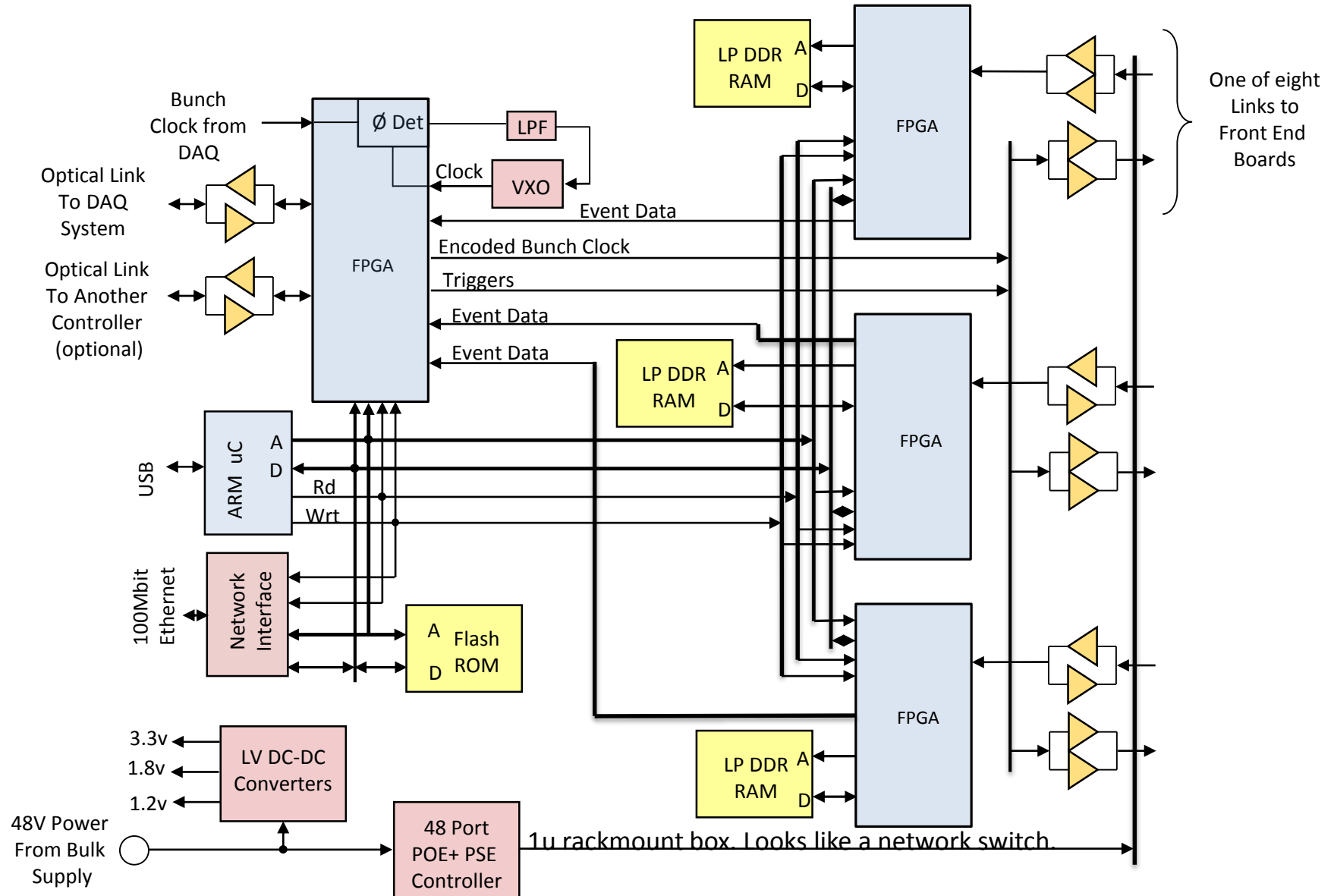
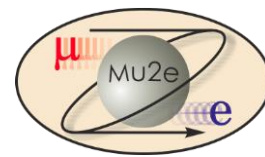


Controller development platform (FPGA evaluation board + FEB adapter):

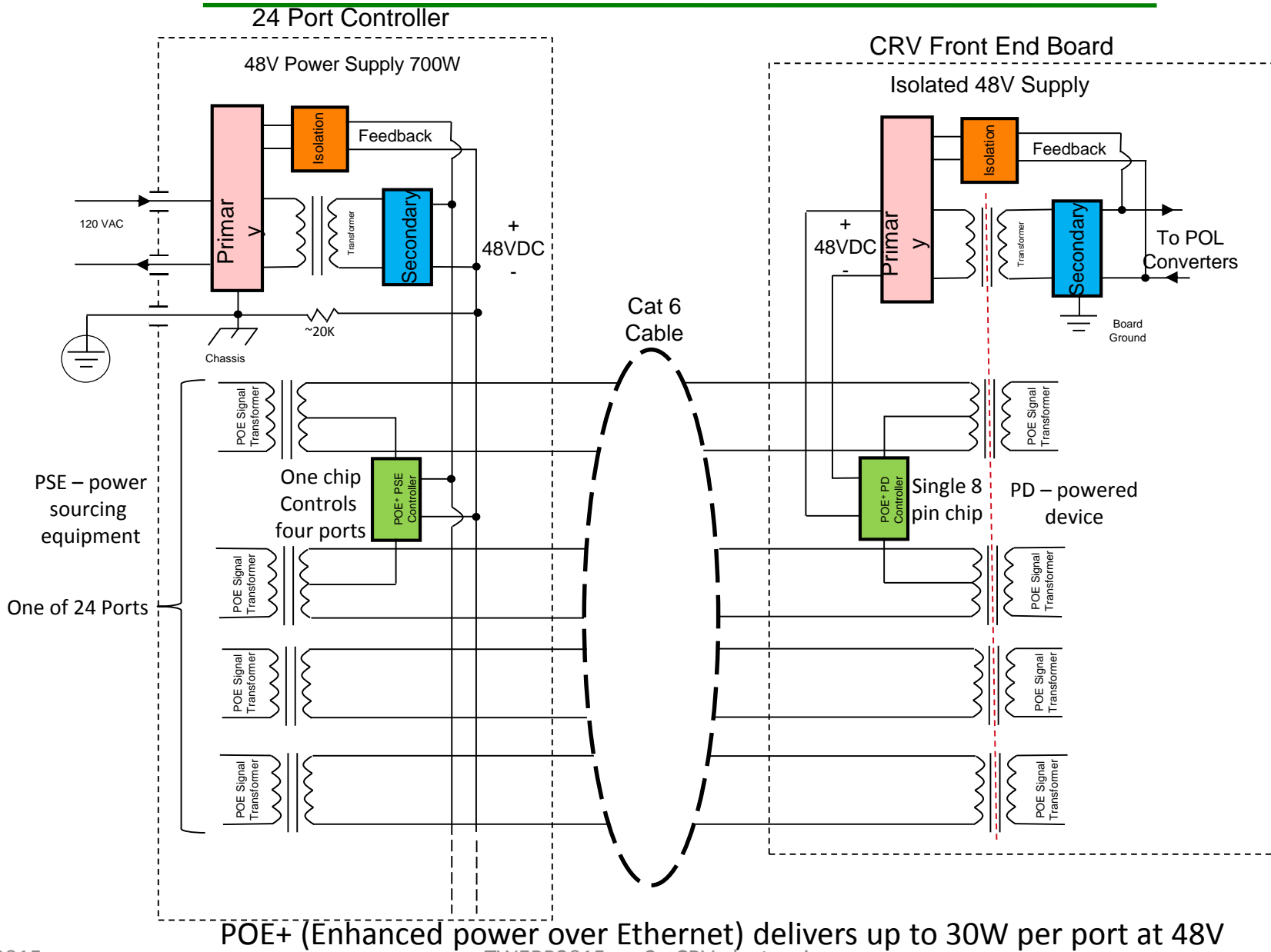
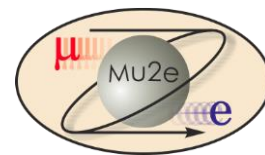




Readout controller Block Diagram

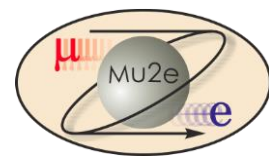


Power and Signal Arrangement





CRV electronics main features and status



CMB:

small board, many built, optimizing mechanics

FEB:

64 SiPMs, via HDMI connectors, digitizer at 80MSPS, 12bit

Bias generator split into eight groups of eight SiPMs up to 75V,

64 individual bias trims DACs with a $\pm 4V$ span

One 24 bit ADC + PGA with 64 channel multiplexer for measuring SiPM current

Single +48 volt power input either from the controller (or auxiliary input)

20W power consumption per FEB

100 Mbps Ethernet TCP/IP data connection for standalone data taking/diagnostics

100 Mbps data connection to the controller + timing & trigger

One GB of buffer memory (total per 64 ch)

Lemo connectors for local triggers

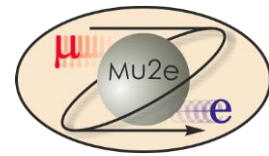
Material cost ~\$1500 per board

8 built, 7 working

Controller: prototype stage

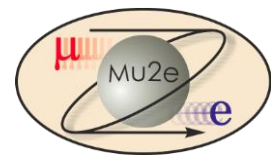


Summary

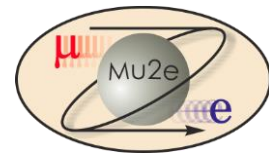


- The electronics is commercial off the shelf
- The design is derived from previous successful projects
- We have fabricated the first prototypes and tested them in test beams

- To Do:
 - Complete prototype readout controller
 - Test performance of FEB under radiation exposure
 - Design/verify local magnetic shielding



Backup slides



Radiation

Maximum expected dose at FEB locations $5e9/cm^2$ 1MeV neutron equivalent.
Two AFE chips exposed to $5E9/cm^2$ and $1E10/cm^2$ 400 MeV protons at CDH
No measurable change in behavior in either chip. Many thanks to CDH.

Remaining tasks

Expose whole board at a lower rate ($\sim 1E7/sec$) while powered to check for latch-up
None expected, but verify. Majority of the IC's including op-amps are CMOS, so no damage expected. If there is no latch-up, board at while powered to determine SEU rate.

SEU mitigation

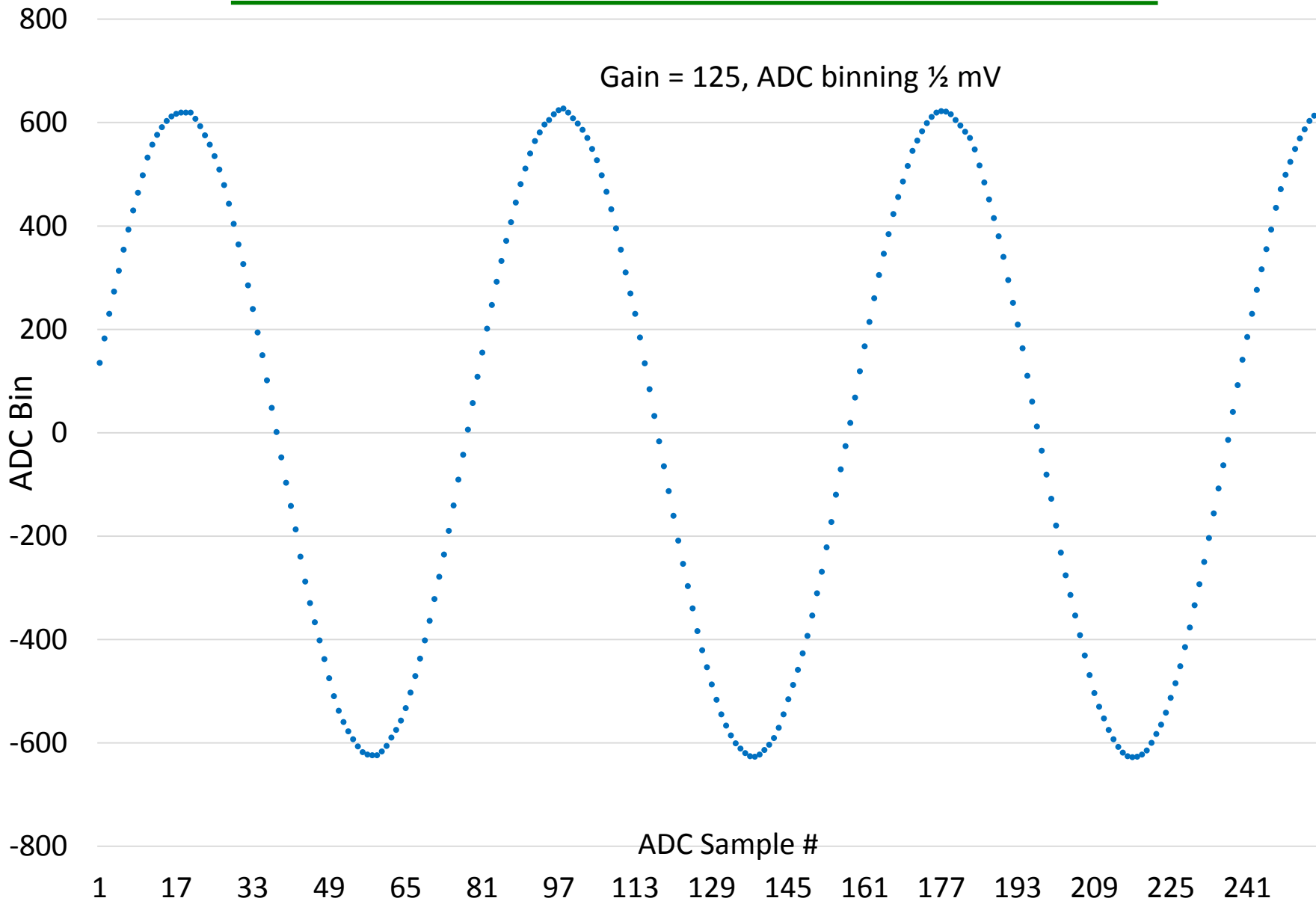
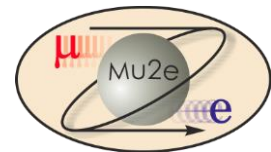
FPGAs set up with parallel configuration. We can re-load the FPGAs in $\sim 50ms$. FPGAs come with configuration checking hardware. Pin asserted when an error is detected.
Processor is medical device with dual CPUs cross checking each other. Resets if error found.
Use processor to check setup registers. Re-load if altered. Implement voting logic for a small fraction of the FPGA logic (e.g. counters). No error correction for event data.

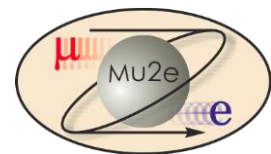
SEU rate estimate

Xilinx quotes a neutron cross section of $1E-14 cm^2/bit$ of configuration RAM. XC6SLX25 has $\sim 7E6$ config bits. Estimate $\sim 50Hz/cm^2$ during running. One SEU/FPGA every 78 hours. With 1200 FPGAs expect one config bit flip in the CRV every four minutes. On average five config bit flips required to change FPGA behavior. Simplest response is to unconditionally reset once every accelerator super cycle (1.33 seconds).

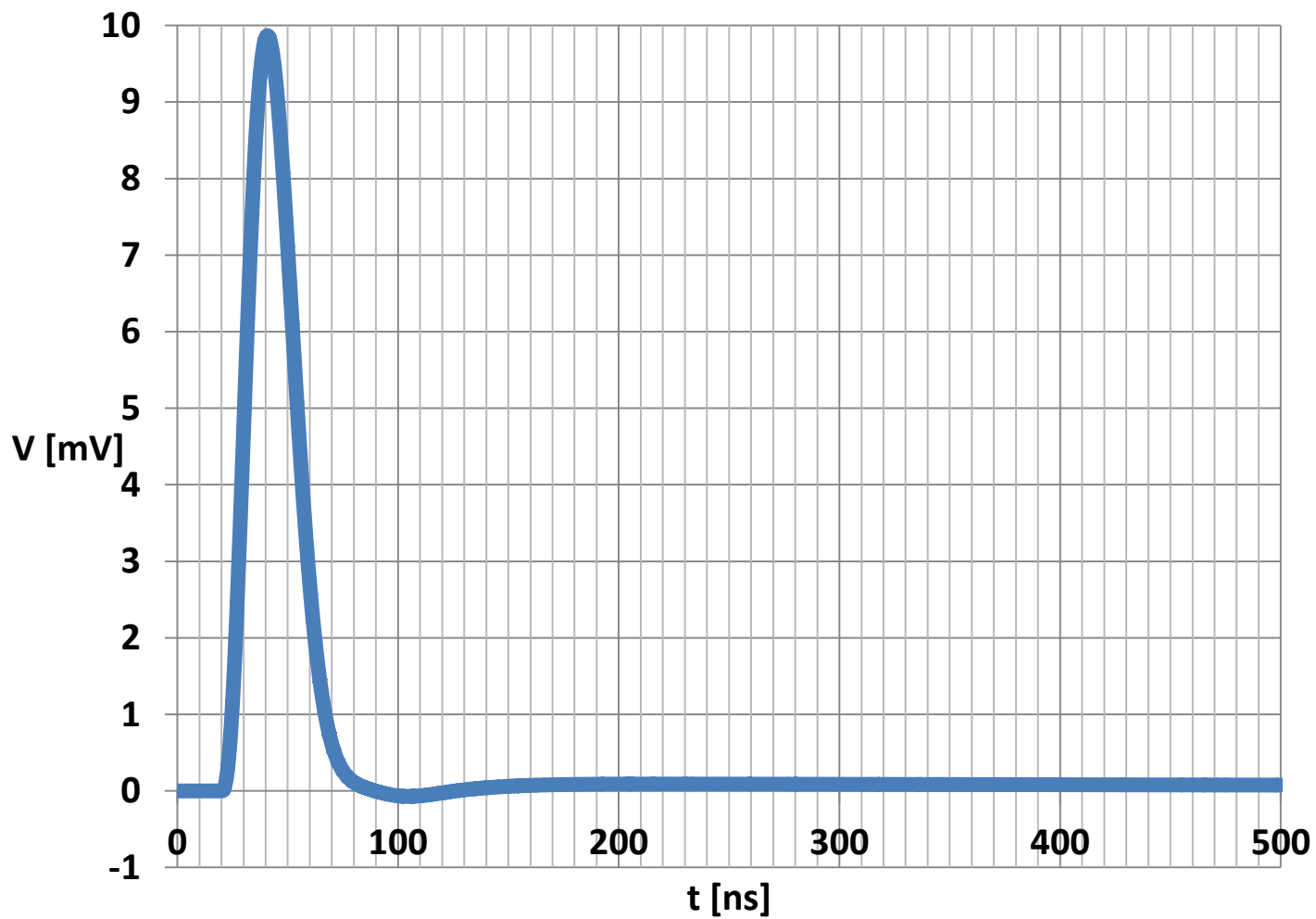


AFE Trace 5mV pk-pk 1MHz Input



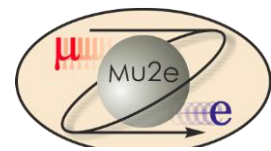


Simulation of a 1p.e. signal at the ADC input

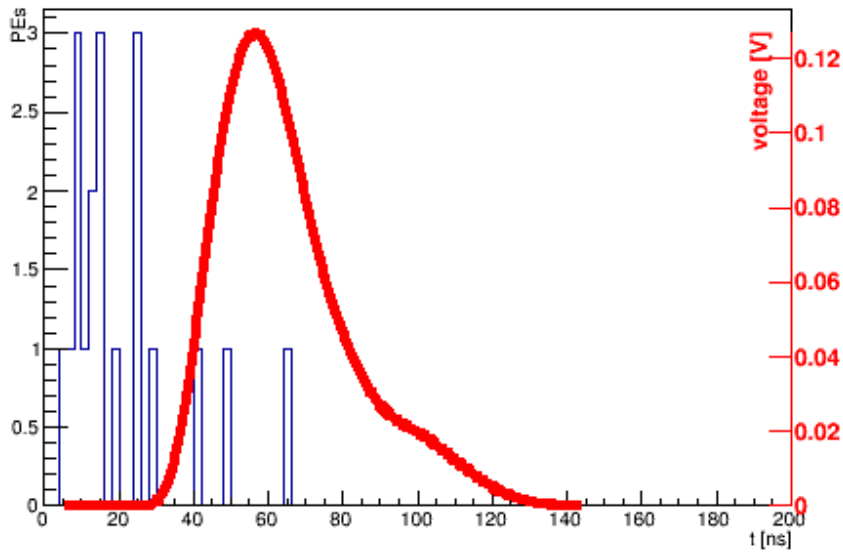




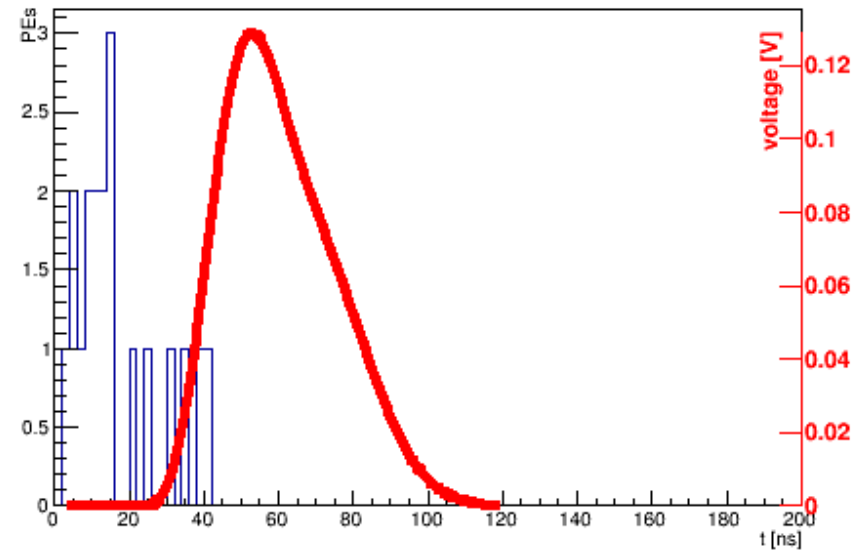
Ralf Erlich's simulation of p.e. arrival times and the resulting ADC input voltage



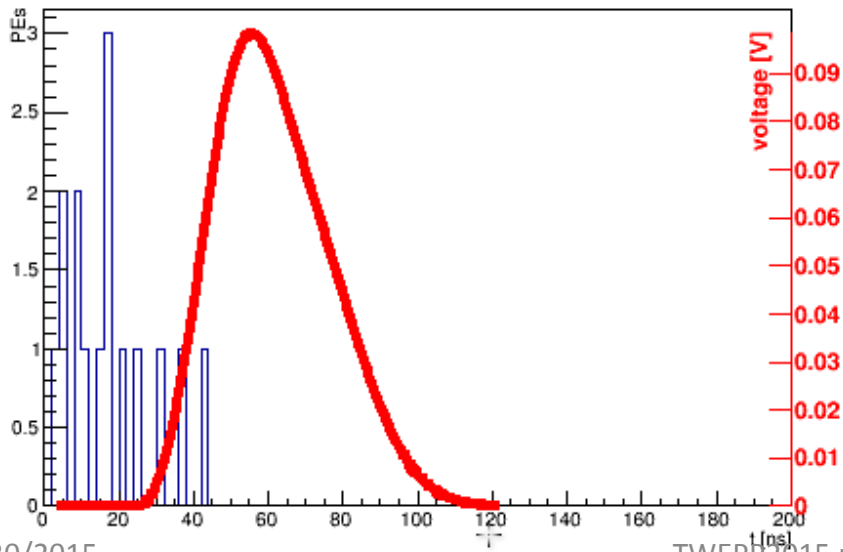
Fiber: 0, Side: 0



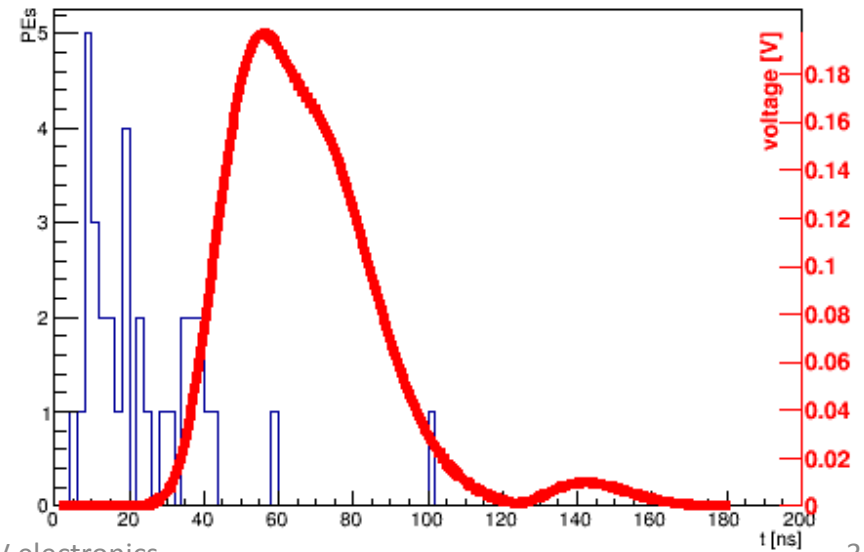
Fiber: 0, Side: 1

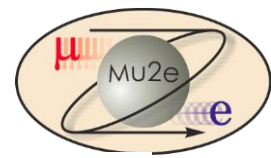


Fiber: 1, Side: 0

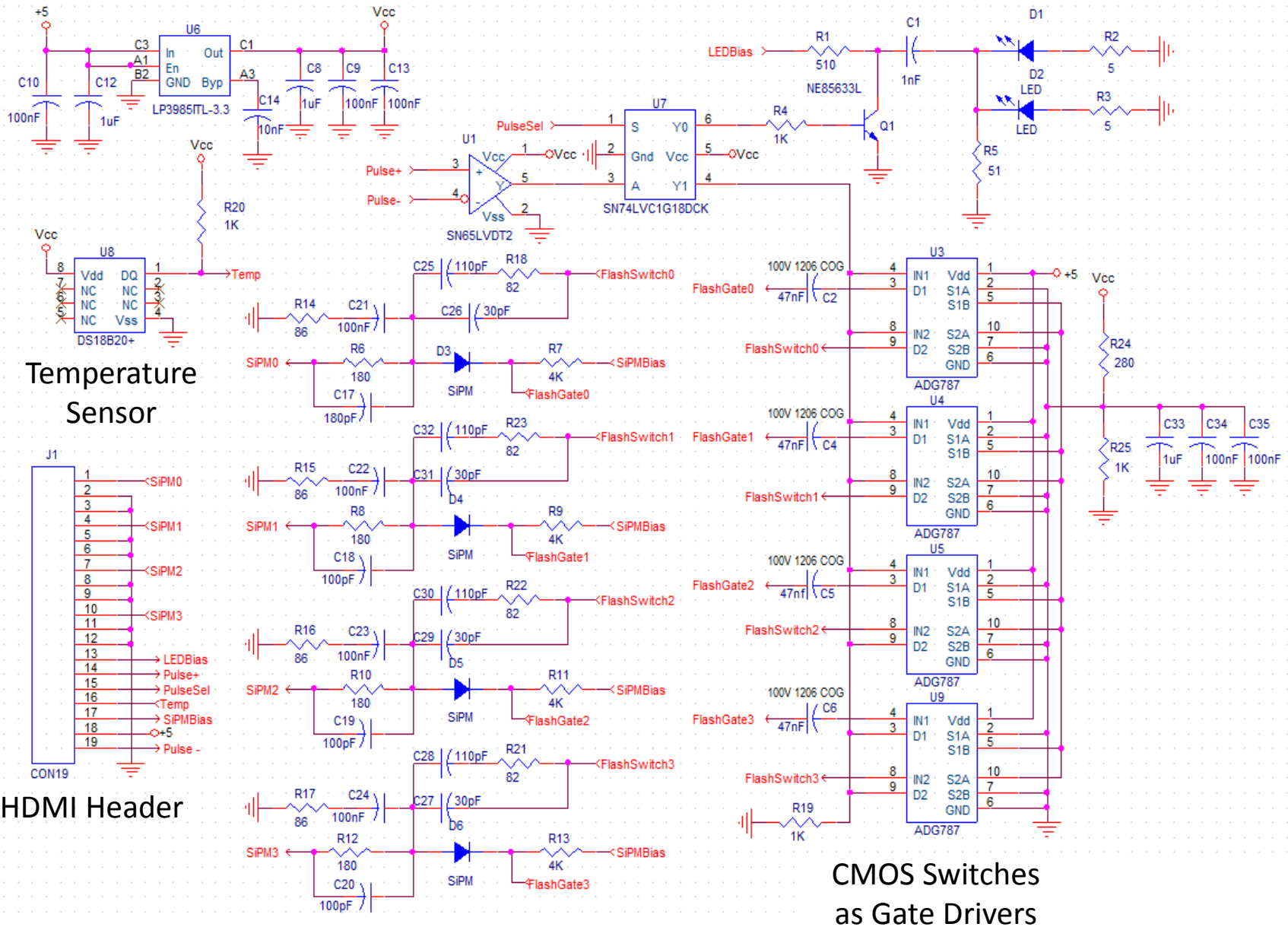


Fiber: 1, Side: 1





Electronics Mounted at the extrusion (CMB)



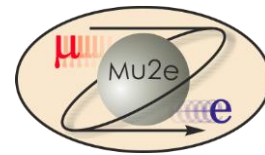
Temperature Sensor

HDMI Header

CMOS Switches as Gate Drivers



TI Ultrasound AFE chips



Compare Parts - Mozilla Firefox

www.ti.com/assets/js/compareParts/compare.html?familyId=2138&parts=AFE58JD18,AFE5809,AFE5803,AFE5807,AFE5808A,AFE5808,AFE5804&cols=o1,o4,p480,p84,p1568typ,p1006typ

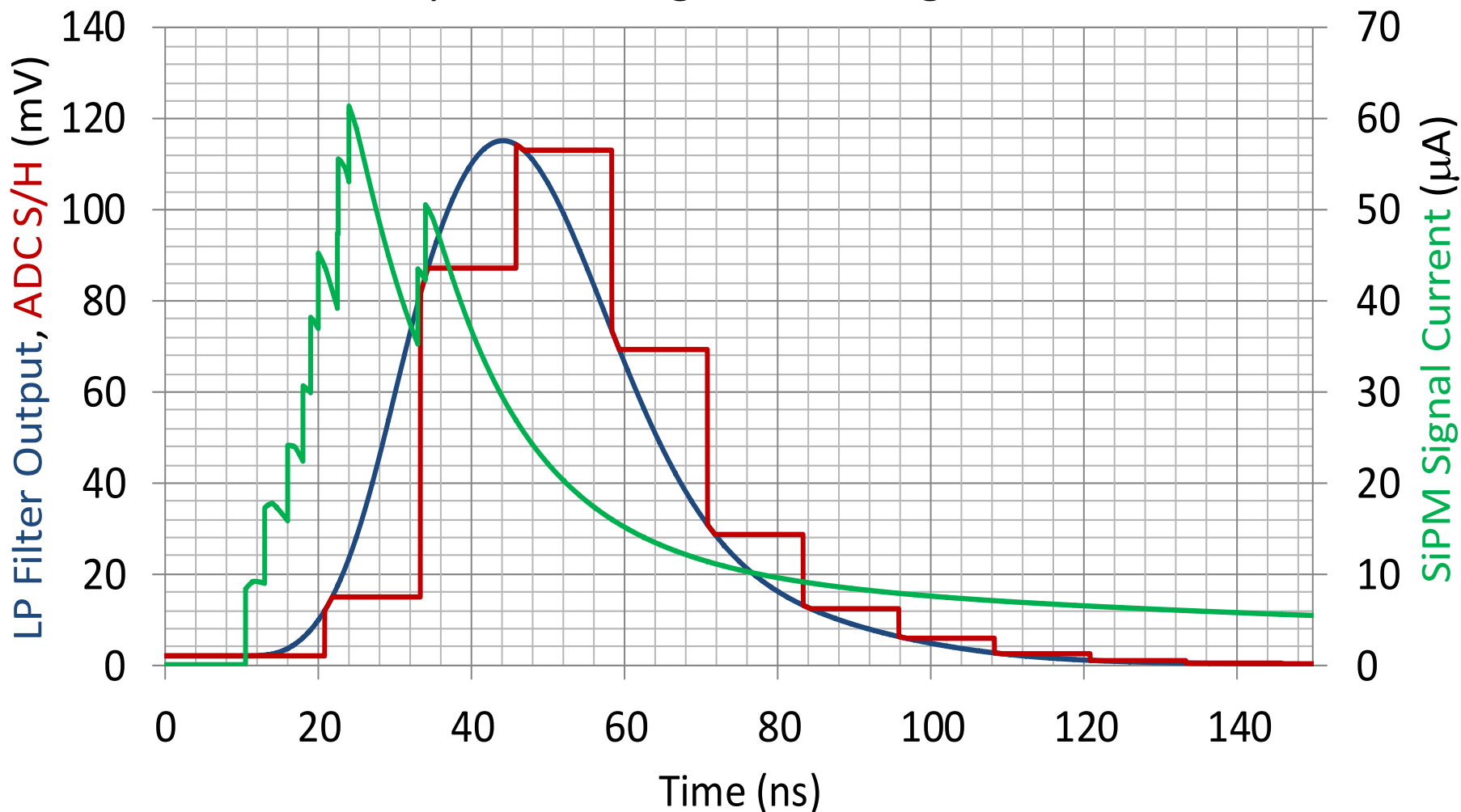
Compare Parts	AFE58JD18	AFE5809	AFE5803	AFE5807	AFE5808A	AFE5808	AFE5804
Number of Channels (#)	8	8	8	8	8	8	8
Resolution (Bits)	12 14	12 14	12 14	12 14	12 14	12 14	12
Input Voltage Noise (Typ) (nV/rtHz)	0.75	0.75	1.1	0.75	0.75	1.23	
Power/Channel (Typ) (mW)	158	158	97	158	149	101	
Gain Control Range (Typ) (dB)	40	40	40	40	40	46	
Input Range (Typ) (mVpp)	1000	1000	1000	1000	1000	280	
Total Max Gain (Typ) (dB)	54	54	54	54	54	49	
Gain Error (Typ) (dB)	+/-0.5	0.5	+/-0.5	+/-0.5	+/-0.5	+/-0.5	
HD2 Distortion (Typ) (dB)	-60	-60	-60	-60	-60	-65	
Overload Recovery (clock cycle)	1	1	1	1	1	1	
Function	Analog	Ultrasound Analog Front End with digital demodulator	Ultrasound Analog Front End	Ultrasound Analog Front End	Ultrasound Analog Front End	Ultrasound Analog Front End	Ultrasound Analog Front End



Design

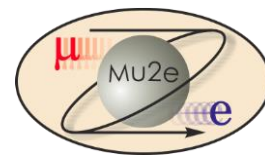


Simulation of an 11 p.e. SiPM signal showing tail cancellation:

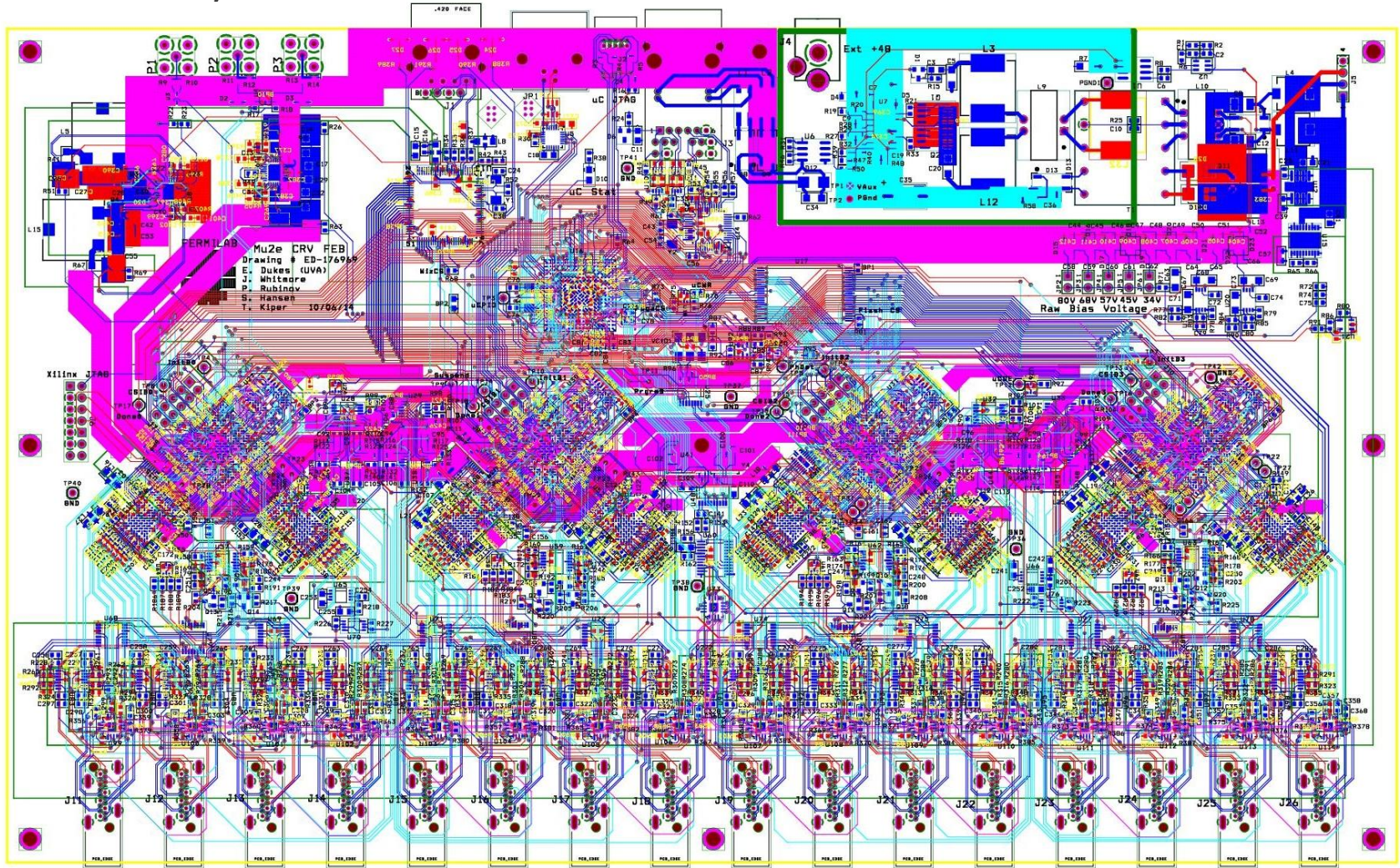




Design

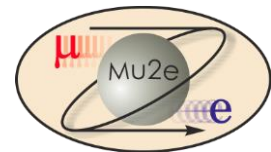


Plot of the FEB layout:

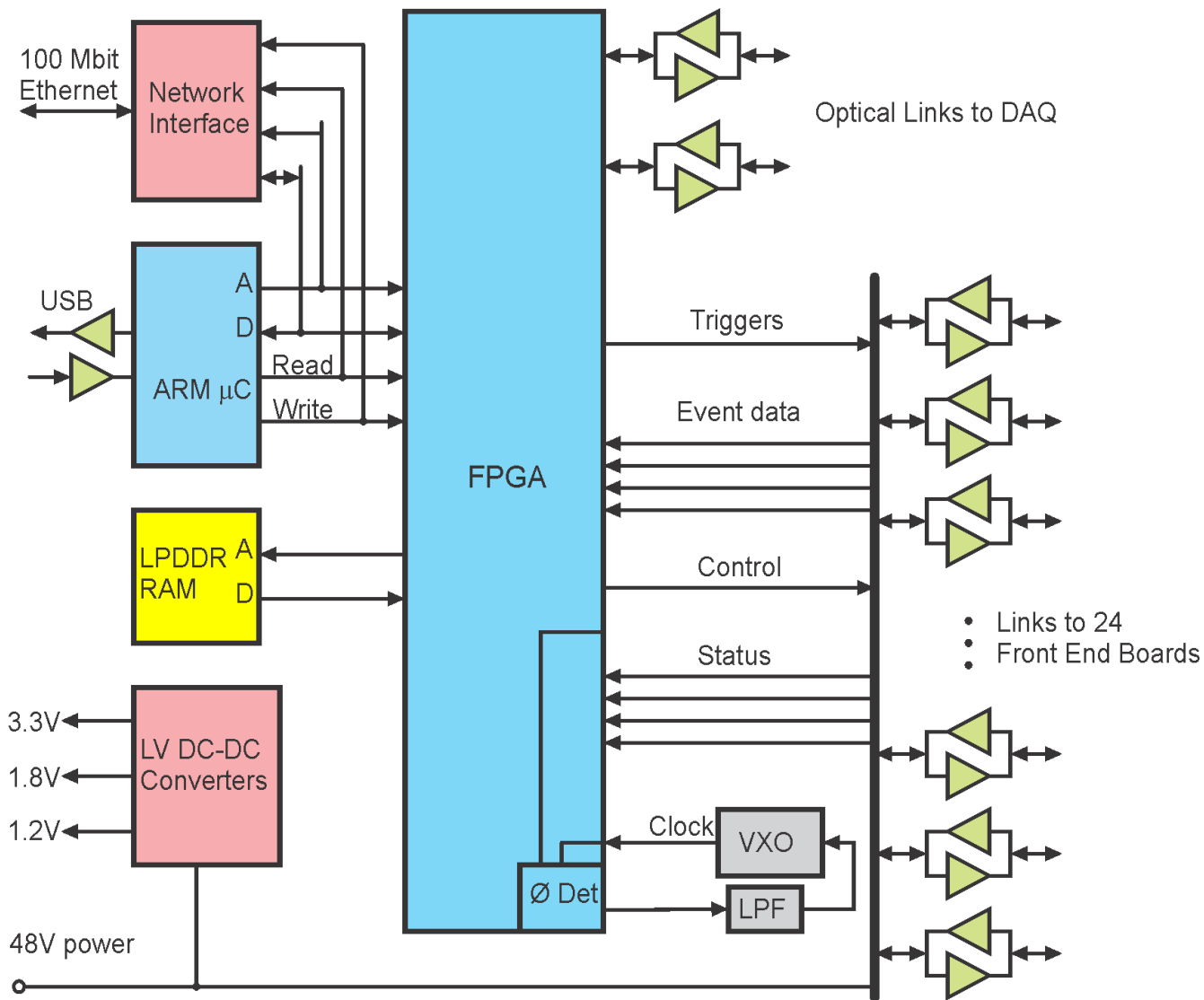




Design

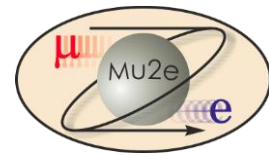


Controller
block diagram:





Design



Rate Estimates:

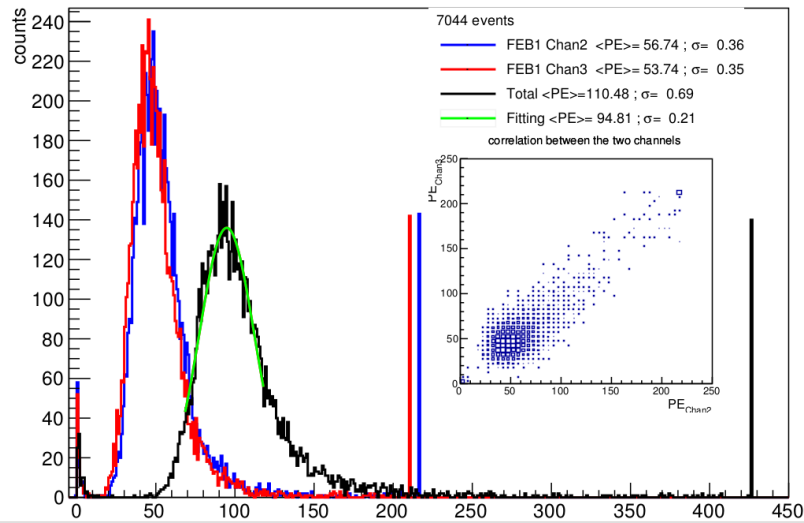
	Item	Average	Design
Live Spill Period	Instantaneous hit rate/channel	127.0 kHz	1000.0 kHz
	Hit event size	12 bytes	
	Instantaneous data rate/channel	1.5 MB/s	12.0 MB/s
	Spill length (s)	0.497	
	Spill duty factor	0.528	
	Average data rate/FEB	51.5 MB/s	405.7 MB/s
	Total data per FEB per live spill	25.6 MB	201.6 MB
Interspill Period	Instantaneous hit rate/channel	10.0 kHz	100.0 kHz
	Instantaneous data rate/channel	0.1 MB/s	1.2 MB/s
	Interspill length (s)	0.836	
	Interspill duty factor	1.000	
	Average data rate/FEB	7.7 MB/s	76.8 MB/s
	Total data per FEB per interspill	6.4 MB	64.2 MB
Total	Average data rate/FEB	24.0 MB/s	199.4 MB/s
	Average data rate/CRV	7.1 GB/s	59.0 GB/s
	Total data per FEB per cycle	32.0 MB	265.9 MB
	Total data CRV per cycle	9.5 GB	78.7 GB
FEB to DAQ	Trigger rejection		100
	Data rate out per FEB	0.2 MB/s	2.0 MB/s
	Average data rate to a ROC	5.8 MB/s	47.9 MB/s
	Total CRV data rate to DAQ	71.1 MB/s	590.2 MB/s
	Total CRV data for run	1.0 PB	8.0 PB

10 MB/s Links
FEB to Controller

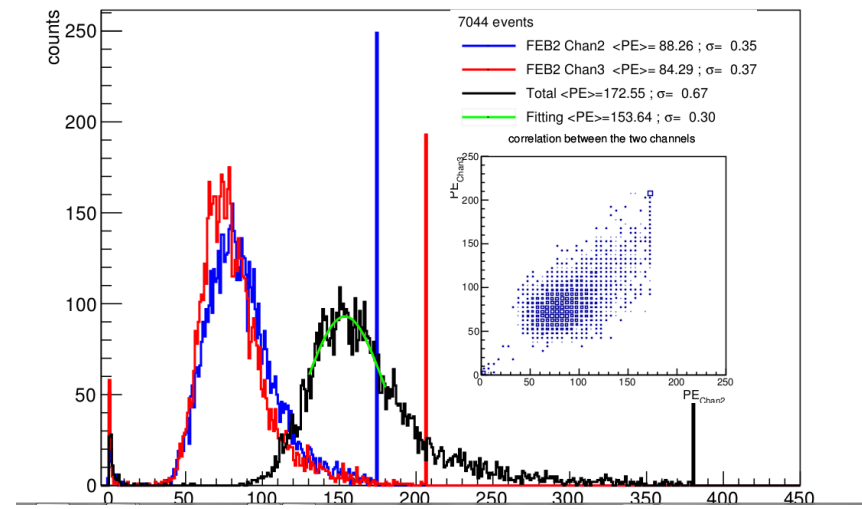
200 MB/s Links
Controller to DAQ

PE Yield

Run217 FEB1 PE Yield

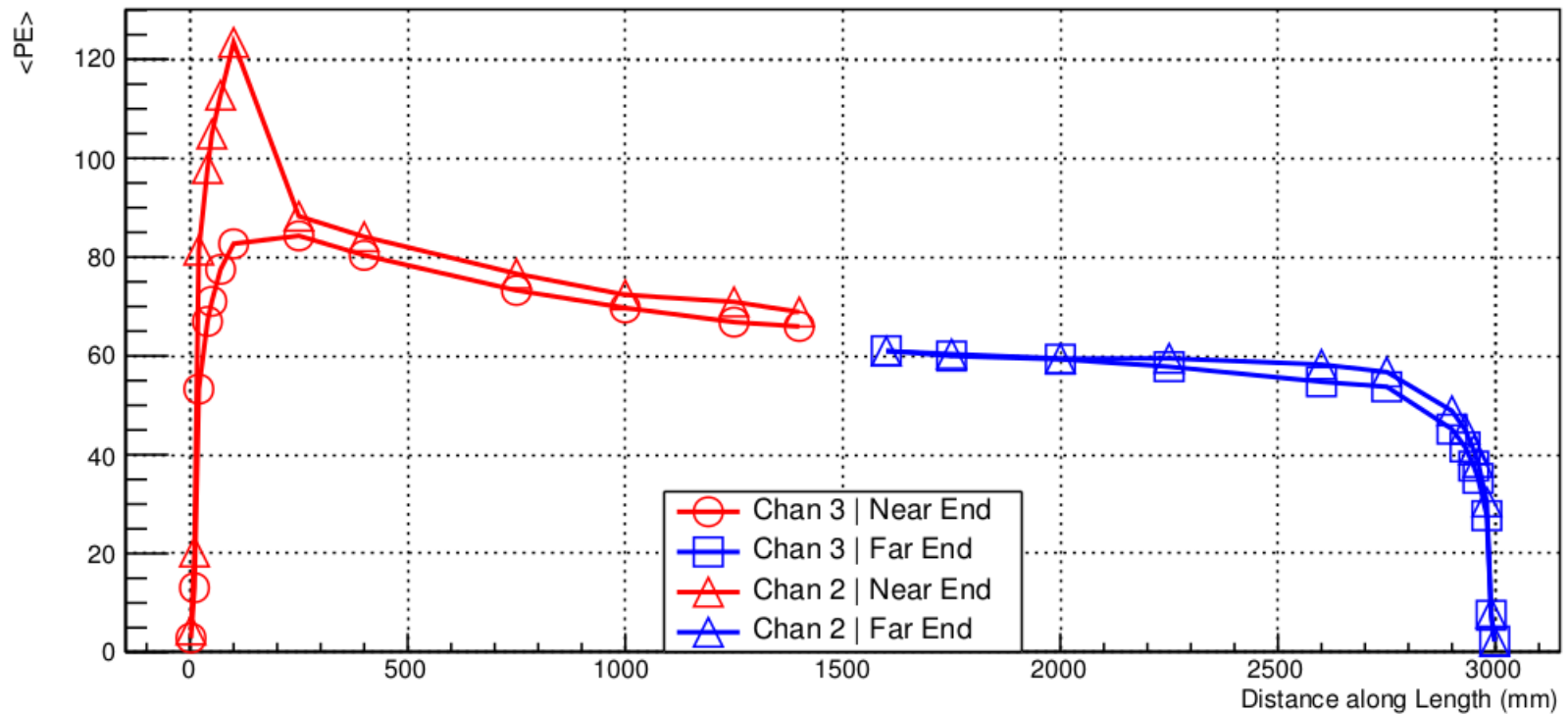


Run217 FEB2 PE Yield



Attenuation

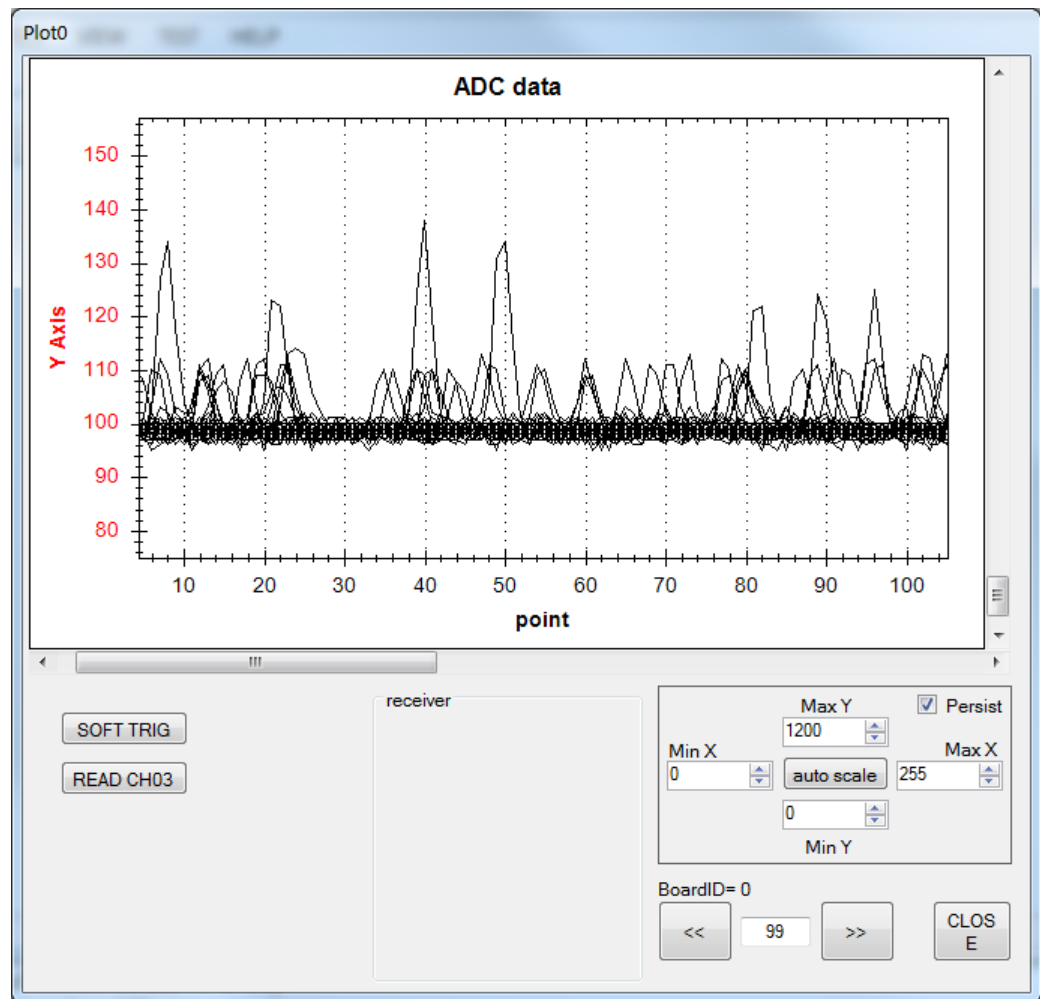
Attenuation along Length



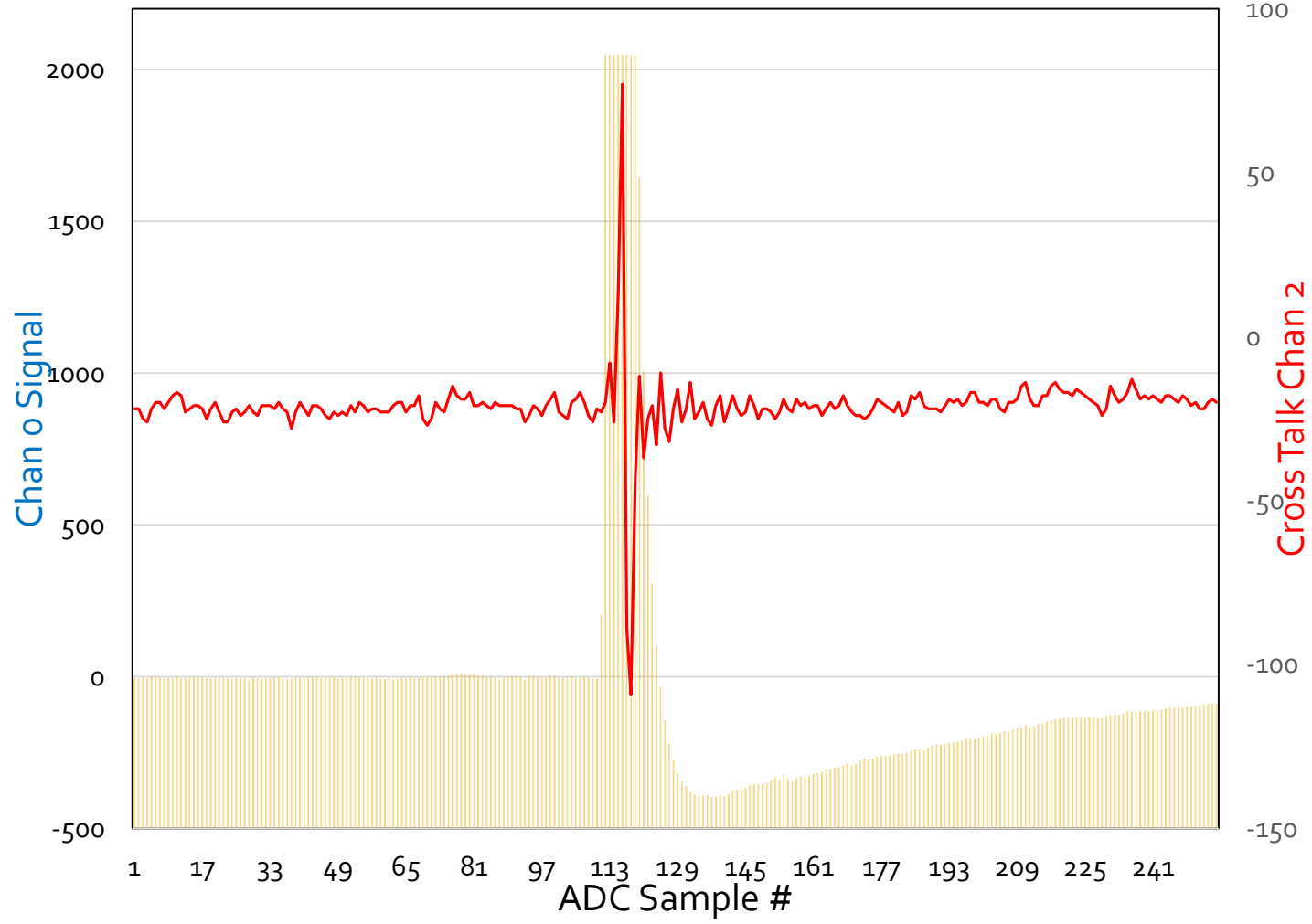
Dark rate is low,
but single PE very
clear

Single pe is $\cong 12$
counts

Single pe S/N $\cong 5$



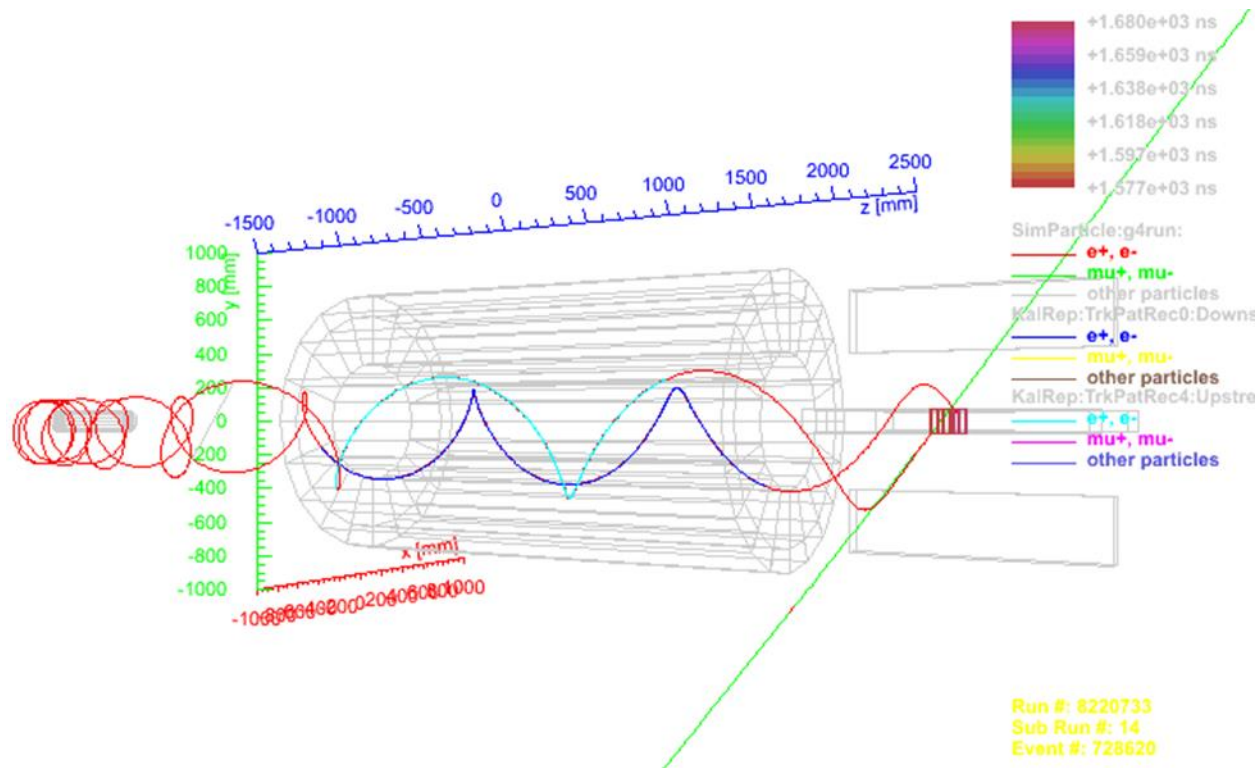
Cross Talk Trace



Tracking

Upstream Track Cuts:

- Many electrons are produced in the calorimeter and tracker, move upstream, and then back downstream
- Test for a segment consistent with an upstream-going electron, and reject it if that is the case



Boards will experience solenoid fringe field (400G max).

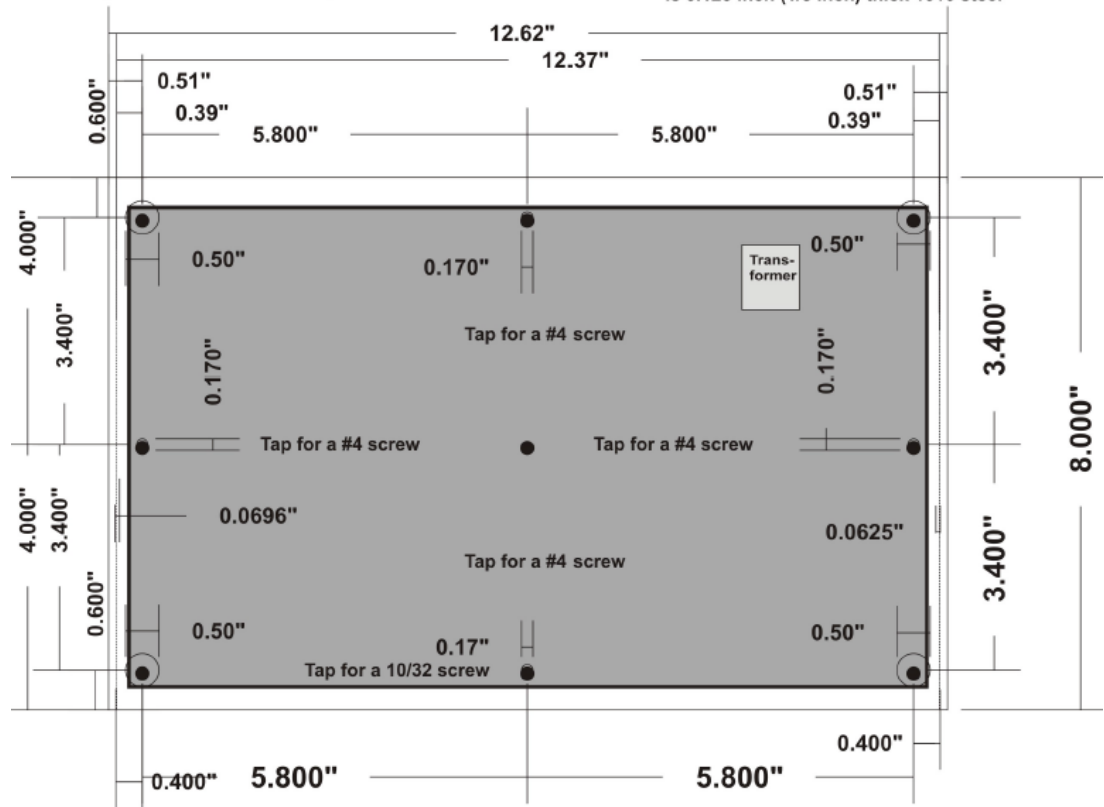
Merrill Jenkins mag shield design
Based on Mauricio Lopes field simulations.

Boards are mounting vertically.

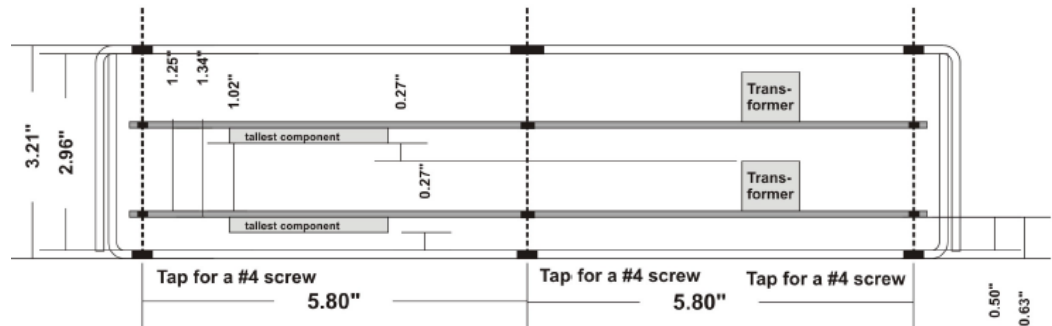
Cosmic Ray Veto Front End Board Magnetic Shields: Bottom Piece

Top View: Bottom piece (closest to enclosure)

Note: the material used for the shields is 0.125 inch (1/8 inch) thick 1010 steel



Side View: Top/Bottom piece



Requirements: Fundamental

- The requirements for the Cosmic Ray Veto are described in detail in Mu2e-doc-944.
- Fundamental (detector independent) requirements:
 1. To reduce the conversion-like electron background from cosmic rays to less than 0.10 events over the course of the run
 2. To provide a cosmic-ray trigger primitive to the DAQ
 3. Not to produce more than 10% dead time
 4. Not to use more than 20% of the DAQ bandwidth

Note: about 1 conversion-like electron per day is produced by cosmic-ray muons