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Implementation of the Timepix chip in the Scalable Readout System

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As proof of principle for a Pixel-TPC, the Timepix ASIC featuring a matrix of 256 x 256 charge sensitive pixels was chosen as anode readout of a gaseous detector. To read out more than a few chips, a new readout system was designed by developing dedicated hardware and FPGA firmware, on which the presentation will focus. The Scalable Readout System, as a general system also used for example in LHC experiments, was used for the implementation. In a test beam, 160 chips with about 10 mio. channels were read out in parallel - a new record for a TPC.

Summary

For the International Large Detector at the ILC, a Time Projection Chamber (TPC) is foreseen as main tracking device. Gas Electron Multipliers (GEM) or Micromegas are considered for the charge amplification of primary electrons from the ionisation of particle tracks. Besides the standard pad-based readout of the gaseous detectors, a new concept, the Pixel-TPC, is studied. As charge sensitive anode, ASICs are placed at the TPC endplate, resulting in a large number of channels and the need of a new readout system, which is modular and can be scaled from a single unit to a large detector. The Scalable Readout System(SRS) developed by the RD51 collaboration provides these features.
The Timepix ASIC, recently implemented in this system, is capable of measuring the arrival time of charge, which is necessary for a TPC. This chips contains 65536 charge sensitive pixels of 55 µm pitch on a active area of 2 cm^2, which allows to improve the pattern recognition and performance of the detector. The charge amplification is achieved by an integrated Micromegas on top of the chip, a so called InGrid. To increase the active area, many of theses chips have to be placed on the endplate.

For the SRS, a new FPGA firmware has been designed as well as electronics to connect the chips to the system. The capability of the setup was constantly increased from a single chip to octoboards and finally to an arbitrary number by taking advantage of the scalability.

The Timepix chip itself does not provide zero suppression. This feature has been implemented in the firmware to decrease the amount of data to be transmitted through Gigabit Ethernet to the data acquisition computer. Together with some multi-threading techniques, the maximum theoretical readout rate, only limited by the ASIC, was achieved. Another feature of the designed hardware, together with the slow control software is, that it provides an automated calibration procedure for the Timepix chips.

Particular care has been taken to suit the special demands in a particle detector environment concerning the presence of strong magnetic fields and noise on the data and slow control cables.
To demonstrate the feasibility of a Pixel-TPC as well as the readout, a testbeam was carried out at the Large Prototype of the LCTPC Collaboration at DESY in March/April 2015. Three endplate modules of the TPC were equipped with a total of 160 chips, which amounted to 10.5 million channels on a active area of 320 cm^2. Tracks from 5 GeV electrons were recorded in a magnetic field of 1 T.
The presentation will mainly focus on the SRS-based Timepix readout system and the hardware to operate the chips. But also some preliminary results from the successful test beam will be shown.

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