TWEPP 2015

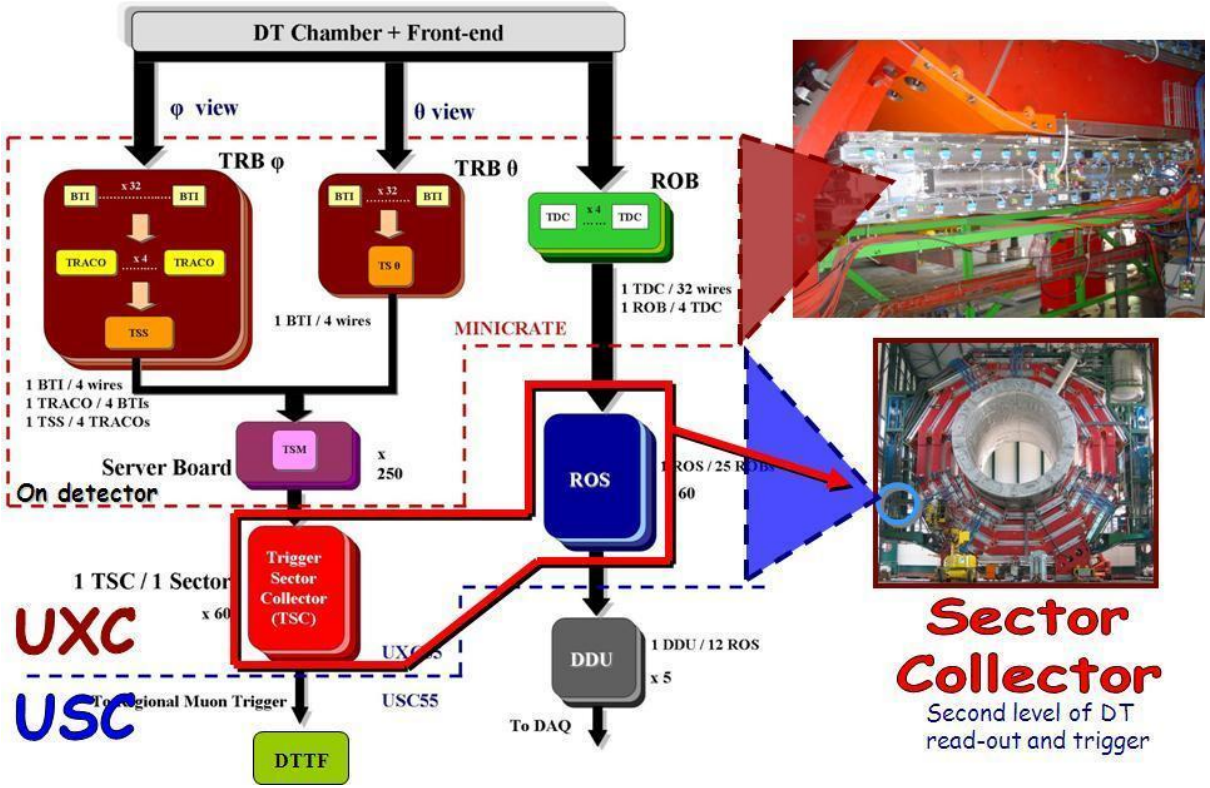
Lisbon, 28/9-2/10

CMS DT Upgrade: The Sector Collector Relocation

Álvaro Navarro-Tobar

on behalf of the CMS Collaboration

The CMS Drift Tubes electronics before LS1 upgrade



The sector collector is a complex electronics system located in UXC:

- 10 crates, 60 ROS boards, 60 TSC boards, + timing and VME interface boards

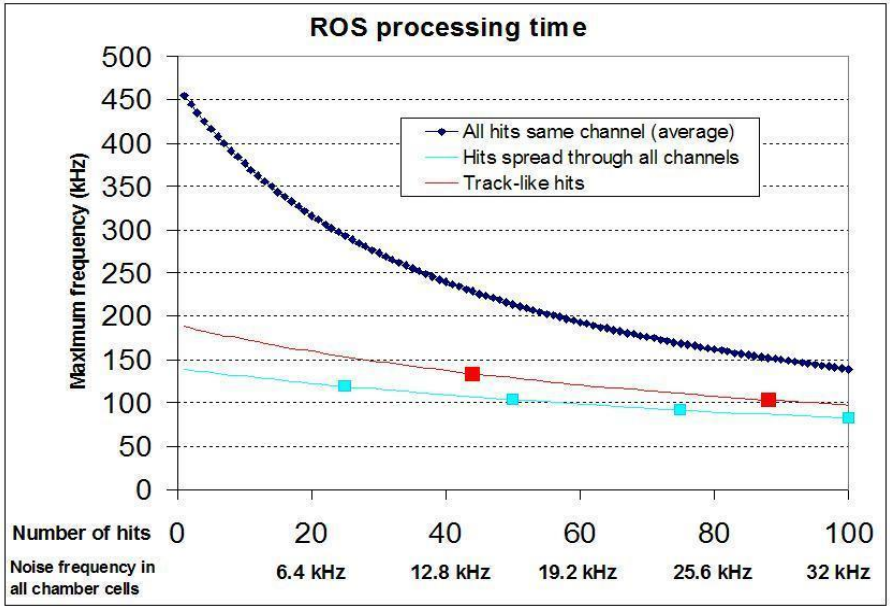
Carries out a concentration task over the multiple input links from the minicrates:

- Readout (ROS): data merging & data quality monitoring
- Trigger (TSC): multiplexing and sorting trigger data

Motivation for the relocation

Reliability

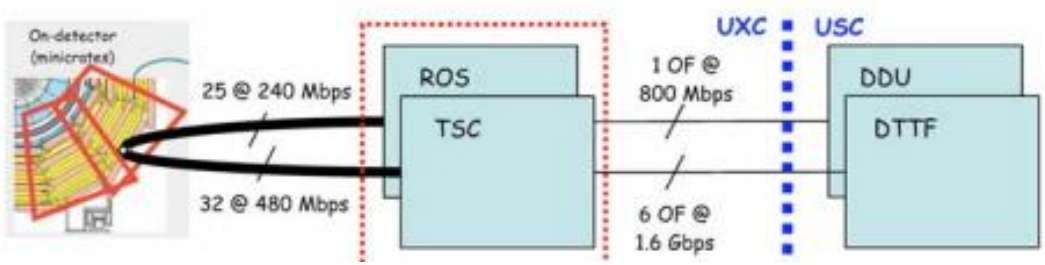
- UXC is an aggressive environment: radiation, magnetic field
- Failures compromised large fractions of the detector (up to 10 % in case one board fails) and cannot be solved for weeks



Performance

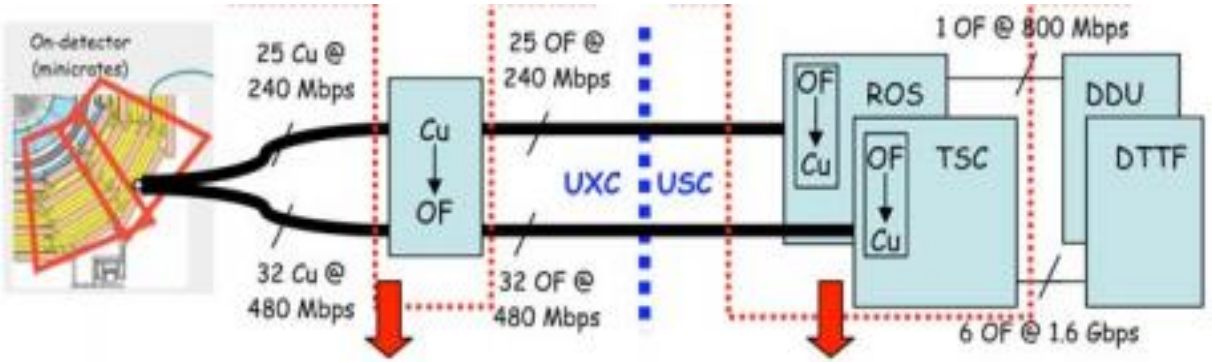
- CMS' L1 trigger system is upgrading to µTCA to allow handling of higher luminosity and early merging of RPC, DT and HO
- ROS board becomes a bottleneck for readout at increased luminosity conditions in Phase 1
- Moving to USC will allow for looser design constraints (power, magnetic and radiation tolerance) and higher performance

Relocation overview



Previous system

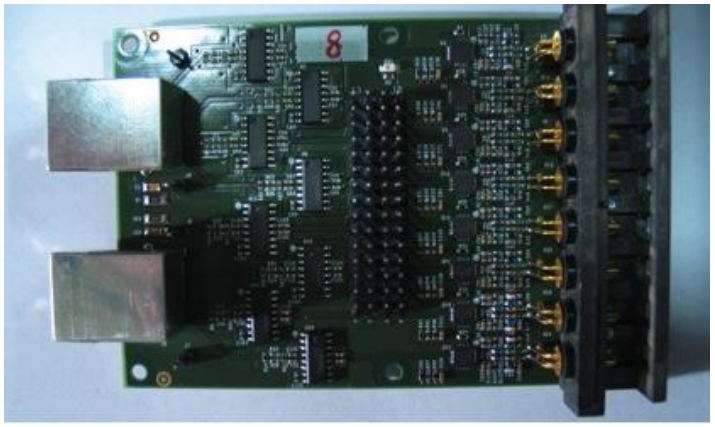
SC Relocation

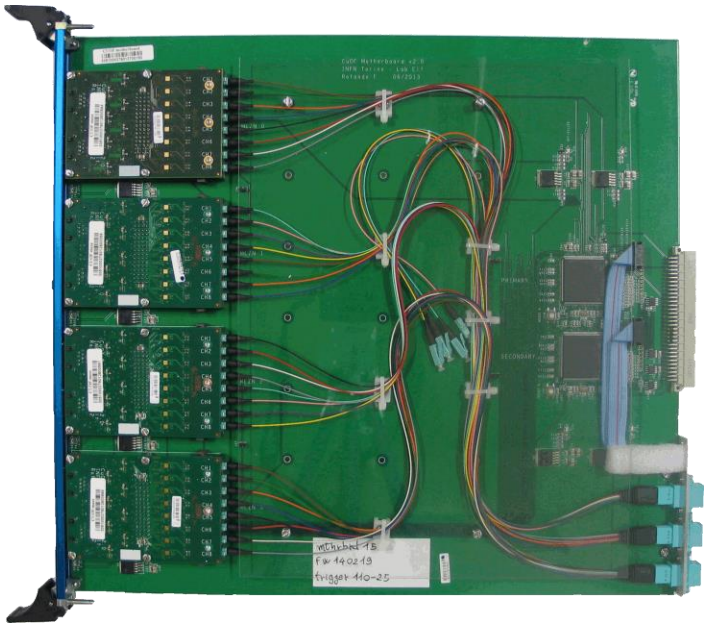


- 1 to 1 pseudo-analog electrical to optical conversion
- Distance from minicrates grows by ~60 m: data links are converted to optical and back (3500 optical links)
- UXC system (CuOF) kept simple to improve robustness

UXC: CuOF board

- Motherboard + 4 mezzanines (optical conversion)
- Mezzanines: 8x {equalizer + laser driver + laser}
- Motherboard does ADC monitoring and bias control: FPGA + CAN bus
- Optical output is organized into MTP connectors by means of MTP to 12xLC fan-out cables
- Due to trigger signal's DC-unbalance it is necessary to fine-tune laser's bias and modulation to optimize transmission quality
- Completely redundant slow control (FPGA, CAN, OCB, ECB)
- Power consumption has been reduced to ~ 50% of the SC; power distribution partitioned for robustness





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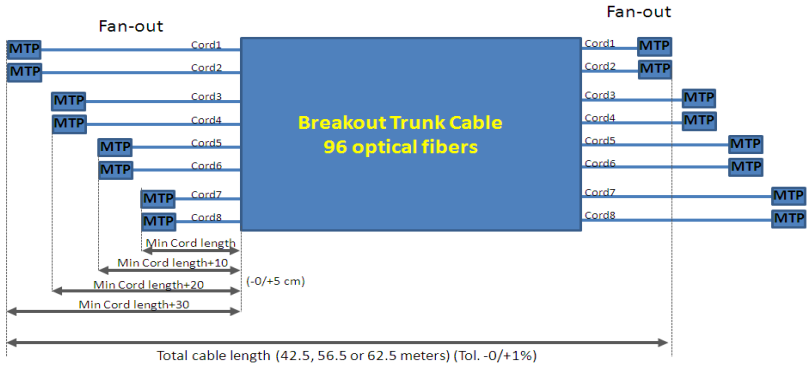
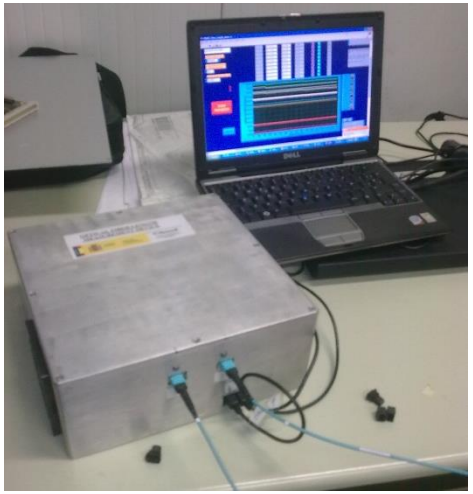
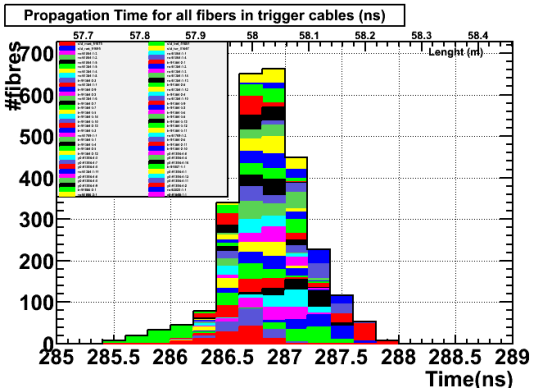
Optical fibres & validation

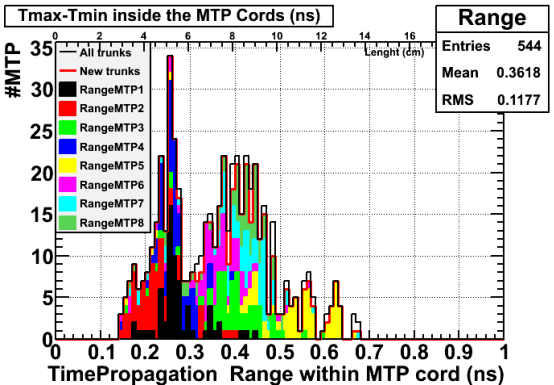
- 3500 links, OM3 50/125 µm 850 nm fibres up to 10 Gbps
- 60 trunk cables, each 96 fibres (5760 in total), terminated in 8 12-fibre cords with MTP connectors (staggered to minimize needed diameter)

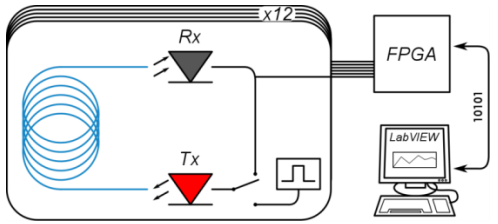


- Propagation delay uniformity is critical to preserve phase relationship among trigger links → ~6000 links measured
- A low-cost, high-precision system for validation: transit-time oscillation method (self-sustained oscillation generated in a closed loop, and its period is measured by a FPGA and LabView)
- Delay uniformity was excellent, inter-cable differences below 2.5 ns, same-MTP differences under 1 ns









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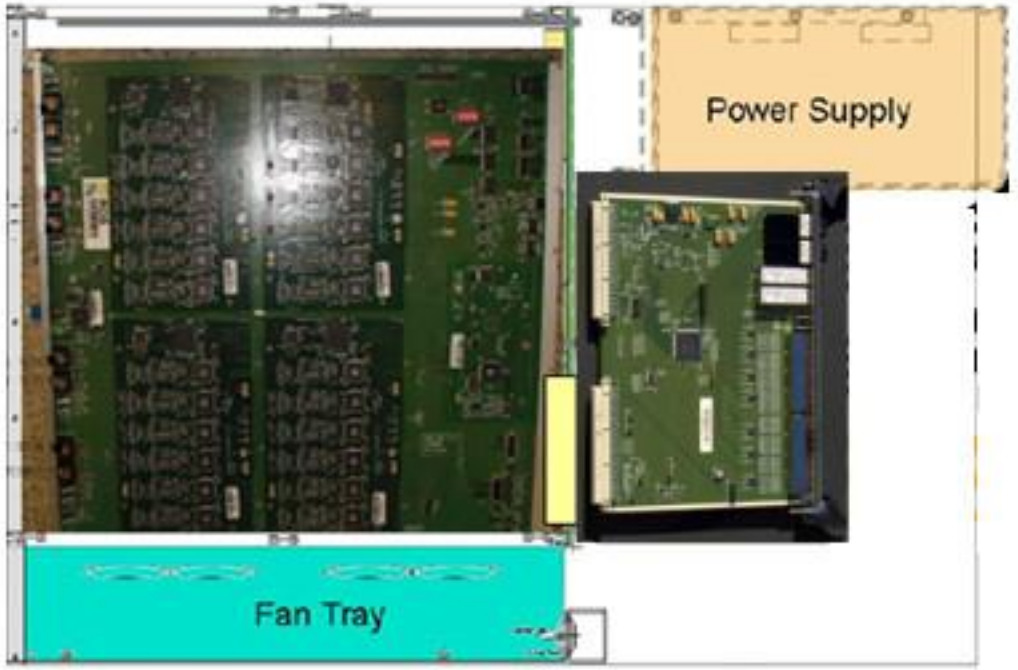
USC: OFCu system overview

- Main goal: convert back to electrical (LVDS) to keep legacy electronics without modification

- But… TRG and RO crates are now separated (due to space availability and to minimize latency) → TRG-RO backplane communication impossible
  → Additional optical "TSC link" between crates. TSC/ROS communicate with Rear Transition Module **(RTM)** boards by pass-through backplane connectors

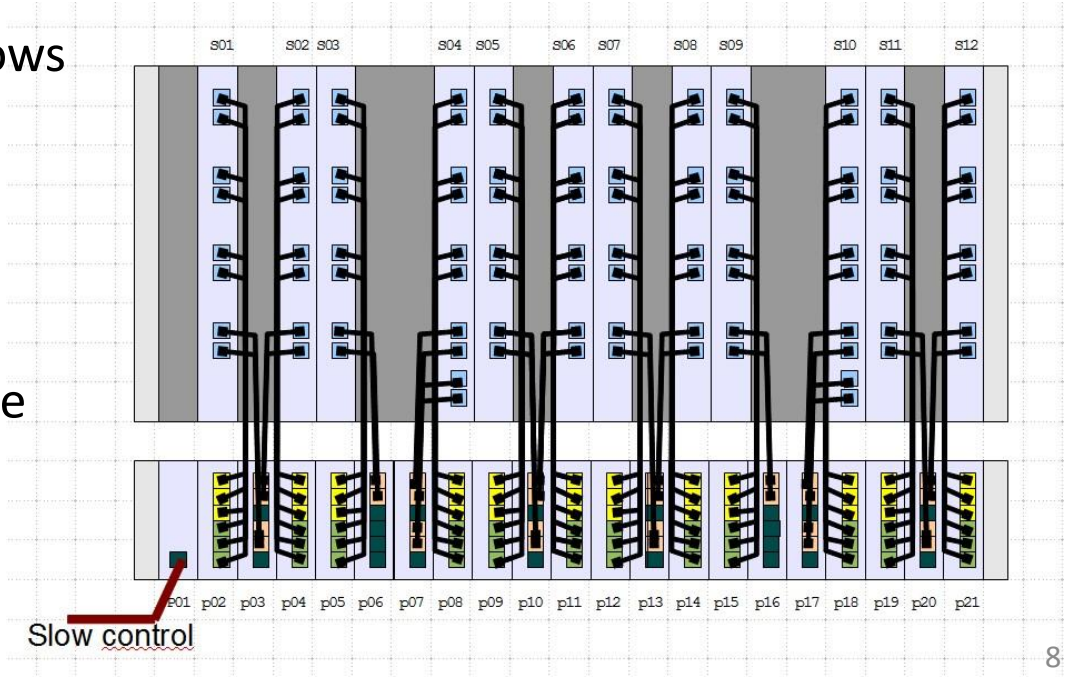
- New Wiener crates host:
  - 12 9U boards (ROS/TSC)
  - Their respective RTMs
  - TIM (TTC distribution)
  - Linco VME interface
  - VMEpatch board

- VMEpatch board developed to allow slow control communication to the RTM modules through the VME link (custom protocol). It also interfaces to external OFCU-TRG system through I2C lines for slow control



Trigger OFCu

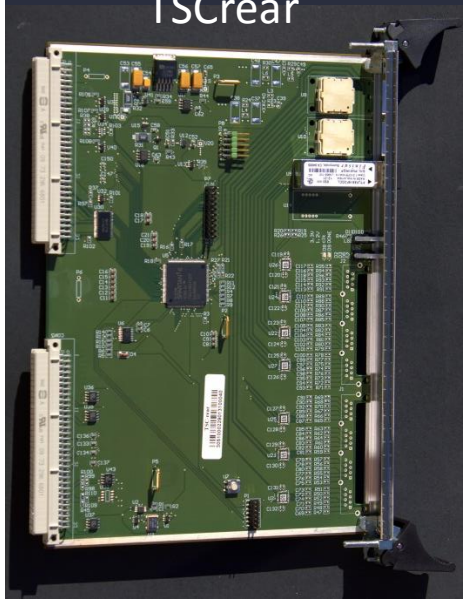
- The OFCU-TRG is a 3U board which converts 24 links from optical (2xMTP rear connectors) to LVDS (6xRJ45 front connectors)
- Based on CotS parallel optics receiver from AVAGO
- Signal path is clean, parallel and free of skew between channels.
- Rear-front configuration allows easy cable routing
- Standalone operation (or almost)
- Boards connect to a narrow backplane on the optical side for monitoring and power



Readout OFCu & TSC link

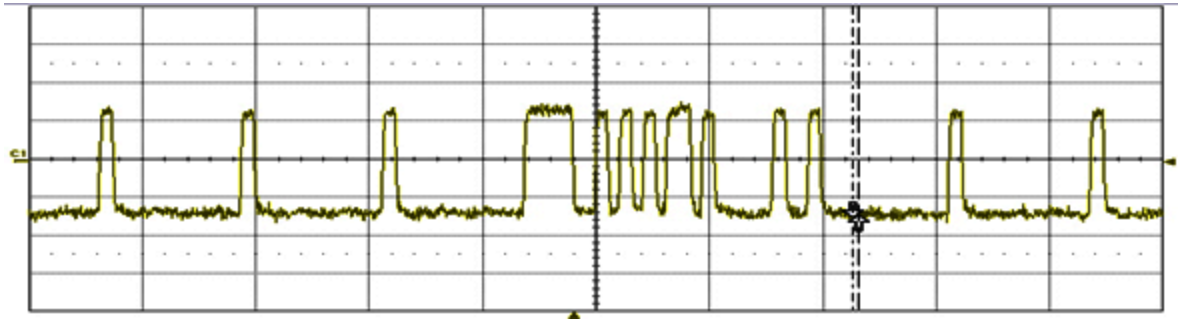
- Converts the 25 optical links into LVDS signals for each ROS using also an AVAGO receiver
- Semi-autonomous operation; no skew requirements to met in readout
- LVDS signals are carried by FTP cables from the OFCu boards on the back to the ROS RJ45 connectors on the front
- TSCrear/OFCu-RO transmit the TRG debug data that was exchanged through the backplane for inclusion in readout stream
- TSCrear receives trigger data from a TSC, and sends it over an 800 Mbps optical serial link to the OFCu-RO
- The OFCu-RO receives the data, makes some quality checks, and delivers it to the ROS
- The operation is transparent to the TSC/ROS boards

OFCu-RO



TSCrear

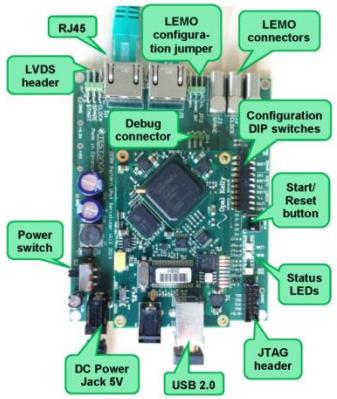
System validation

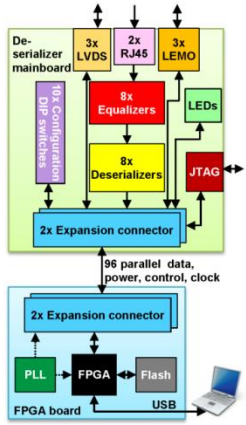


- System validation critical due to the high reliability needed
- Most relevant problem related to the severe unbalance of the 480 Mbps trigger links: 8 % duty cycle during idle
- Readout links are 240 Mbps and 42 % duty cycle during idle
- Important to fine-tune the bias and modulation current of the selected laser driver to pair it with the receiver (several driver/laser/receiver combinations were evaluated)

System validation

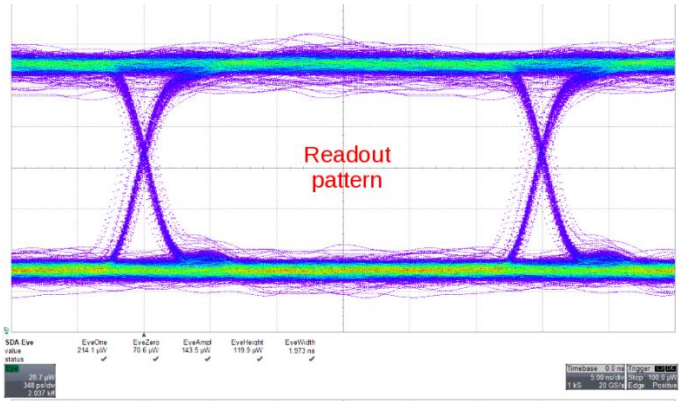
- Custom versatile Pattern Unit boards (both tx/rx) were made to simulate the output of a minicrate and receive and verify the data at the other end

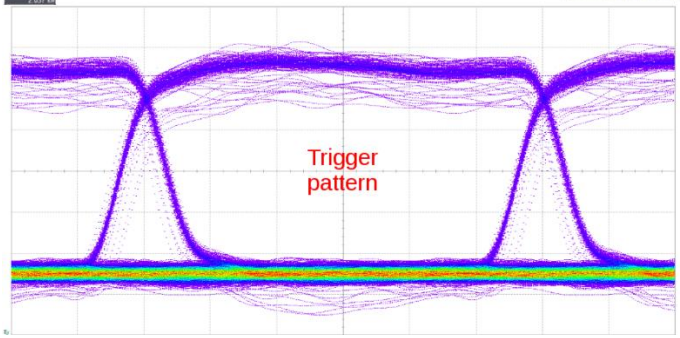




- Eye diagrams of the CuOF were taken with PRBS, trigger-like and readout-like patterns

- The CuOF was subject to 2 irradiation tests at CERN's H4IRRAD facility, with conditions equivalent to 10 years of HL-LHC operation, in order to validate the prototype. No variation of optical power detected, and BER and SEU rate were found acceptable

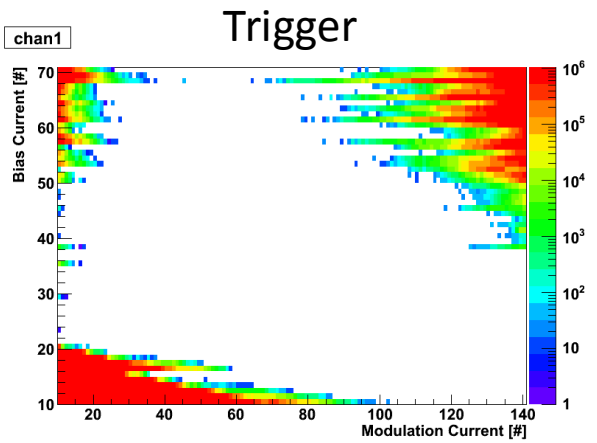


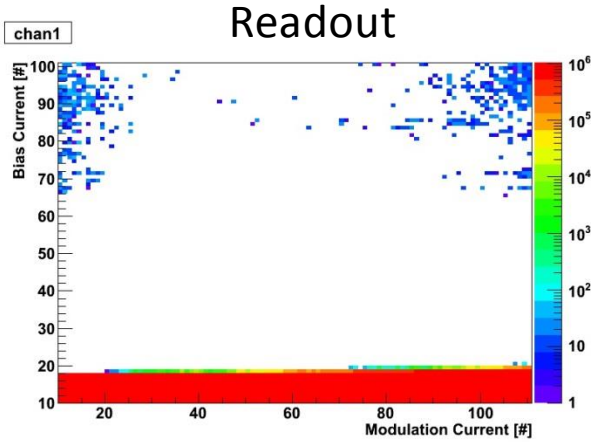


- Full-chain tests with magnetic field were carried out at CMS in 2012-2013

System validation

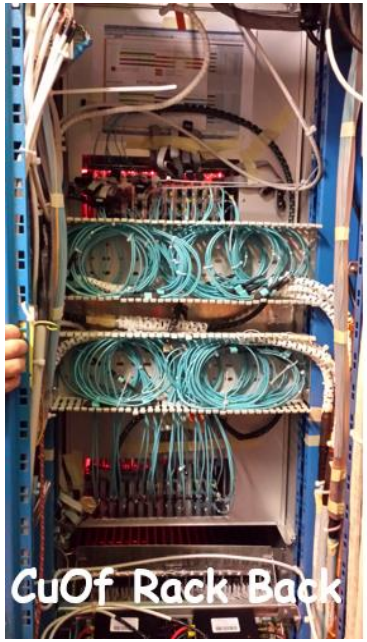
- A power dissipation test was done with two crates full of mockup boards (and a real CuOF) inside a LHC rack
- Accelerated aging test was done in a climatic chamber: 1000 hours @70 ºC, 70 % RH
- QC included tests to the mezzanines, motherboards and complete system
- Mezzanines underwent a "Scan Test" in which the BER is characterized for all bias and modulation currents with a trigger-like pattern (more unbanlanced so more sensitive)
- Motherboards underwent a CAN bus communication test and ADC test with mockup mezzanines
- The full CuOF board underwent again a Scan Test

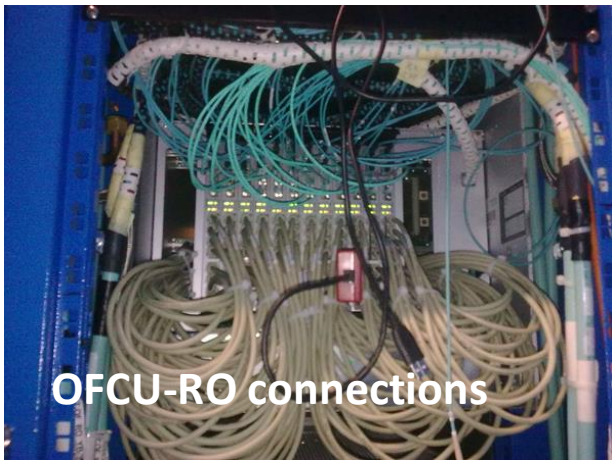




Installation & commissioning

The complete installation took place during LS1, between 2/2013 and 8/2014. It consisted in several sub-tasks (fibre laying, LVDS cables rearrangement, racks and crates refurbishment, new crates installation, etc.), highly inter-dependent, which also had to be coordinated with the detector maintenance activities





Commissioning was done after each wheel's relocation with cosmic rays and testpulse runs. As expected, latency increased by +3 BX.

Conclusions

- The Sector Collector relocation was completed in time for the 2015 data taking and is performing satisfactorily
- It significantly increases the reliability of the old Sector Collector electronics, by making the poorly-accesible electronics more simple, robust and redundant, and improving the accessibility of the data-processing electronic systems
- It allows to carry out further upgrade projects (which are already under way), placing it in an easily accessible area, with looser environmental constraints

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Backup Slides

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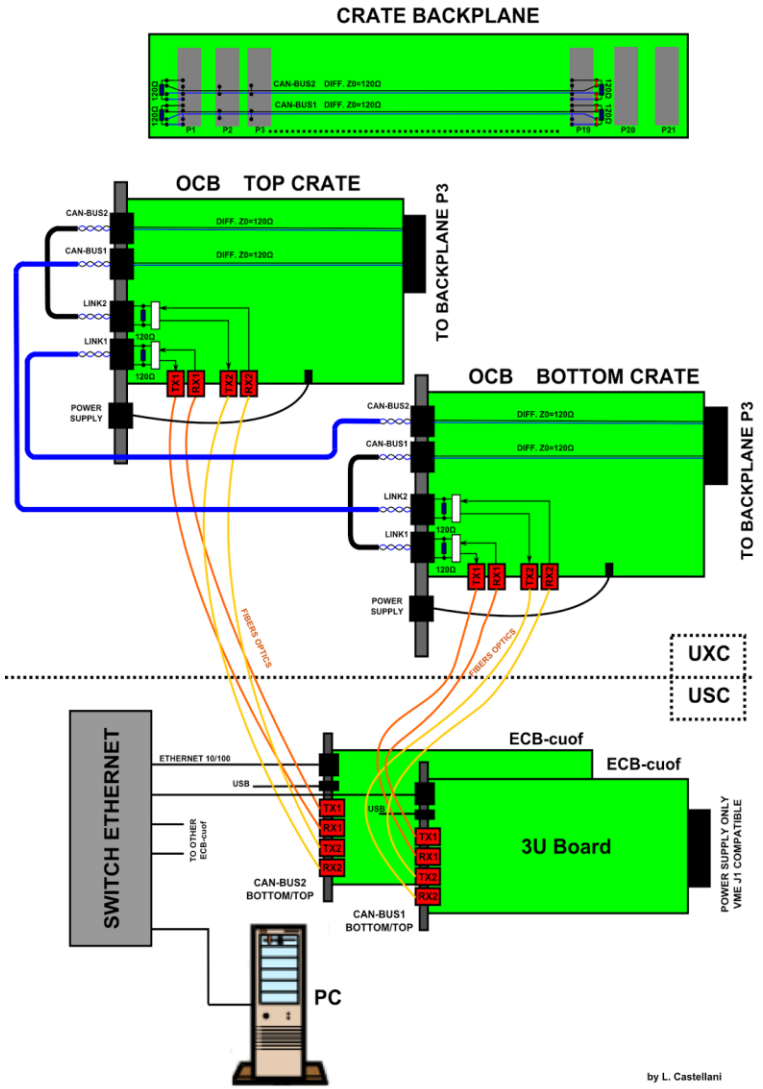
on behalf of the CMS Collaboration

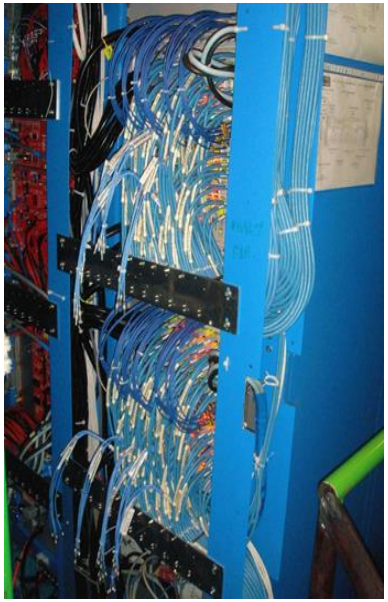
CuOF power and slow control

- Both CANbus lines are routed by the backplane to the OCB boards, which translate the signals to optical links arriving to USC
- ECB boards bridge CAN signals to Ethernet network
- Both ECB boards (2/wheel) can access CAN buses in both wheel crates, resulting in a highly redundant and robust system

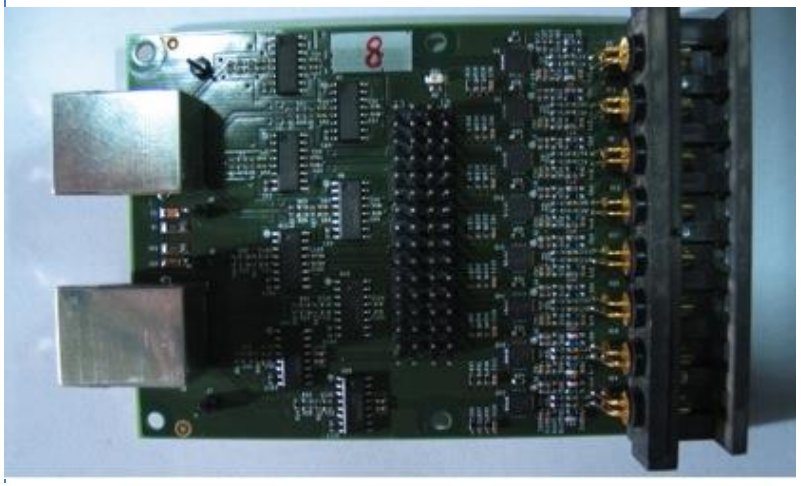
- The A3100 DC-DC modules that powered the SC were refurbished to A3050 dual-channel modules.
- Each crate has 4 power partitions to minimize the effect of a failure
- The crates were adapted to the new configuration
- Power consumption has been reduced to ~ 50% of the SC

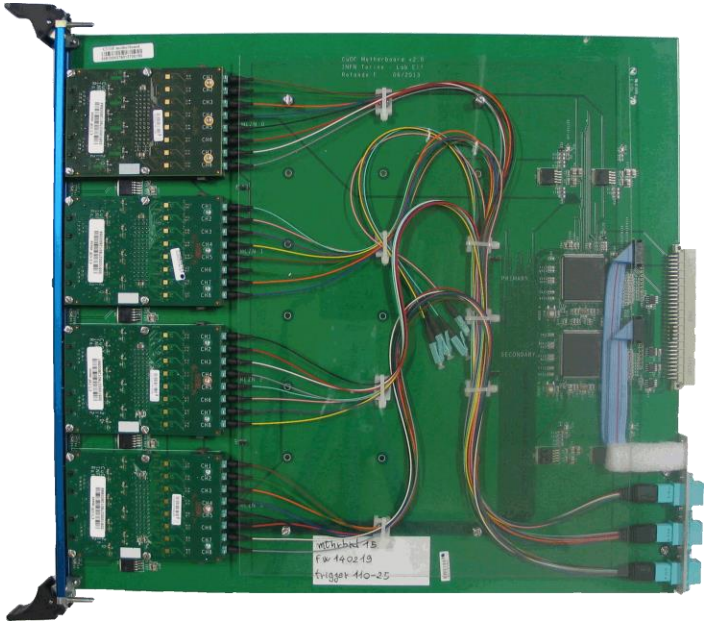


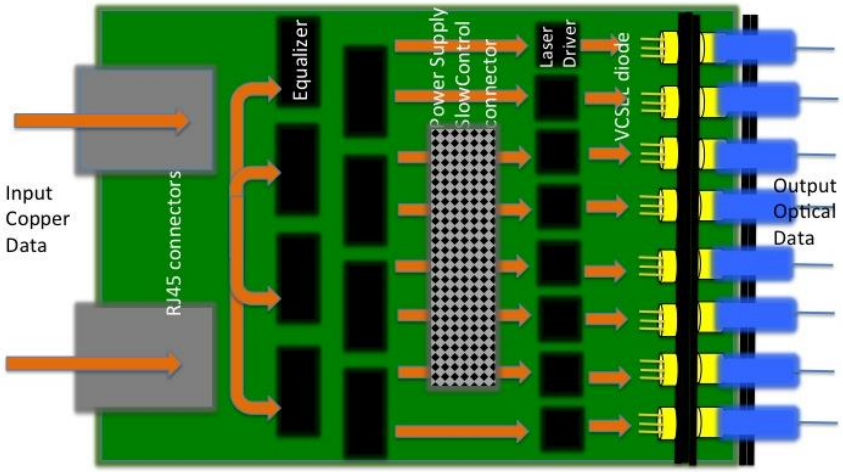
Pre-upgrade SC

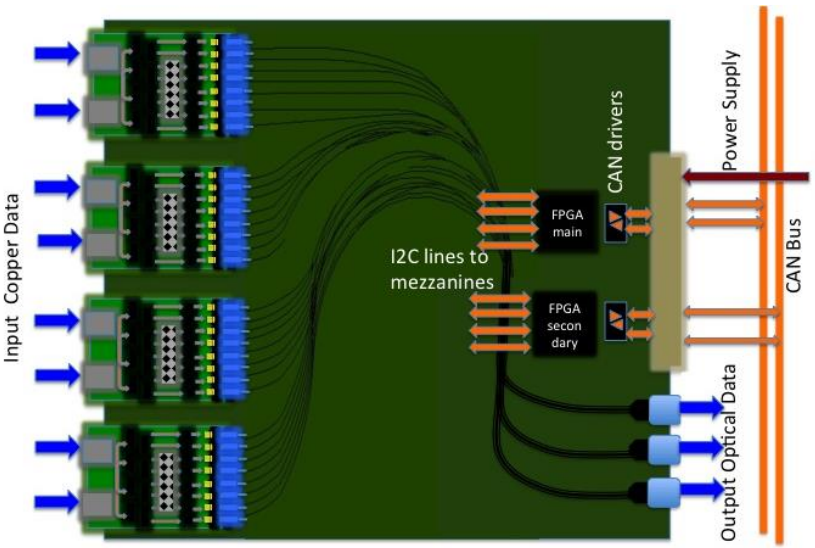


CuOF photos

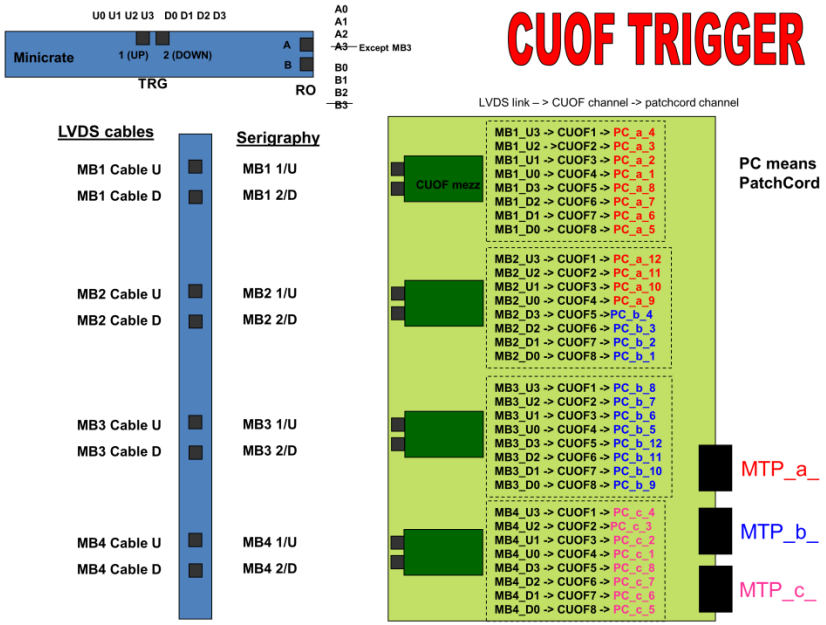


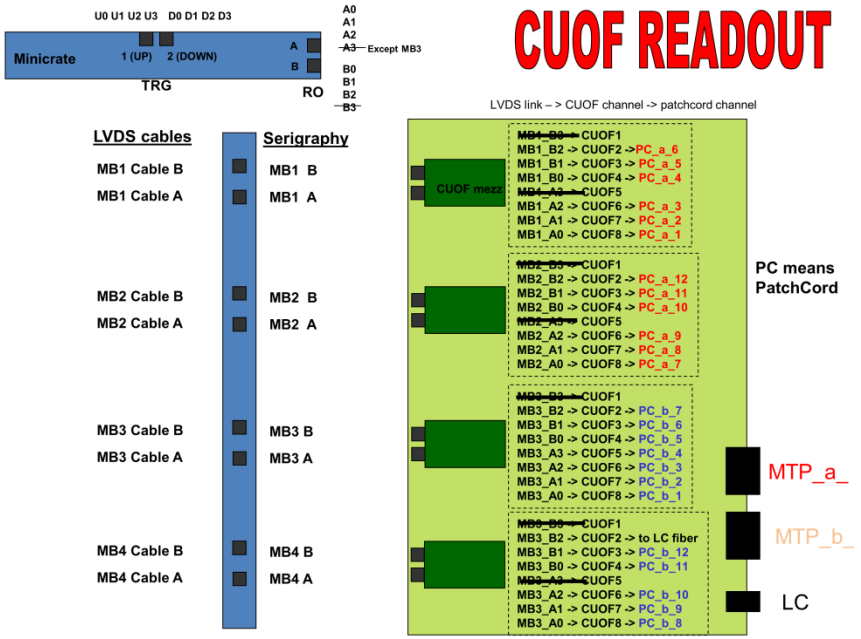



Input
Copper
Data
RJ45 connectors
Equalizer
Power Supply
SlowControl
connector
Laser
Driver
VCSEL diode
Output
Optical
Data


Input Copper Data
I2C lines to
mezzanines
FPGA
main
FPGA
secon
dary
CAN drivers
Power Supply
CAN Bus
Output Optical Data

CuOF fibre mapping





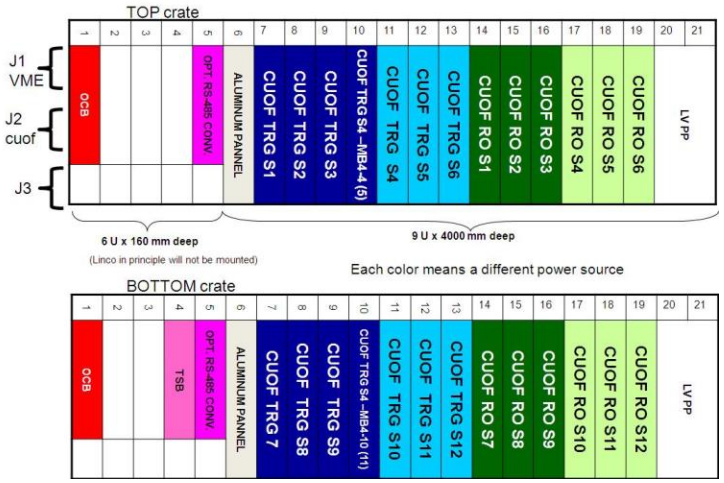
TOP CRATE

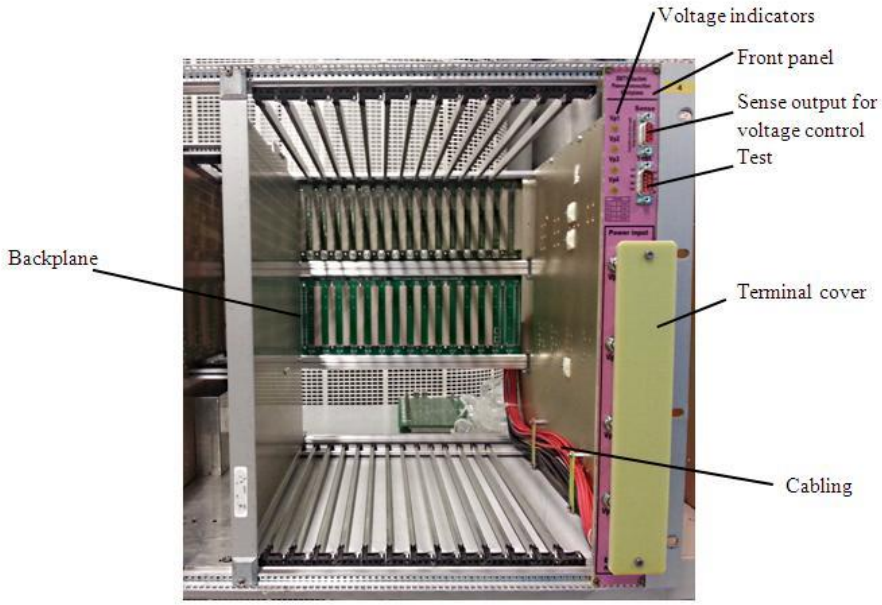
19	18	17	16	15	14	13	12	11	10	9	8	7
RO-S6	RO-S5	RO-S4	RO-S3	RO-S2	RO-S1	TRG-S6	TRG-S5	TRG-S4	TRG-S4BIS	TRG-S3	TRG-S2	TRG-S1
LC-6	LC-5	LC-4	LC-3	LC-2	LC-1							
						MTP-4	MTP-1	MTP-4	MTP-7	MTP-1	MTP-4	MTP-1
MTP-5	MTP-3	MTP-1	MTP-5	MTP-3	MTP-1	MTP-5	MTP-2	MTP-5		MTP-2	MTP-5	MTP-2
MTP-6	MTP-4	MTP-2	MTP-6	MTP-4	MTP-2	MTP-6	MTP-3	MTP-6		MTP-3	MTP-6	MTP-3

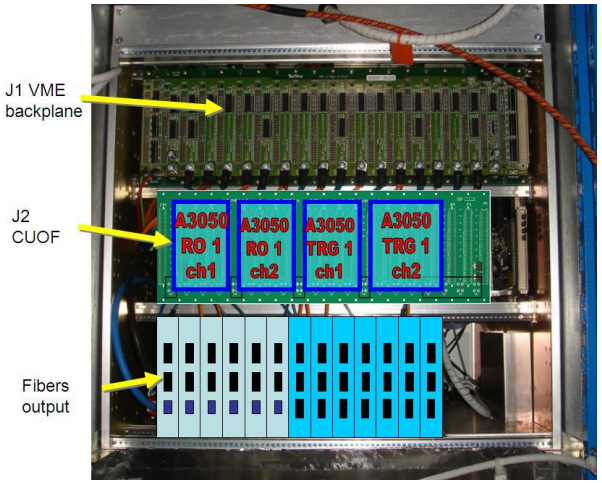
BOTTOM CRATE

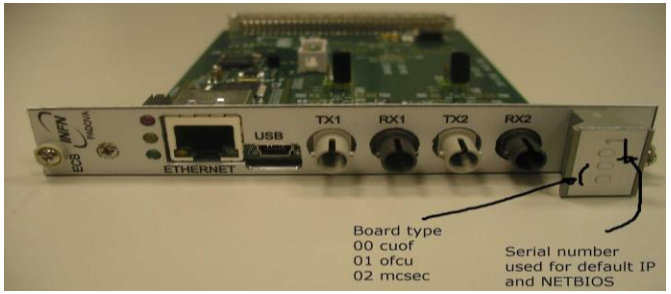
19	18	17	16	15	14	13	12	11	10	9	8	7
RO-S12	RO-S11	RO-S10	RO-S9	RO-S8	RO-S7	TRG-S12	TRG-S11	TRG-S10	TRG-S10bis	TRG-S9	TRG-S8	TRG-S7
LC-12	LC-11	LC-10	LC-9	LC-8	LC-7							
						MTP-4	MTP-1	MTP-4	MTP-7	MTP-1	MTP-4	MTP-1
MTP-5	MTP-3	MTP-1	MTP-5	MTP-3	MTP-1	MTP-5	MTP-2	MTP-5		MTP-2	MTP-5	MTP-2
MTP-6	MTP-4	MTP-2	MTP-6	MTP-4	MTP-2	MTP-6	MTP-3	MTP-6		MTP-3	MTP-6	MTP-3

CuOF crate, backplanes, power

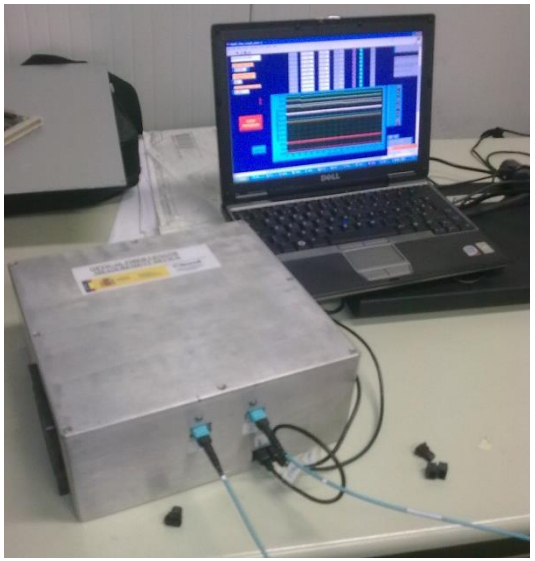


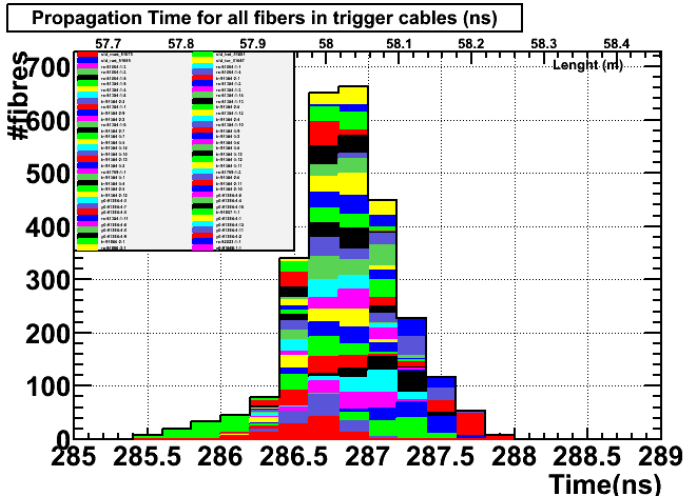


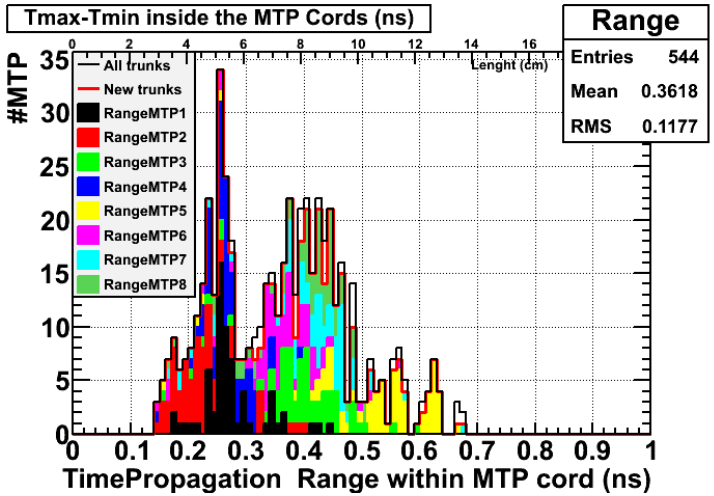




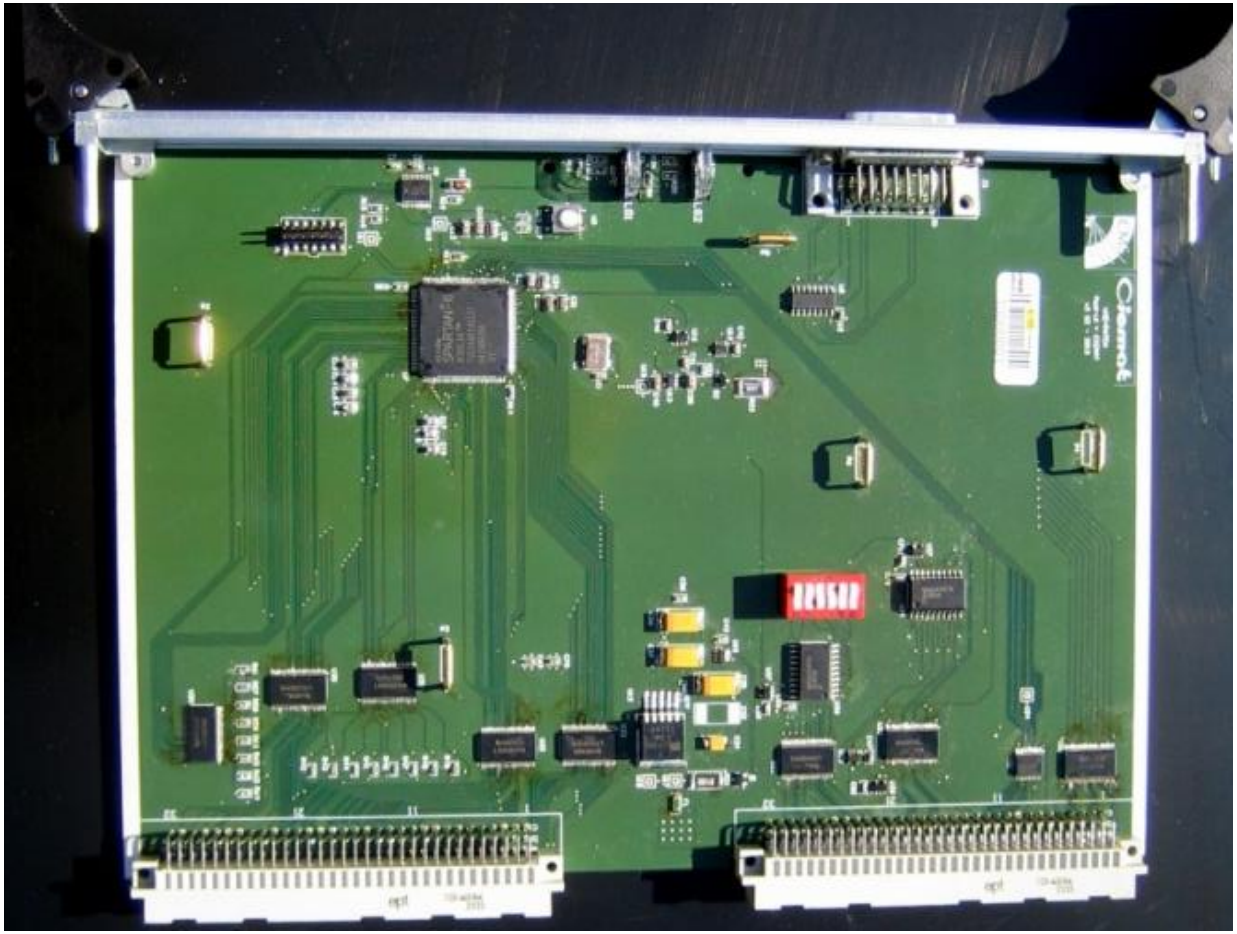
Fibre validation



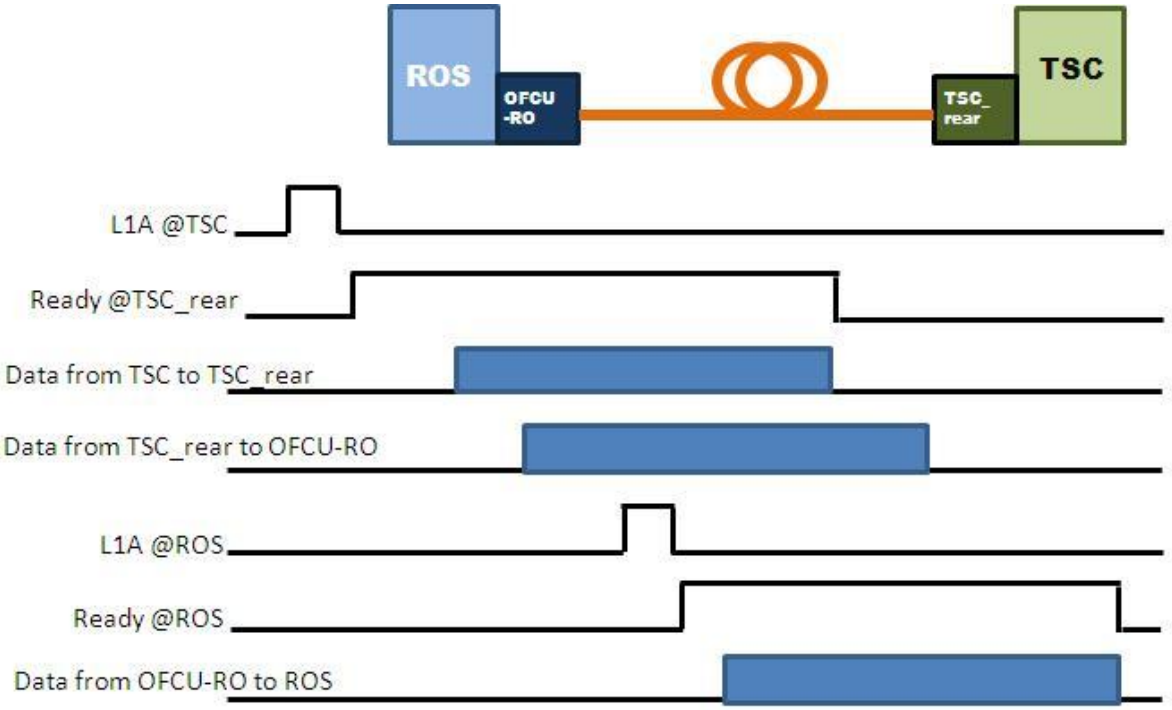




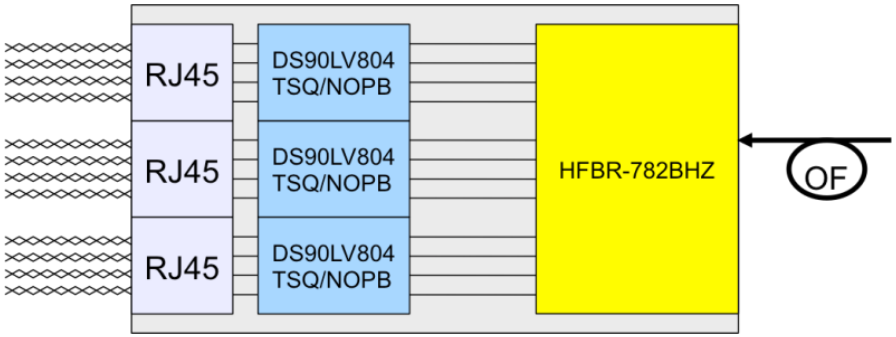
VMEpatch



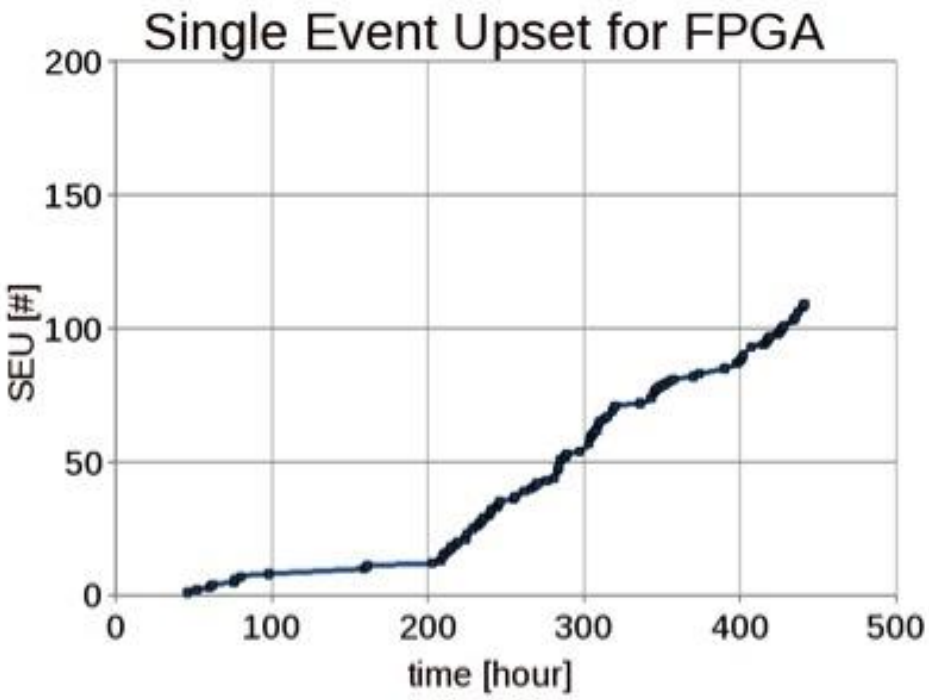
TSC debug link



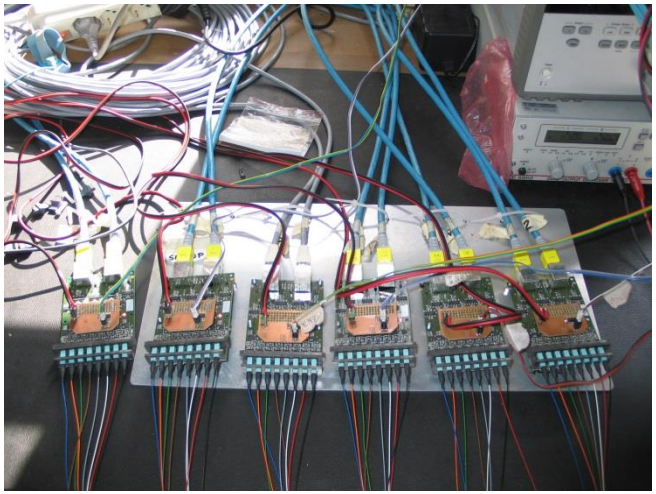
OFCU-TRG basic block

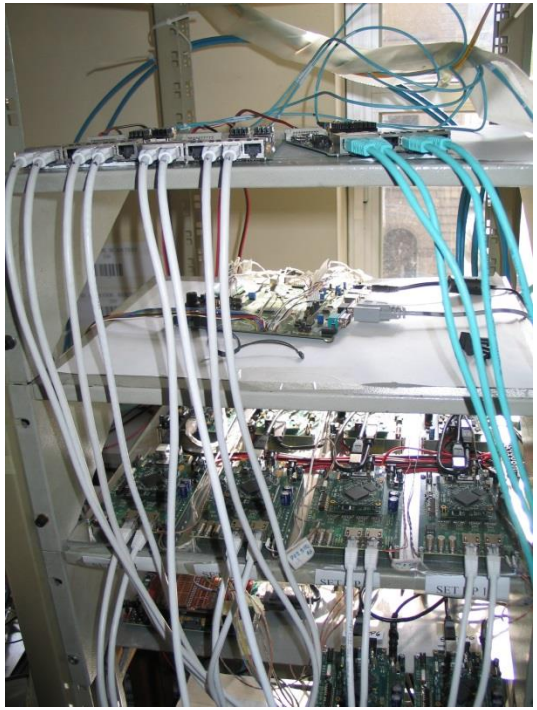


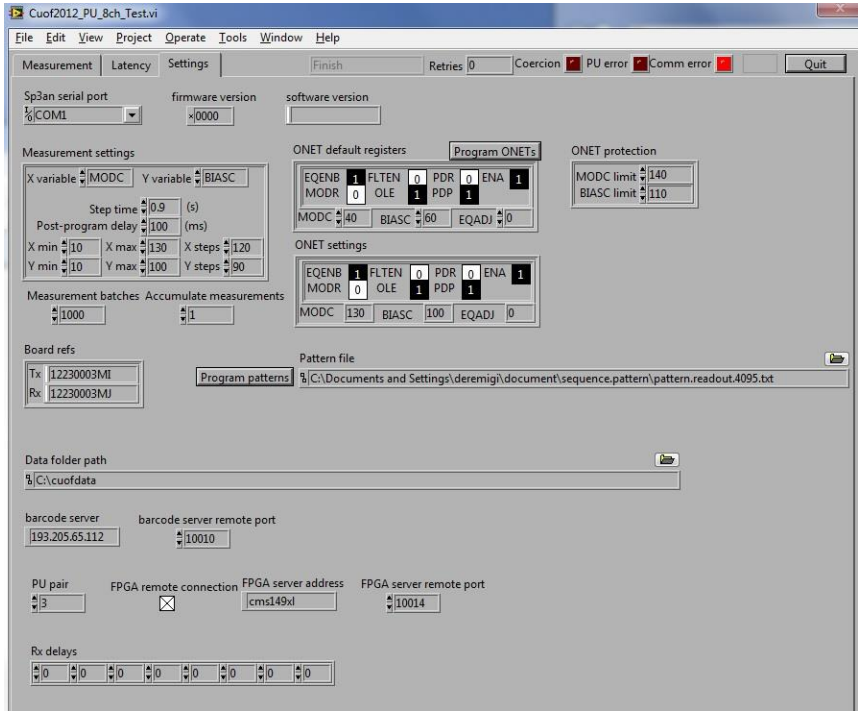
CUOF irradiation: SEU



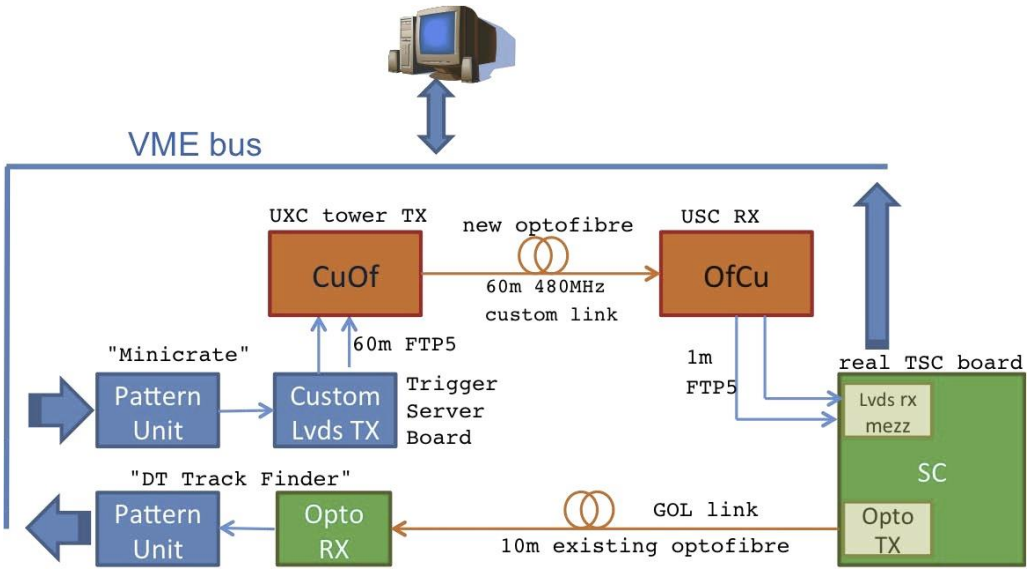
CuOF validation



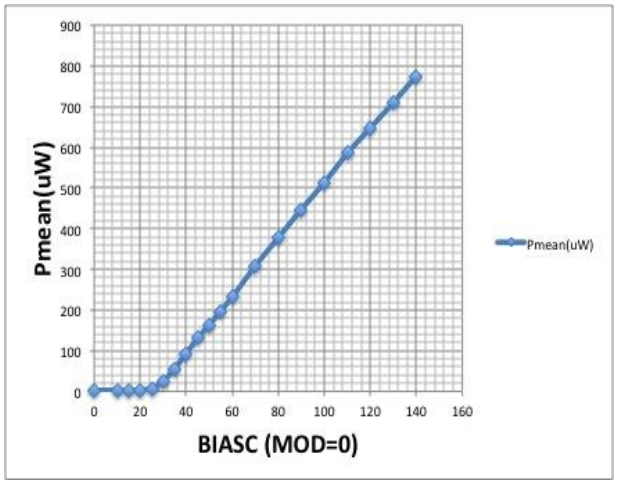


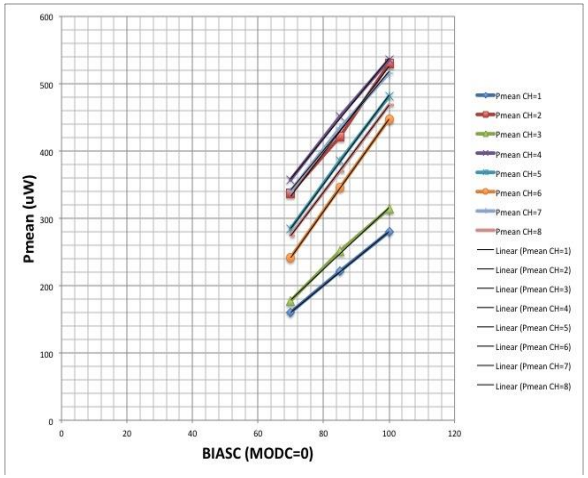


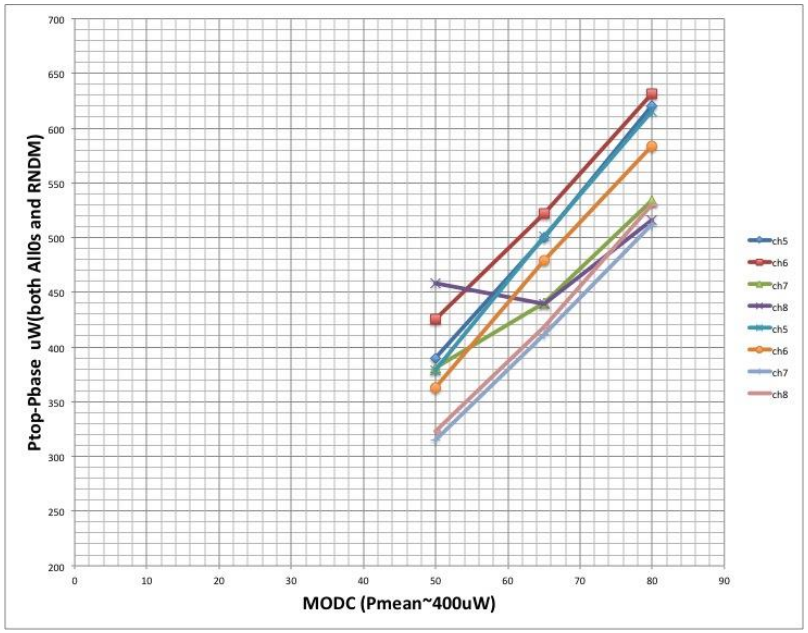
OFCU-TRG validation



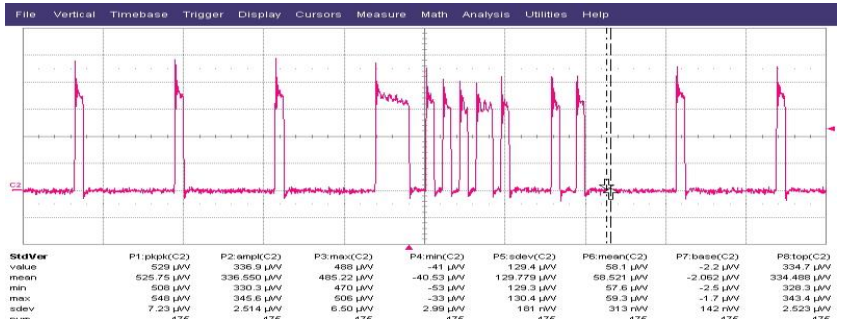
CuOF power vs bias/mod

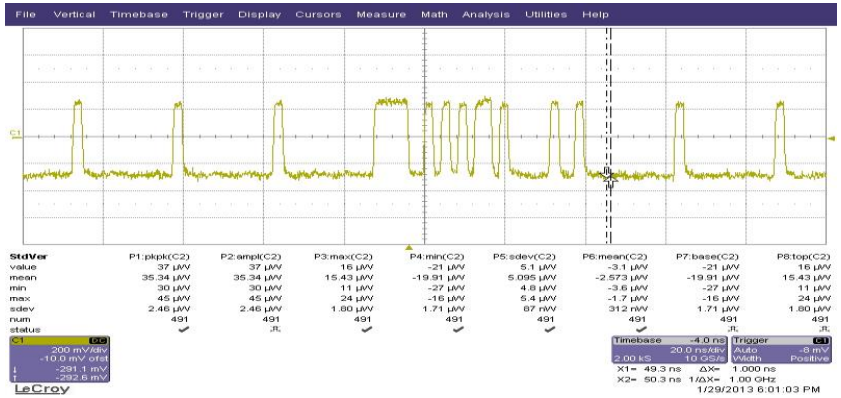


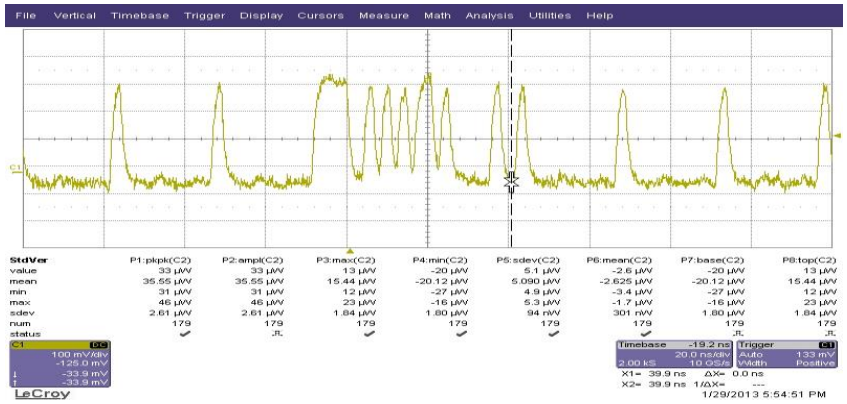




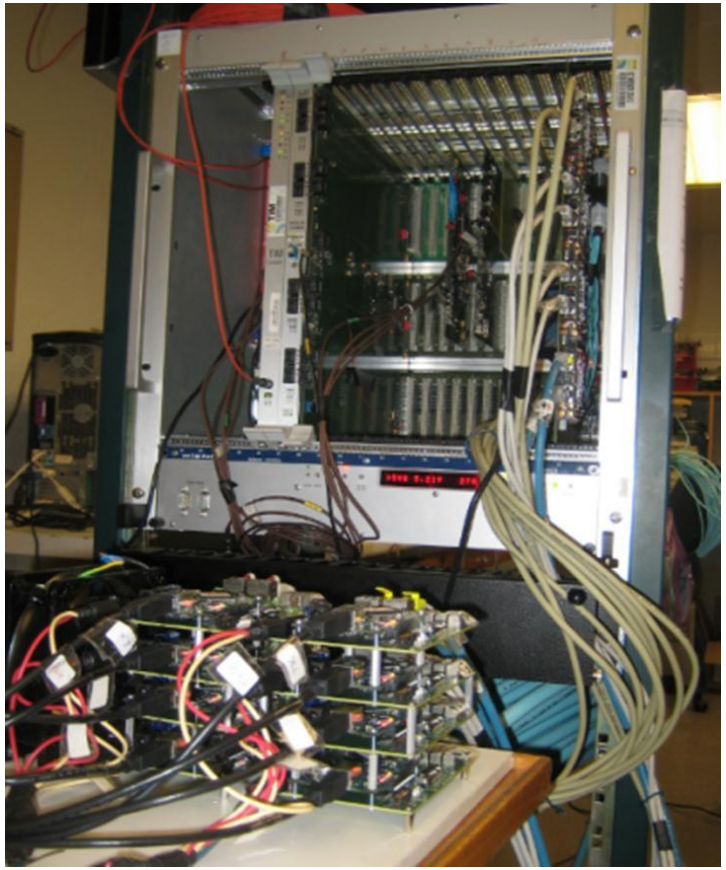
OFCu signals

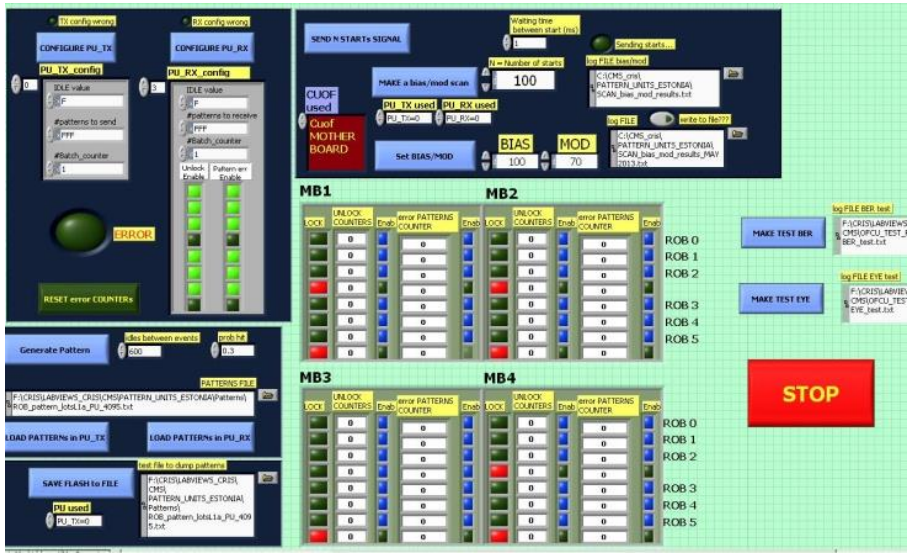


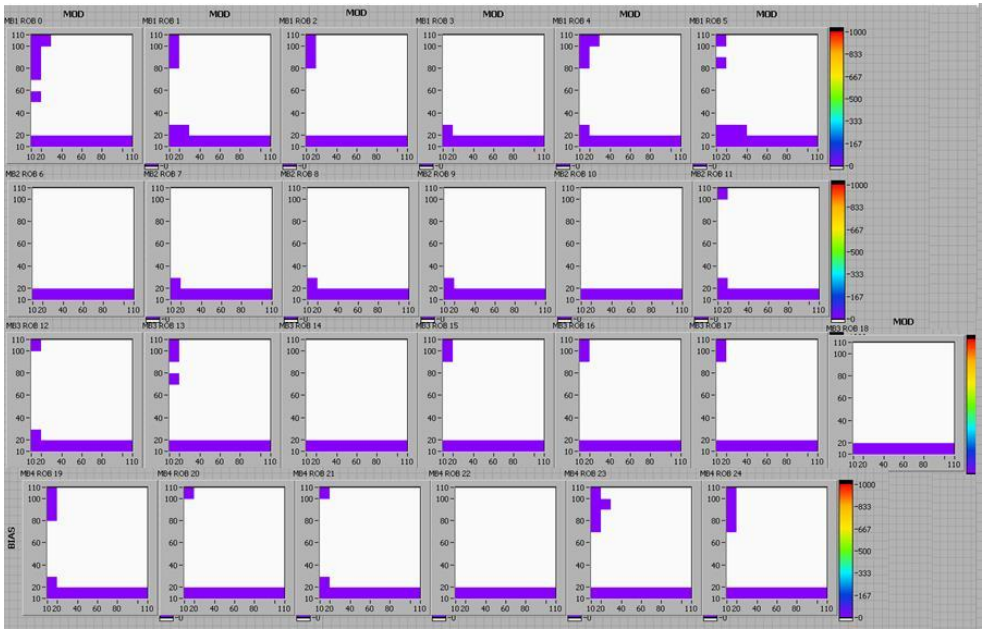




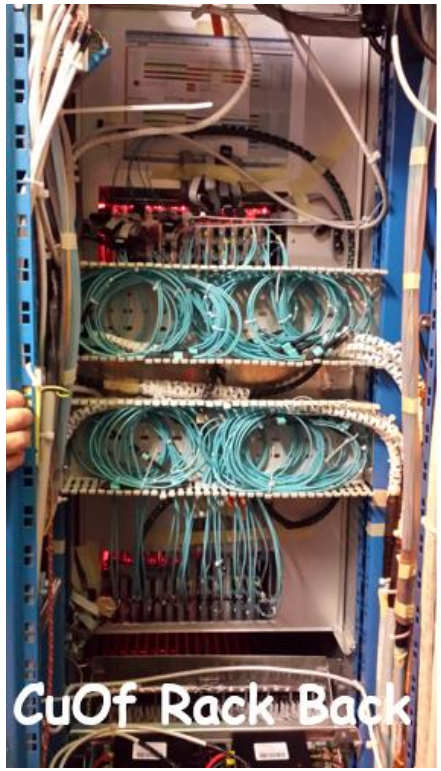
OFCu test stand

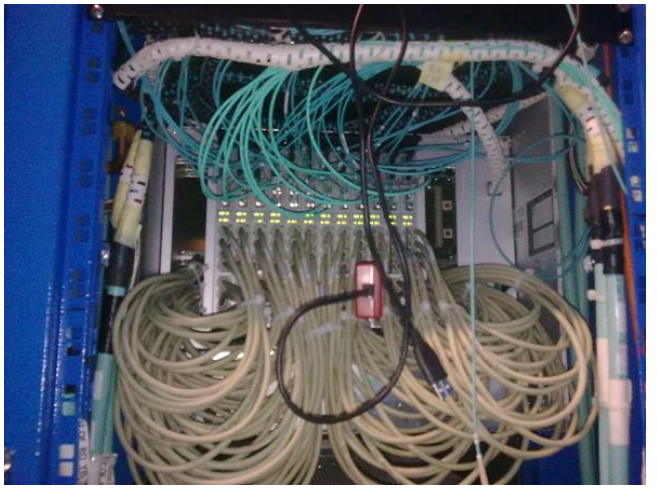




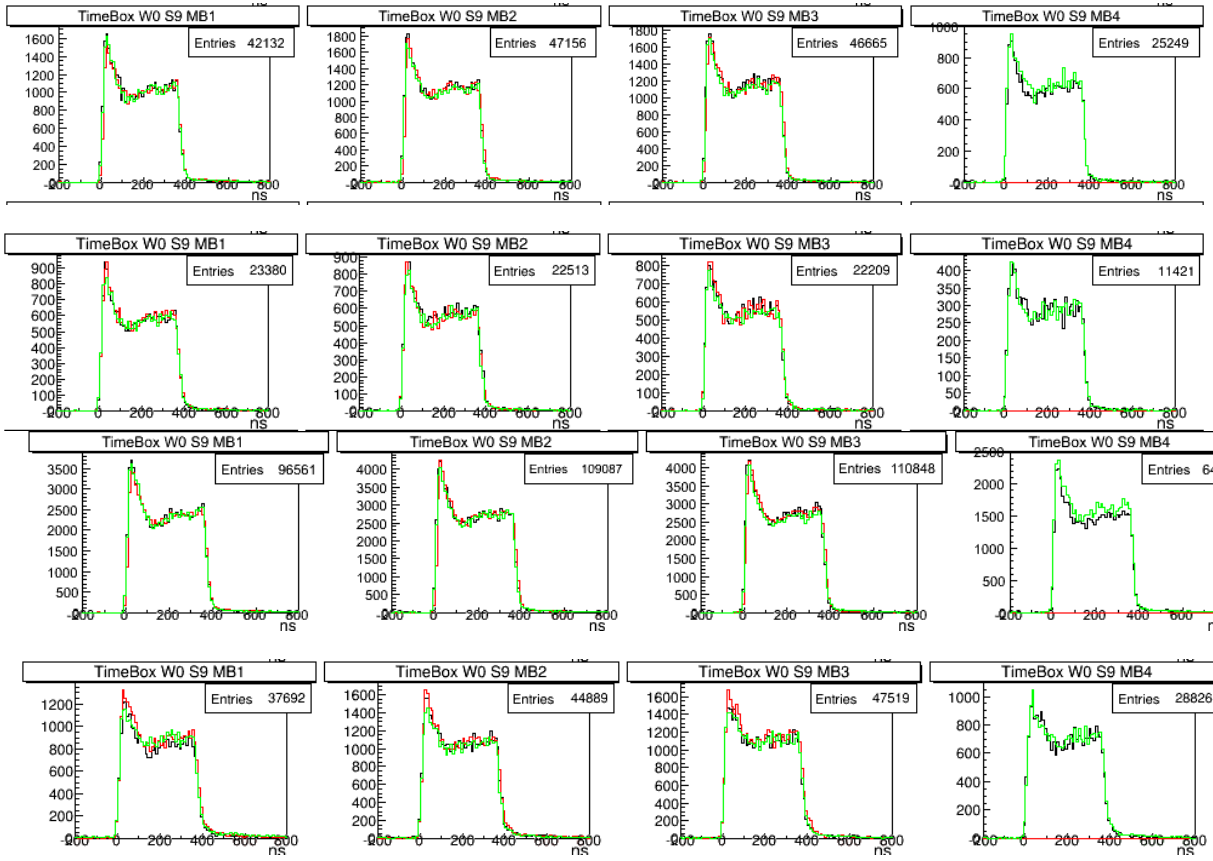


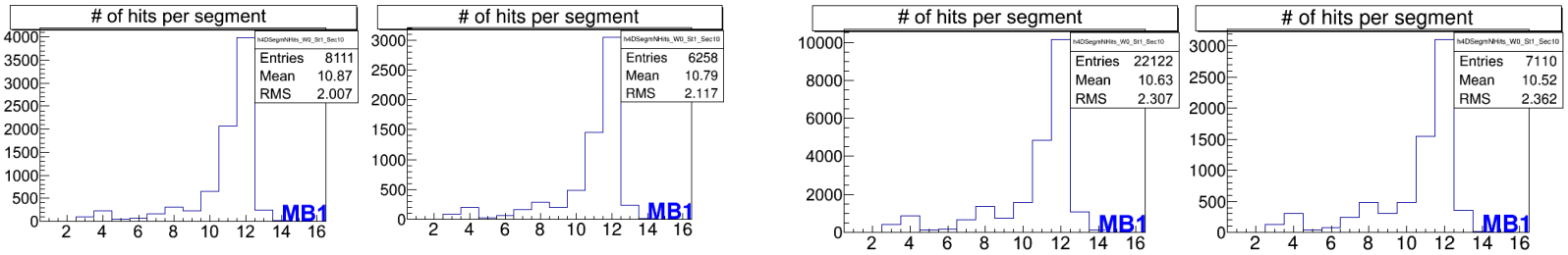
Racks





Cosmics





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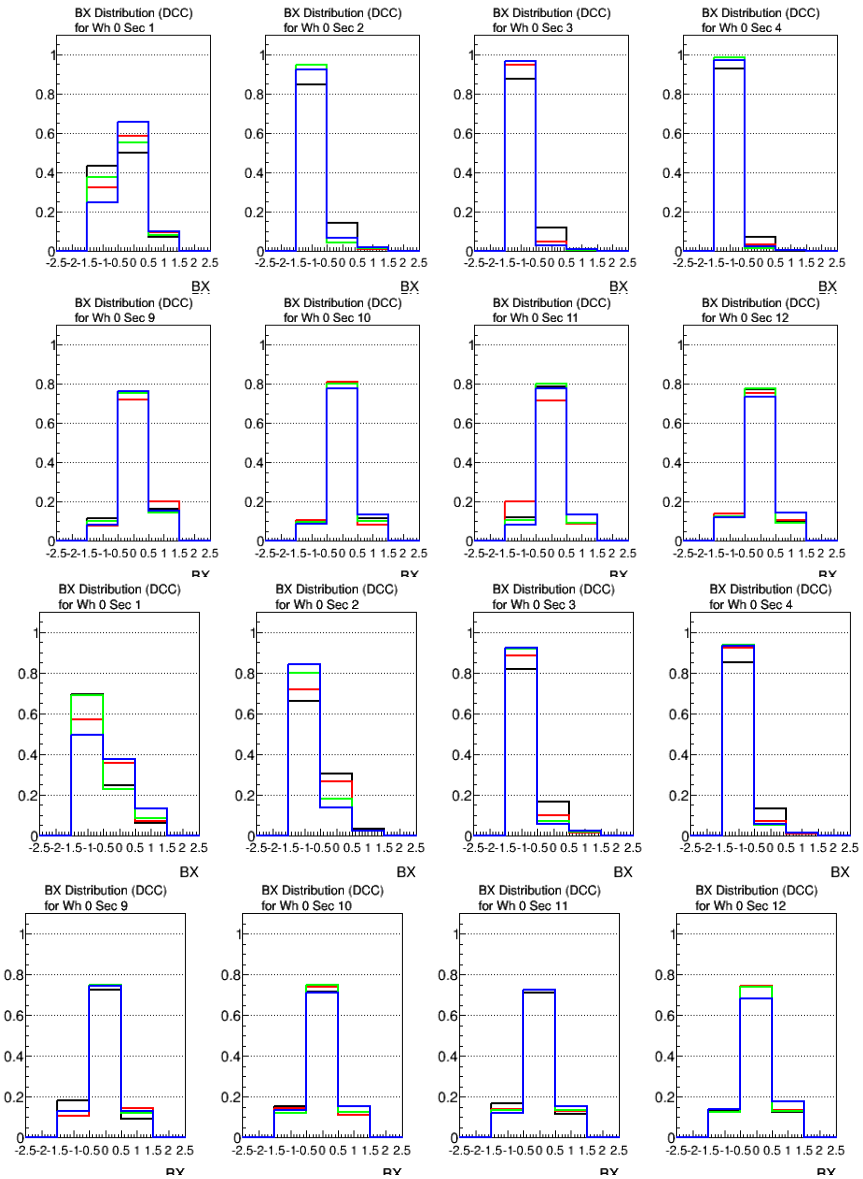
BX Distribution (DCC) for Wh 0 Sec 1
BX Distribution (DCC) for Wh 0 Sec 2
BX Distribution (DCC) for Wh 0 Sec 3
BX Distribution (DCC) for Wh 0 Sec 4
BX Distribution (DCC) for Wh 0 Sec 9
BX Distribution (DCC) for Wh 0 Sec 10
BX Distribution (DCC) for Wh 0 Sec 11
BX Distribution (DCC) for Wh 0 Sec 12
BX Distribution (DCC) for Wh 0 Sec 1
BX Distribution (DCC) for Wh 0 Sec 2
BX Distribution (DCC) for Wh 0 Sec 3
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BX Distribution (DCC) for Wh 0 Sec 12
BX


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