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The ALICE HLT Readout Upgrade for Run2

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The ALICE High Level Trigger (HLT) is a computing cluster dedicated to the online reconstruction and compression of experiment data. The interfaces to the HLT are realized with FPGA based PCIe boards. HLT has replaced all of its previous interface boards with the Common Read-Out Receiver Card (C-RORC).
This contribution describes the ALICE HLT C-RORC firmware upgrade for Run2, the extended preprocessing core for hardware based cluster finding, the software interface to the HLT data transport framework and the firmware revision management for automated deployment in the HLT cluster.

Summary

The ALICE Experiment at the Large Hadron Collider (LHC) at CERN is the detector system optimized for the study of heavy ion collisions. The readout electronics and interfaces have partially been upgraded to cope with the increased event and data rates expected during Run2.

The ALICE High Level Trigger (HLT) is a computing cluster dedicated to the online reconstruction and compression of experiment data. The HLT receives a copy of the detector data stream from the Data Acquisition System (DAQ) via the optical Detector Data Link (DDL) protocol and provides its processing results back to DAQ via DDL. Event reconstruction is performed in the HLT with the help of FPGA based cluster finding directly in the input data stream and with GPU based tracking supporting the CPU data processing. The interface between the optical readout link and the processing nodes is realized with FPGA based PCIe boards. The HLT has replaced all of its previous readout boards with the Common Read-Out Receiver Card (C-RORC), which has been developed and produced in a cooperation of ALICE DAQ, ALICE HLT and ATLAS TDAQ ROS.

This contribution describes the ALICE HLT C-RORC firmware upgrade for Run2, the commissioning phase and first running experience. The FPGA PCIe interface consists of a custom scatter-gather based DMA engine operated from a user space device driver and integrated into the existing data transport software framework. An on-board DDR3 interface provides data replay capabilities of previously recorded detector data. The hardware preprocessing core for online cluster finding was extended to handle the double input data rate, providing significant savings on the required CPU computing power. The mix of different optical link rates for different detectors makes it necessary to deploy a number of different firmware images throughout the cluster. An automated firmware revision management and deployment system makes sure that each node in the HLT cluster runs the correct firmware.

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