Simulation of Digital Pixel Readout Chip Architectures with the RD53 SystemVerilog-UVM Verification Environment Using Monte Carlo Physics Data

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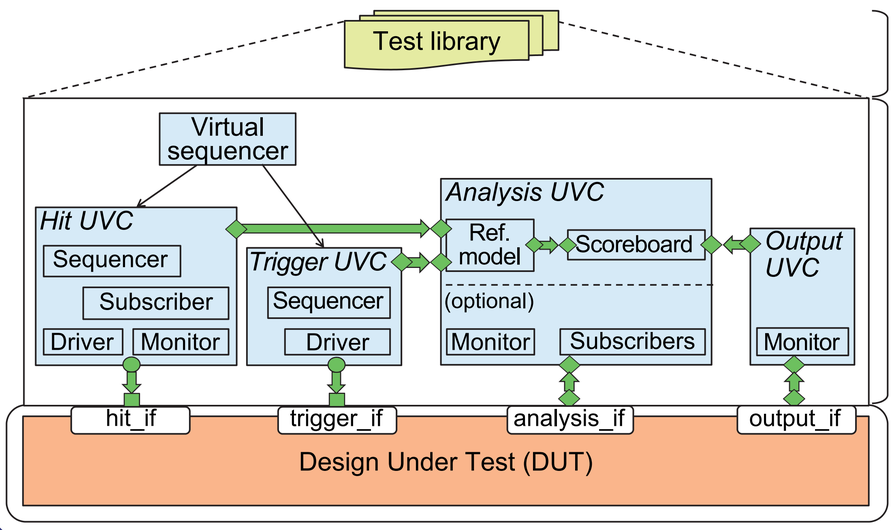
I. INTRODUCTION: VEPIX53 FRAMEWORK

- A flexible simulation and verification platform is being developed within the RD53 collaboration using the SystemVerilog hardware description and verification language and the Universal Verification Methodology (UVM) library.
- Such an environment, called VEPIX53 (**V**erification **E**nvironment for RD53 **PIX**el chips) is seen as a valuable development tool for the next generation hybrid pixel readout chips that will be used in the foreseen Phase 2 pixel upgrades at the LHC [1].
- Main goals:
  - flexible generation of input stimuli
  - automated verification functions
  - simulation at increasingly refined level as design progress

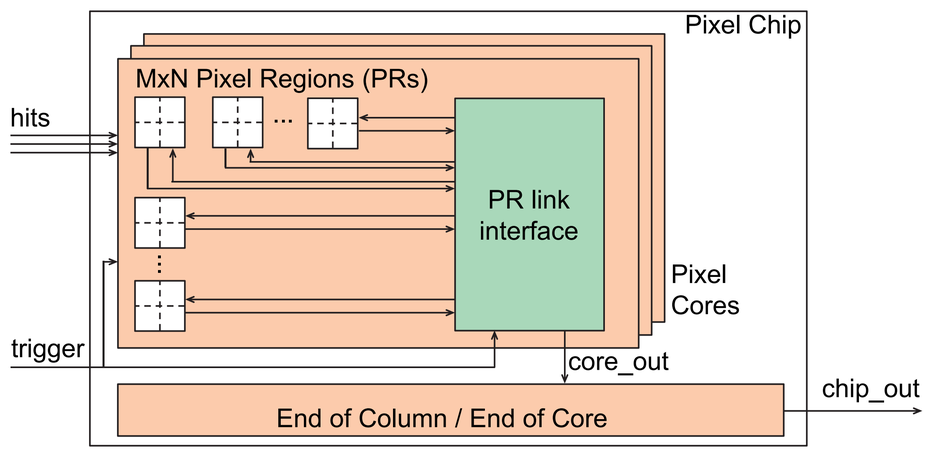


TEST SCENARIO
– configures UVM verification components (UVCs)

TESTBENCH
– hit generation and injection
– monitoring of pixel chip input and output
– conformity checks and statistics collection

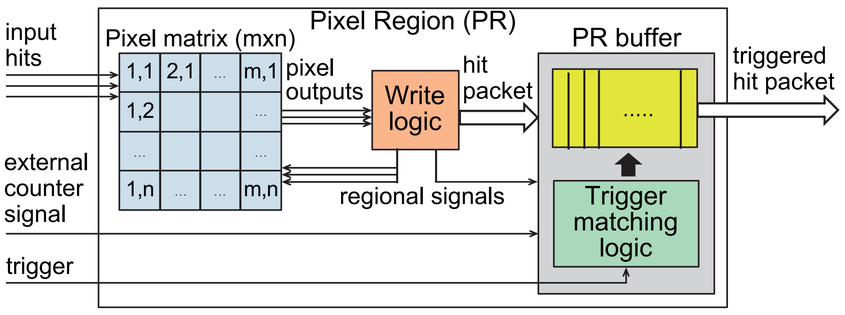
TOP MODULE
– contains DUT and connects it to verification components

II. GENERIC PIXEL CHIP MODEL

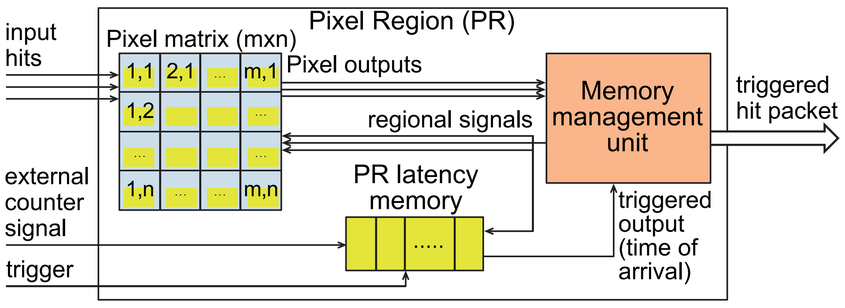


- Highly parameterized description at behavioral level for investigating each building block: digitization (ToT/ADC), pixel regions (PR), pixel region arrangement (columns/cores), EoC (data merging, readout)
- PR link interface abstracts link between pixel regions enabling simple description of arbitration schemes

Pixel region: latency buffering architectures



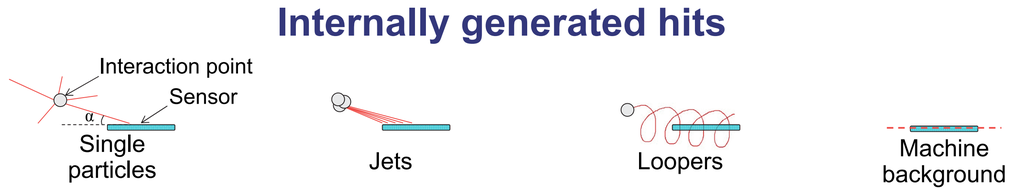
Zero-suppressed FIFO
– single shared hit packet buffer



Distributed latency counters
– shared hit time buffer (latency counters)
– independent ToT buffer in each pixel unit cell

III. DIFFERENT KINDS OF INPUT STIMULI

Internally generated hits



External Monte Carlo simulation data

CMS: ROOT/ASCII files produced by workflow based on CMSSW

- Pixel size: 25x100 μm² / 50x50 μm²
- Sensor thickness: 150 μm
- Pileup: 140
- Layer: 1 → center/edges of detector
- Digitizer threshold: 1500 e⁻

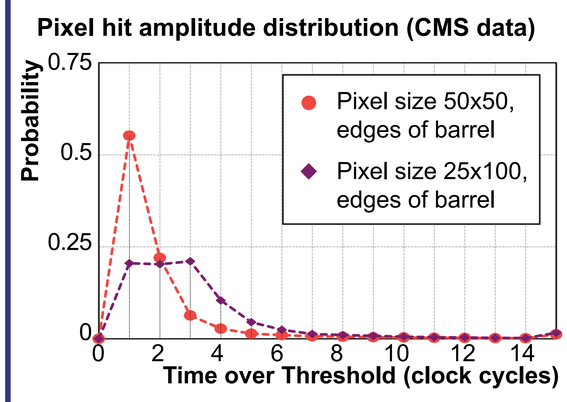
ATLAS: text files extracted from Analysis Object Data (xAOD) generated with the ATLAS simulation chain

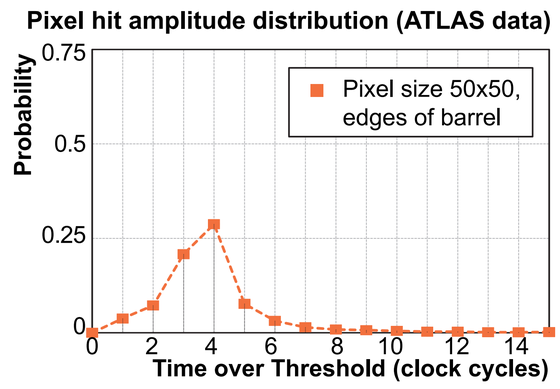
- Pixel size: 50x50 μm²
- Sensor thickness: 150 μm
- Pileup: none (integration over phi)
- Layer: 0-3 → center/edges of detector
- Digitizer threshold: 500 e⁻

IV. SIMULATION RESULTS

a. Statistics on input hits

Information extracted from data sets through VEPIX53 simulations (independent from DUT):
- Hit amplitude distribution per pixel
- Monitored hit rate on full matrix

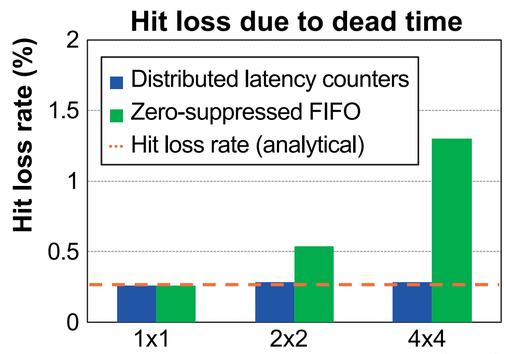


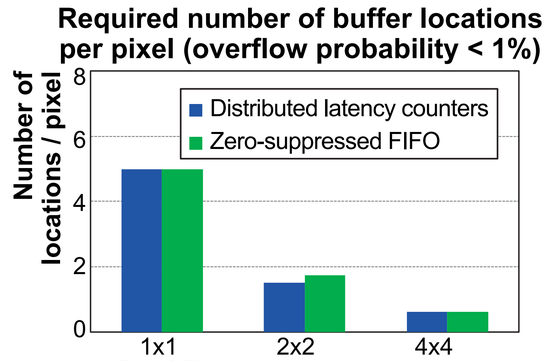


b. Single Pixel Region simulation

Simulation parameters (imported Monte Carlo data):
- Pixel size: 50x50 μm²
- Innermost layer, center of detector
- Simulation run for 480,000 clock cycles (~12 ms)

⇨ Monitored hit rate: 2.1 GHz/cm²





After fixing the buffer size to the suggested number of locations:

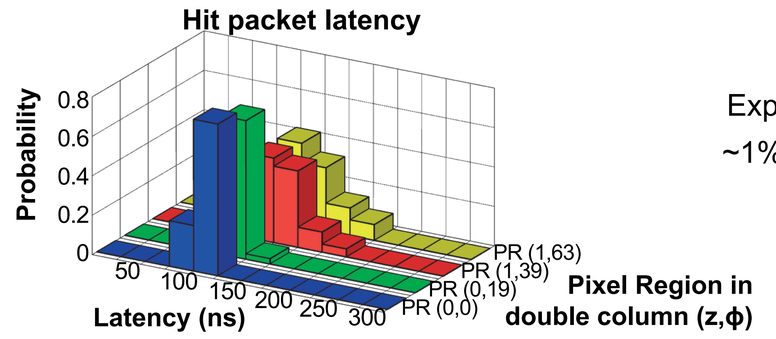
Pixel region (zxϕ)	Buffer locations	Lost hits due to buffer overflow	
		Zero-suppressed FIFO	Distributed latency counters
2x2	7	0.10%	0.11%
4x4	10	0.17%	0.27%

c. Double Column simulation

Design Under Test (DUT):
- Double column made of 2x64 pixel regions
- Pixel Region made of 2x2 pixel unit cells
- Arbitration scheme based on token passing with fast skipping (similar to ATLAS FE-I4 [2])

Simulation parameters (imported Monte Carlo data):
- Pixel size: 50x50 μm²
- Innermost layer, center of detector
- Independent triggers
- Simulation run for 650,000 clock cycles (~16 ms)

⇨ Monitored hit rate: 2.1 GHz/cm²
Monitored trigger rate: 960 kHz



⇩

Expected bandwidth:
~1% of a 40 MHz bus

V. CONCLUSIONS AND FUTURE WORK

- Simulation framework with Monte Carlo data is vital for design optimization; quantities currently under investigation are correctly monitored.
- 2x2 and 4x4 regions are more efficient than single pixel in terms of memory utilization and the distributed latency counters architecture is more convenient than the zero-suppressed FIFO one in terms of dead time.
- Double column simulation shows that double column bus is largely sufficient if running at 40 MHz.
- Extensive architecture simulation has started; validation of Monte Carlo data through sanity checks to be finalized.
- Behavioral results to be completed with RTL (implementation-oriented).
- Other arbitration schemes and complete architectures (e.g Transfer While Wait) will be implemented and simulated.

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References

[1] S. Marconi, E. Conti, P. Placidi, J. Christiansen and T. Hemperek, "The RD53 collaboration's SystemVerilog-UVM simulation framework and its general applicability to design of advanced pixel readout chips," Journal of Instrumentation, vol. 9, no. 10, p. P10005, 2014.

[2] FE-I4 Collaboration, "The FE-I4A Integrated Circuit Guide," Version 11.3, CERN (2011).

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