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Simulation of Digital Pixel Readout Chip Architectures for the LHC Phase 2 Upgrades with a SystemVerilog-UVM Verification Environment

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The SystemVerilog-UVM simulation and verification platform VEPIX53, developed by the RD53 collaboration, is being used for the study and optimization of digital pixel chip architectures at behavioral level. The stimuli used by the framework can be generated internally using pre-defined hit classes or can also be imported from external CMS and ATLAS Monte Carlo detector simulations, featuring very high rate ($\sim 2-3$ GHz/cm^2). VEPIX53 simulations produce statistics on inputs and enable architecture study through monitoring of design under test performance. A dedicated generic pixel chip model is being described at behavioral level for evaluating different architectures.

Summary

A flexible simulation and verification platform is being developed in the framework of the RD53 collaboration using the SystemVerilog hardware description and verification language and the Universal Verification Methodology (UVM) class library. Such an environment, called VEPIX53 (Verification Environment for RD53 PIXel chips) is a valuable development tool within the collaboration for the next generation hybrid pixel readout chips that will be used in the foreseen Phase 2 pixel upgrades at the LHC, aimed to handle system complexity, evaluate multiple system architectures and achieve best design optimization through the concurrent contribution of multiple designers.

The VEPIX53 environment is currently being used for both the simulation of existing designs, such as the ATLAS FE-I4 at Register Transfer Level (RTL), and the explorative study of digital pixel readout chip architectures. For the latter case a generic, fully parameterized pixel chip model is being developed at behavioral level and initial simulation results have already been produced concerning the trigger latency buffering section of single groups of pixels (so-called pixel regions), for which two alternative architectures were described.

Different categories of input stimuli can be injected to the design under test (DUT) in the environment. Realistic-looking clusters of hit pixels can be generated internally using a set of pre-defined classes of hits. On the other hand, it is also possible to import external actual physics data produced by Monte Carlo simulations of pixel detectors: different sets of hit patterns are being used for simulations, provided by both the CMS and ATLAS experiments, featuring different parameters and operating conditions related to HL-LHC and the prospected specifications of the Phase 2 upgrade, such as pileup (140 or 200), pixel size (50×50 or 25×100 μm^2), sensor thickness, layer, position in the barrel (center or edges) and others.

Independently from the specific DUT being simulated, VEPIX53 produces statistical information on the imported hits, like monitored hit rate and hit amplitude distribution. In case of architecture exploration, the analysis verification components defined in the environment make it possible to monitor the performance of the DUT and, therefore, different architectures can be compared under several conditions using different data sets. In particular, latency buffer occupancy and hit loss rate due to pixel dead time and buffer overflow are being investigated as performance indicators for trigger latency buffering architectures. The study will also move on the evaluation of different strategies of arranging pixel regions in cores, in accordance with the layout proposed by the RD53 community. The environment will be used for extensive verification of the full pixel chip design, from high abstraction level down to detailed gate level after final place and route.

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