Pulsar IIb Design, System Integration and Next-Generation Full Mesh ATCA Backplane Test Results

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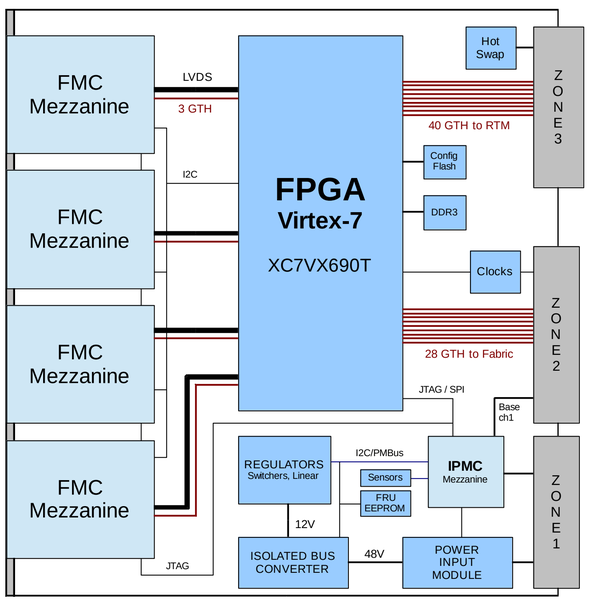
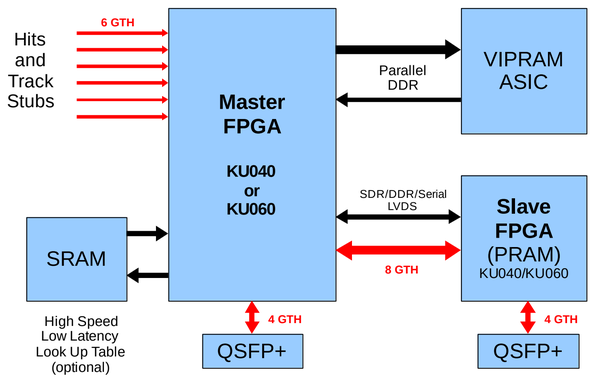
Abstract

The Pulsar IIb is a custom ATCA full mesh enabled FPGA-based processor board which has been designed with the goal of creating a scalable architecture abundant in flexible, non-blocking, high bandwidth interconnections. The design has been motivated by silicon-based tracking trigger needs for LHC experiments. In this talk we describe the Pulsar II hardware and it's demonstrated interconnection capabilities, including the test results with the ATCA 40G+ full mesh backplane. In addition we present the ProtoPRM mezzanine board which can serve as the core pattern recognition and track fitting engine for CMS L1 Tracking Trigger R&D using the associative memory approach.

Pulsar IIb Architecture



Pulsar IIb Front Board



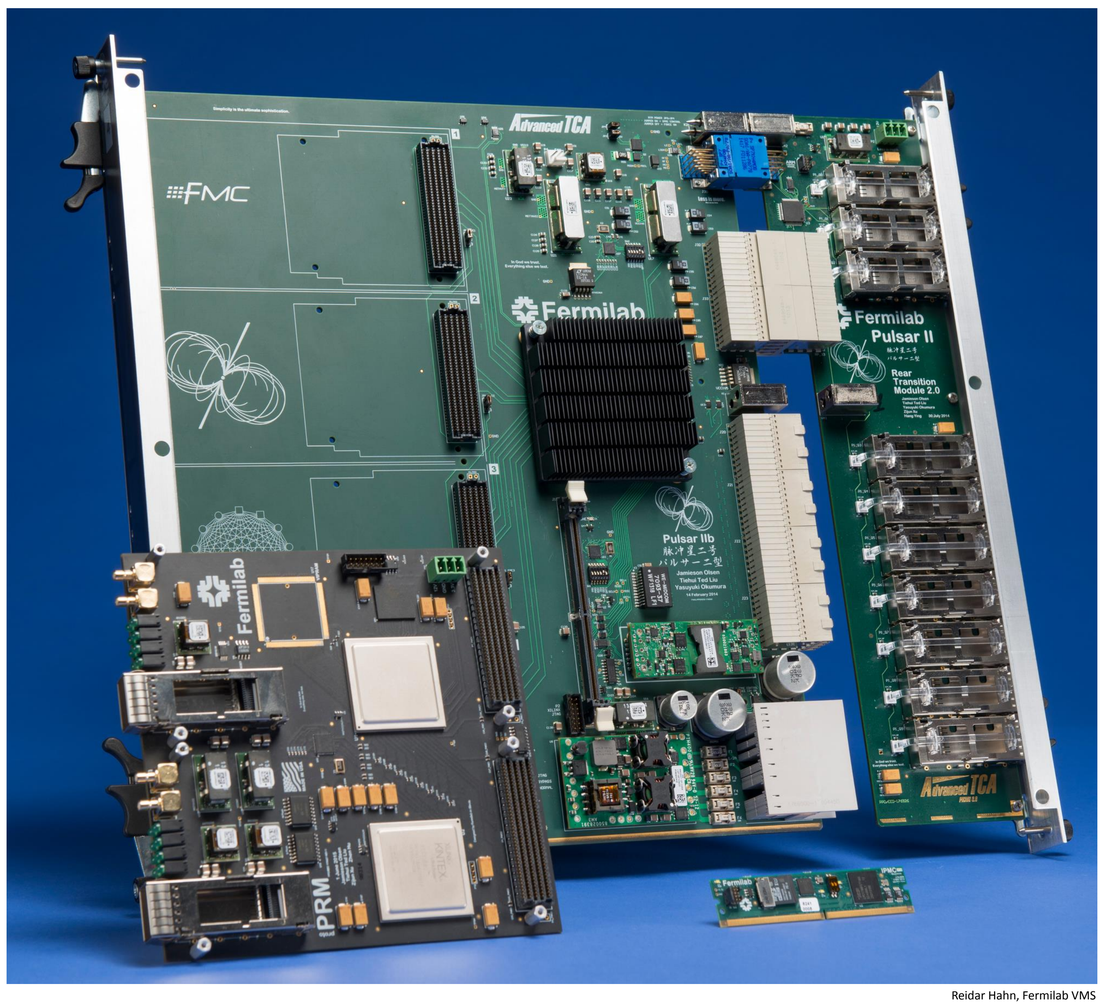
Prototype Pattern Recognition Mezzanine Board

Pulsar IIb Front Board Features

- Xilinx Virtex 7 FPGA
  - XC7VX690T -2 FFG1927C
  - 690,000 logic cells
  - 52 Mbit dual port BlockRAM
- 80 GTH 12.5 Gbps transceivers
  - 40 GTH for Rear Transition Module (RTM)
  - 28 GTH for Full Mesh Fabric Interface
  - 12 GTH for Mezzanines
- 256 MB DDR3-1066
- Four FMC Mezzanine Cards
  - 35W per card, up to 60W possible
  - 34 unidirectional LVDS pairs per card
  - 3 SERDES (GTH) lanes per card
- IPMC Mezzanine Card
  - Basic IPMI protocol support including hot swap for front board and RTM
  - Monitors over 30 temperature, voltage, and current sensors with data records and thresholds
  - 100BASE-T Ethernet on the Base Interface for slow controls and JTAG programming (XVC protocol)
- M-LVDS clock distribution on ATCA backplane
- Programmable low-jitter reference clocks
- Zone-3 connectors are PICMG 3.8 compliant

ProtoPRM Features

- Dual Kintex UltraScale FPGAs
  - KU040 or KU060, -2 speed
  - Up to 580k logic cells
  - Up to 38 Mbit dual port BlockRAM
- 16 Gbps GTH serial transceivers
  - Up to 8 lanes for communication with Pulsar2b
  - 8 lane Master-Slave FPGA local bus
  - 4 lanes per FPGA for QSFP+ optical modules
- 36 Mbit low latency DDR II+ static RAM
- Socket for VIPRAM ASIC (TQFP176)
- Dual high pin count FMC connectors
- Slave FPGA can be used for implementing PRAM ASIC functionalities for performance and optimization studies.



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Demonstrated Interconnection Bandwidth

- ✓ Pulsar IIb FPGA to full mesh backplane channels **10Gbps/lane**
- ✓ Pulsar IIb FPGA to FMC Mezzanine (GTH) **10Gbps/lane**
- ✓ Pulsar IIb FPGA to FMC Mezzanine (parallel LVDS) **800 Mbps/pair**
- ✓ Pulsar IIb FPGA to Rear Transition Module QSFP+ over fiber **10 Gbps/lane**
- ✓ ProtoPRM FPGA to QSFP+ over fiber **10 Gbps/lane**
- ✓ ProtoPRM Master-Slave FPGA interconnections **15.6 Gbps/lane**

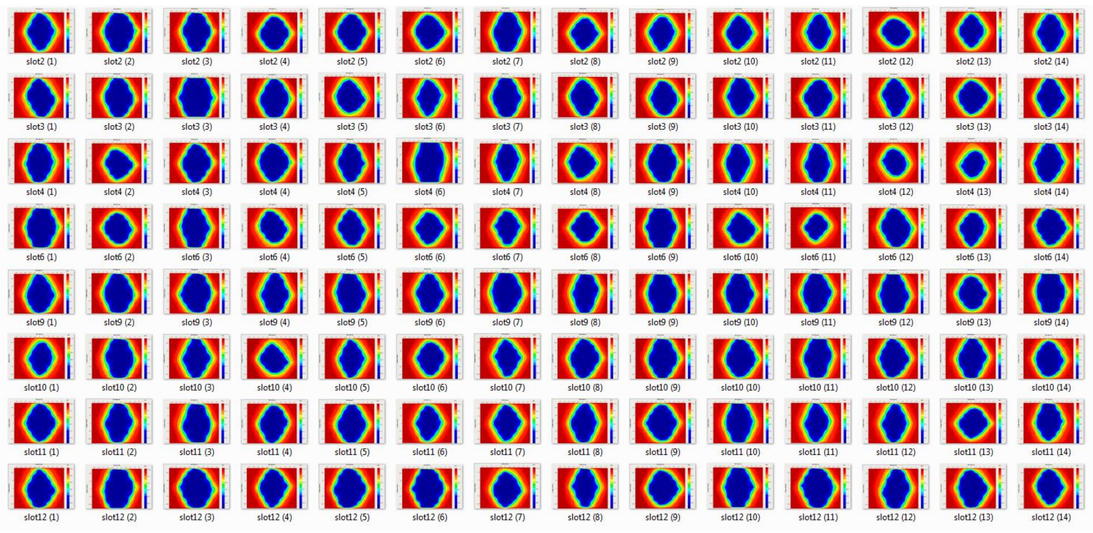
Achieved performance meets all expectations and satisfies the needs for the Tracking Trigger Demonstration

Pulsar IIb FPGA to Full Mesh ATCA Backplane

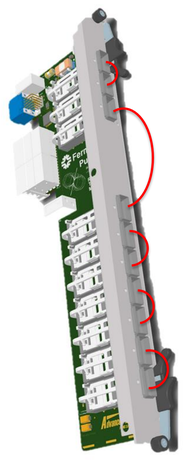
The CMS L1 Tracking Trigger demonstration system requires flexible high-bandwidth non-blocking communication channels between boards at the crate level. In order to handle sustained **multi-Tbps** data input rates the Pulsar IIb boards in the ATCA shelf utilize sophisticated time-multiplexing schemes which take advantage of the full mesh backplane architecture. The Pulsar IIb was designed to support 10 Gbps per lane across the full mesh backplane.

Our backplane test results indicate that channel performance consistency is one of the most significant challenges facing ATCA backplane manufacturers today. Many of the ATCA full mesh backplanes we tested showed significant slot to slot link performance variations across the backplane.

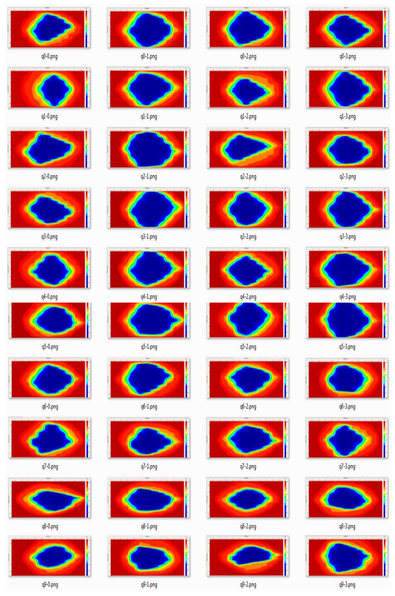
In late 2014 COMTEL delivered to us their latest "Air/Plane" 40G+ full mesh ATCA backplane. This new backplane design, which uses an advanced low loss substrate material and careful layout to minimize the slot dependences, has to date yielded the best and most consistent link performance with all eight Pulsar IIb prototype boards running all GTH transceivers simultaneously (56 lanes) at 10 Gbps. The statistical eye diagrams below show a large blue region which corresponds to a bit error ratio of 10^{-9}. After a few days all channels reported no errors with a BER of 10^{-15}.



Pulsar IIb to Rear Transition Module

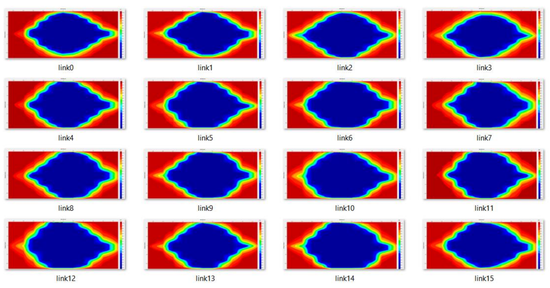


The rear transition module (RTM) receives the silicon detector data upstream, each supports up to ten QSFP+ fiber transceiver modules, which are directly connected to the Pulsar IIb front board FPGA. A QSFP+ module has four lanes each capable of bidirectional transfers up to 10.3125Gbps. Our RTM design has been tested successfully at **10 Gbps** per lane. In this test configuration the Pulsar IIb FPGA is loaded with the Xilinx IBERT firmware and generates test patterns on 40 GTH transmitters. The differential serial lines travel from the FPGA to the Zone-3 data connectors (up to 12cm) and then down the RTM board (up to 30cm) before entering the QSFP+ module and looping back over active optical cables (AOCs).



ProtoPRM FPGA Interconnection

The ProtoPRM Mezzanine was designed, in part, to test and evaluate new high speed I/O interfaces for future versions of the pattern recognition associative memory (PRAM) ASICs being developed at Fermilab. For this reason the master and slave FPGAs are connected with a 24-bit parallel LVDS bus and eight GTH transceivers. The eight GTH transceivers have been successfully tested at 15.6 Gbps per lane, which is the upper limit of our Kintex UltraScale FPGAs.



Pulsar IIb to ProtoPRM

In the CMS L1 Tracking Trigger demonstration system the ProtoPRM mezzanine boards act as the core pattern recognition and track fitting engines and they receive hit data from the Pulsar IIb FPGA. The ProtoPRM master FPGA is connected to the Pulsar IIb FPGA through 6 high speed serial GTH lanes over two FMC connectors. These serial connections have been tested at up to 10 Gbps per lane.