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Front End ASIC for AGIPD, a high dynamic range fast detector for the European XFEL

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Adaptive Gain Integrating Pixel Detector (AGIPD) is a hybrid pixel X-ray detector for the European-XFEL. The detector's important part is the radiation tolerant front end ASIC fulfilling the European-XFEL requirements: High dynamic range - from sensitivity to single 12.5keV-photons up to $10^{>4}$ photons. It is implemented using the dynamic gain switching technique with three possible gains of the charge sensitive preamplifier. Each pixel can store up to 352 images in memory operated in random-access mode at ≥ 4.5 MHz frame rate. An external vetoing may be applied to overwrite "bad" frames.

Summary

One of the main features of the European XFEL will be high brilliance pulses at a high repetition rate. The pulses will form a bunch train repeating at a frequency of 10 Hz. Each bunch train contains 2700 pulses of $>10^{>12}$ photons of 12keV each, separated by 220 ns.

The key requirements of AGIPD were derived from the unique properties of this source:

- A high dynamic range, extending from single photon sensitivity to $10^{>4}$ photons
- A frame rate of 4.5 MHz
- As many good images as possible
- Radiation hardness of several 10kGy

Before the development of the full-scale ASIC "AGIPD 1.0" 6 MPW prototypes were designed in IBM 0.13 μ m 8RF-DM technology. Those prototypes were used to prove the adaptive gain concept used to cope with the dynamic range, to measure the characteristics of analogue and digital blocks, and to investigate the radiation hardness of those blocks and the chosen technology.

The full-scale chip is an $\sim 13 \times 14$ mm² ASIC containing a 64×64 array of 200×200 μ m² pixels, steered via digital buffers on two sides by the controlling periphery logic. The third side of the pixel matrix is connected to 4 analogue multiplexers, driven by the logic block as well. The ASIC is supplied with 1.5V and has a consumption of approximately 1.65W in operating mode.

The input stage of each pixel is a charge sensitive preamplifier (CSA), which integrates the charge of the 500 μ m thick silicon sensor. After the preamplifier the signal path splits into a correlated double sampling (CDS) stage to remove the reset and low frequency noise. The other branch is formed by a discriminator, which, if triggered by an input signal, causes the addition of integration capacitors to the preamplifier feedback. This way the sensitivity is lowered and the dynamic range is increased in two steps. Both, the output of the CDS buffer and a voltage level encoding of the selected gain, are written to an analogue memory capable of storing 352 images. Thus each memory cell is actually composed of two capacitors. Operation of the pixel and the arbitrary addressing of the memory are controlled by the periphery logic. It has a command based serial interface. After each bunch train, the stored signals are read out through the pixel buffer, column buffer and off-chip driver as 'amplitude' and 'gain' frames.

All prototype ASICs as well as the full scale one were extensively tested and characterized. The non-linearity of the amplitude for all three gain stages was measured to be less than 0.5% and the noise is approximately

260 e⁺ for the highest gain –and always below the Poissonian fluctuation of the input signal. The ASIC features internal DACs to bias the analogue circuits as well as internal calibration structures - a current source and a capacitor based charge injector are used. Experimental results will be presented as well.

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