# LOCx2, a Low-latency, Low-overhead, 2 × 5.12-Gbps Transmitter ASIC for the ATLAS Liquid Argon Calorimeter Trigger Upgrade


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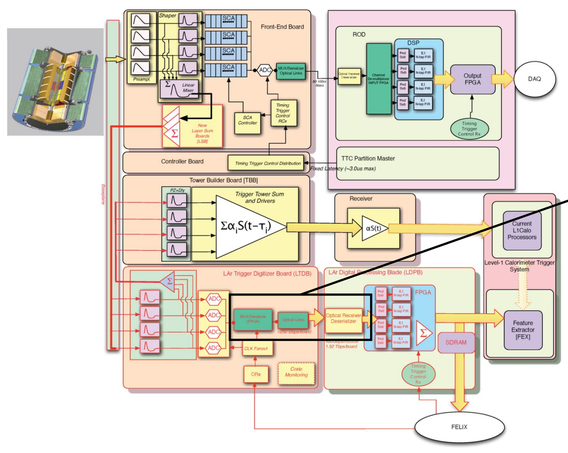
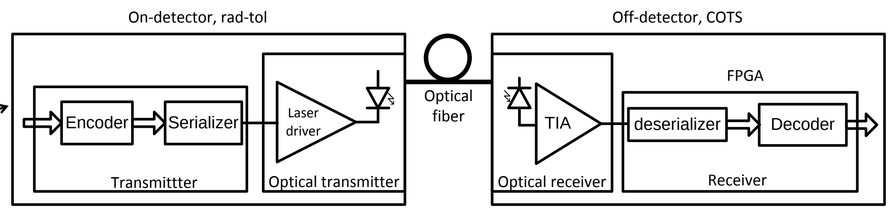
## Introduction

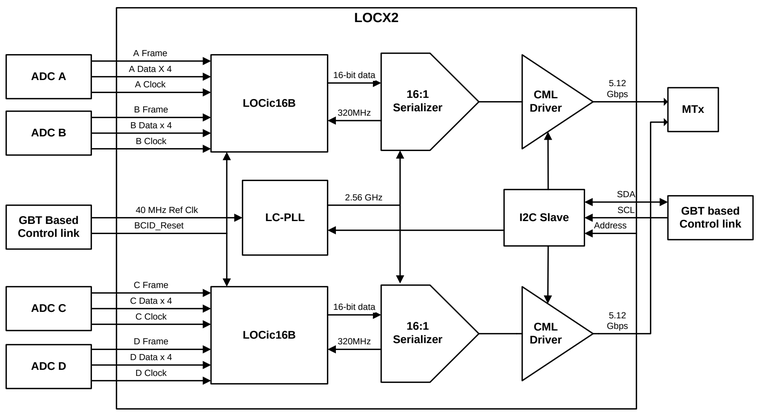


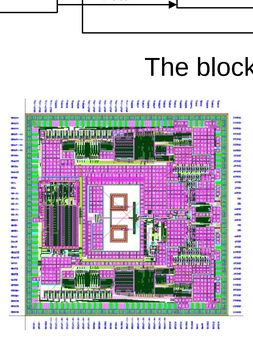

The block diagram of the optical link in ATLAS LAr trigger phase-I update

- The ATLAS Liquid Argon calorimeter (LAr) Phase-I trigger upgrade calls for a data transmission rate of 204.8 Gbps for each front-end board (LTDB) [1].
- The optical link on the transmitter side consists of a transmitter ASIC LOCx2 and a custom optical transmitter module MTx.
- LOCx2 is a two-channal transmitter ASIC. Each channel receives data from the upstream ADCs [2], encodes the data, and outputs them in serial at a speed of 5.12Gbps.
- The transmitter ASIC is fabricated in a commercial 0.25-μm Silicon-on-Sapphire CMOS technology for radiation-tolerance.
- The latency budget of the optical link is 150 ns.
- The power consumption budget of the transmitter ASIC is 1 W.

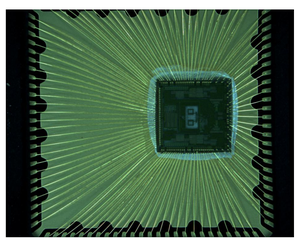
## The design of AISC



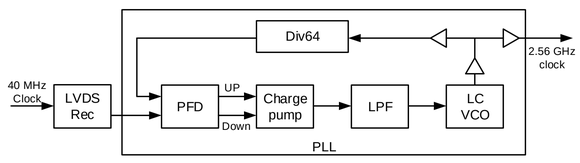

The block diagram of LOCx2 ASIC



Layout of the LOCx2 ASIC

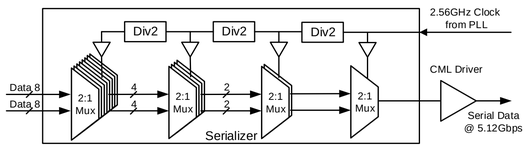


QFN packaged LOCx2 ASIC



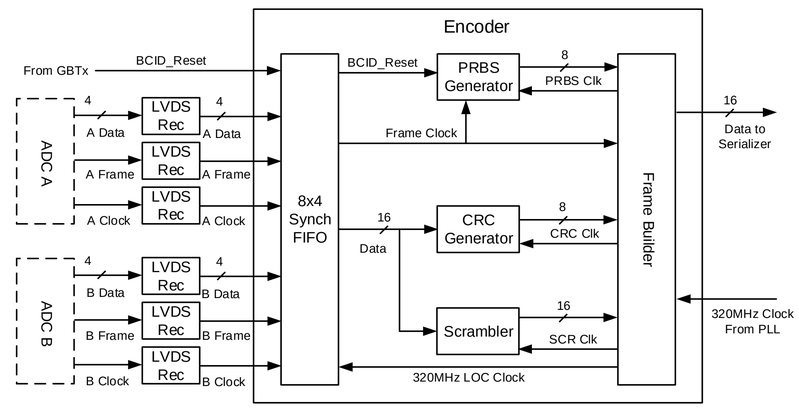

The block diagram of PLL

- The PLL has four tuning frequency bands selected through the I2C interface. The tuning range of LC-VCO is from 1.86 GHz to 2.98 GHz at the nominal process corner and 55 °C.
- Both the bandwidth of the LPF and the charge pump current are programmable, thus the loop bandwidth of the PLL is programmable from 0.5 to 2.5 MHz.




The block diagram of serializer

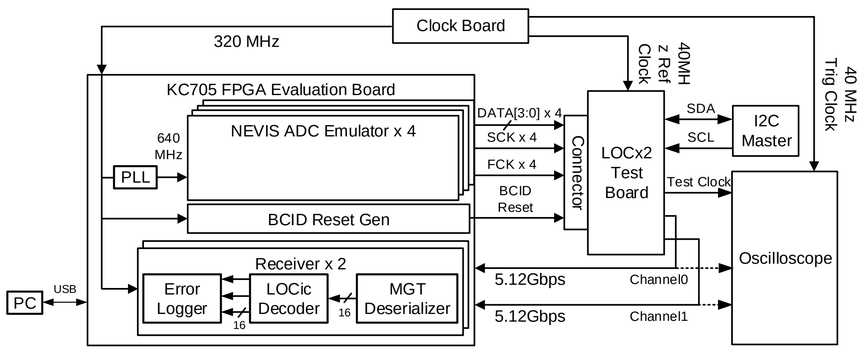
- Each Serializer unit consists of 4 stages of 2:1 multiplexers in a binary tree structure. All 2:1 multiplexer are based on static CMOS D flip flops for single-event effect (SEE) immunity.



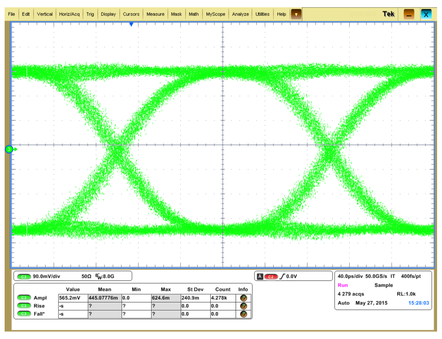

The block diagram of LOCic encoder

- The ASIC uses a custom line code called LOCic [3].
- Each frame consists of 128 bits, including 8-bit frame header, 112-bit payload and 8-bit frame trailer.
- The payload is scrambled before transmitted, whereas the frame header and trailer are not scrambled.
- 12-bit BCID information is embedded in the frame header automatically.
- The overhead is 14.3% (= 16/112).

## The test system and measurement results




The block diagram of test setup



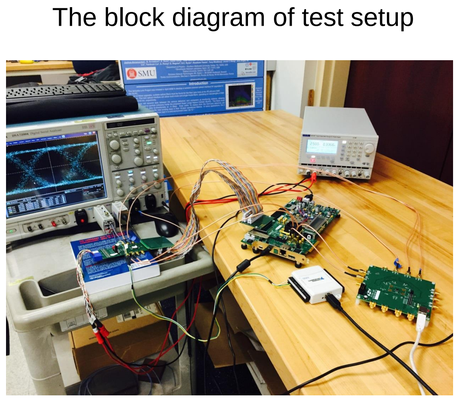
The eye diagram of LOCx2 output at 5.12Gbps

| Function block | | Latency (ns) |
|---|---|---|
| TX | FIFO | 8.4-11.6 |
| | Scrambler & CRC gen | 6.25 |
| | Frame Builder | 3.125 |
| | Serializer | 6.25 |
| | Total LOCx2 | 24.0-27.2 |
| RX | Deserializer | 28.5-31.4 |
| | Data Extractor | 9.4 |
| | Descrambler | 3.1 |
| | CRC Check | 3.1 |
| | Total FPGA | 44.1-47.0 |
| **Total optical link** | | 68.1-74.2 |

Simulation

Measurement

Latency of the optical link



A picture of test setup

| | |
|---|---|
| PLL turning range | 2.0-3.1 GHz |
| PLL random jitter | 1 ps (RMS) |
| Serial date output rise time | 70 ps |
| Serial date output fall time | 64 ps |
| Serial date output deterministic jitter | 28 ps |
| Serial date output random jitter | 1.5 ps (RMS) |
| Serial date output total jitter | 42 ps (peak-peak) |
| Serial date output amplitude | 445mV (peak-peak) |
| Serial date output BER | < $10^{-12}$ |

PLL and LOCx2 output measurment

| Functional blocks | Power consumption (mW) |
|---|---|
| LC-PLL | 52.5 |
| LOCic | 192.5 |
| Serializer | 350.0 |
| CML Driver | 150.0 |
| Clock Buffers | 22.5 |
| SLVS Receivers | 75.0 |
| Total | 842.5 |

Power consumption of LOCx2 chip

## Conclusion and outlook

- An transmitter ASIC, LOCx2, is designed and tested for the ATLAS LAr Calorimeter trigger upgrade.
- LOCx2 consists of two channels and each channel encodes ADC data with an overhead of 14.3% and transmits serial data at 5.12 Gbps with a latency of less than 27.2 ns. The power consumption of the transmitter is 842.5 mW.
- The next version will interface with both ASIC and COST ADCs

## Acknowledgments


This work is supported by US-ATLAS R&D program for the upgrade of the LHC, the US Department of Energy Grant DE-FG02-04ER1299. We are grateful to Drs. Hucheng Chen and Hao Xu of Brookhaven National Laboratory for help on test and firmware development, Dr. Nicolas Dumont Dayot of LAPP for discussion on decoder implement.


## References


[1] ATLAS Collaboration, *ATLAS liquid argon calorimeter Phase-I upgrade technical design report*, CERN-LHCC-2013-017 and ATLAS-TDR-022, September 20, 2013.
[2] J. Kuppambatti, et al, A radiation-hard dual channel 4-bit pipeline for a 12-bit 40 MS/s ADC prototype with extended dynamic range for the ATLAS Liquid Argon Calorimeter readout electronics upgrade at the CERN LHC, 2013 JINST 8 P09008
[3] B. Deng, et al, *A line code with quick-resynchronization capability and low latency for the optical data links of LHC experiments*, 2014 JINST 9 P07020

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