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LOCx2, a low-latency, low-overhead, 2 × 5.12-Gbps serializer ASIC for the ATLAS Liquid Argon Calorimeter trigger upgrade

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We present the design and test results of LOCx2, a high-speed serializer ASIC for detector readout in the ATLAS Liquid Argon Calorimeter trigger upgrade. LOCx2 consists of two channels. Each encodes the ADC data with an overhead of 12.5% and transmits serial data at 5.12 Gbps. The ASIC is fabricated with a commercial 0.25-μm Silicon-on-Sapphire CMOS technology and is packaged using QFN100. LOCx2 consumes 850mW of power and achieves less than 10-12 bit error rate with a latency of less than 38 ns.

Summary

The ATLAS Liquid Argon Calorimeter (LAr) trigger upgrade requires high-speed, low-power and low-latency data transmission. Each LAr Trigger Digitizing Board calls for a data rate of 204.8 Gbps transmitted over 40 optical fibers to the back-end. The latency of the data link needs to meet the L1 trigger timing requirement for the upgrade. Based on a commercial 0.25-μm Silicon-on-Sapphire (SoS) CMOS technology, we have designed a dual-channel serializer ASIC LOCx2 for this upgrade. Each channel of LOCx2, including a low-latency, low-overhead custom data encoder and a high-speed serializer, transmits data of two 12-bit 40 MSPS NEVIS ADC at 5.12 Gbps. Two data channels share an LC-tank based PLL and an I2C controller.

The encoder receives the data from the upstream ADCs to form data frames. The data frame has 112-bit scrambled ADC data, 8-bit Cyclic Redundant Code (CRC) and 8-bit frame header. The 112-bit user data accommodates 8 ADC channels from two 4-channel ADC chips with serial outputs. The 8-bit CRC can detect up to 3 bit flips in any data frame. The 8-bit frame header, used to identify the frame boundary, includes 4-bit fixed code “1010” and 4-bit Pseudo-Random Binary Sequence (PRBS) code. By combining the PRBS code from the previous received data frames, the decoder on the link receive-side can extract the 12-bit Bunch-Crossing Identification (BCID) information. The encoder operates at 320 MHz clock frequency.

The serializer implements 16:1 multiplexing and operates at 5.12 Gbps. The serializer includes 4 stages of 2:1 multiplexers in a binary tree structure and an output line driver. All of the 2:1 multiplexers are designed using static CMOS D-flip-flops. A Current-Mode Logic (CML) driver with 50-Ω output impedance is used to output the data to the optical module.

The LC-PLL is optimized at 2.56 GHz, corresponding to the serializer data rate. The turning range of the VCO is from 1.86 GHz to 2.98 GHz with digital coarse band selection. The PLL charge pump current and loop bandwidth are programmable from 0.5 to 2.5 MHz through an I2C interface.

LOCx2 has been fully evaluated. The power consumption of the whole serializer is 0.85 W. In the link test, the receiver implemented in Kintex 7 FPGA identifies the date frame boundary correctly and the frame data passes the CRC check. The BCID count is extracted as expected. The output of the serializer passes the eye mask test with bit error rate below 10-12. The latency of the link, including the receiver and the serializer, is from 68.9 to 75.3 ns and the chip latency is less than 38 ns. As expected, the serializer tolerates 3.125 ns clock skew between two input ADC chips. Irradiate tests will be carried out in the coming months.

Primary authors: GONG, Datao (Southern Methodist Univeristy); Mr XIAO, Le (Department of Physics, Central China Normal University); LI, Xiaoting (Central China Normal University, Southern Methodist University)

Co-authors: Mr VOSOOGHI, Bozorgmehr (Department of Electrical and Computer Engineering, University of Houston); LIU, Chonghan (S); GUO, Di (University of Science and Technology of China); YE, Jingbo (Southern Methodist University, Department of Physics); TENG, Ping-Kun (Academia Sinica); HOU, Suen (Academia Sinica (TW)); LIU, Tiankuan (Southern Methodist University); SUN, Xiangming (Lawrence Berkeley National Lab. (US)); XIANG, annie (Southern Methodist University); Prof. HUANG, guangming (Department of Physics, Central China Normal University); Ms HE, huiqin (Industrial Training Center, Shenzhen Polytechnic); Prof. CHEN, jinghong (Department of Electrical and Computer Engineering, University of Houston); YOU, yang (Southern Methodist University)

Presenter: GONG, Datao (Southern Methodist Univeristy)

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