GEMMA and GEMINI, two dedicated mixed-signal ASICs for Triple-GEM detectors readout

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Abstract

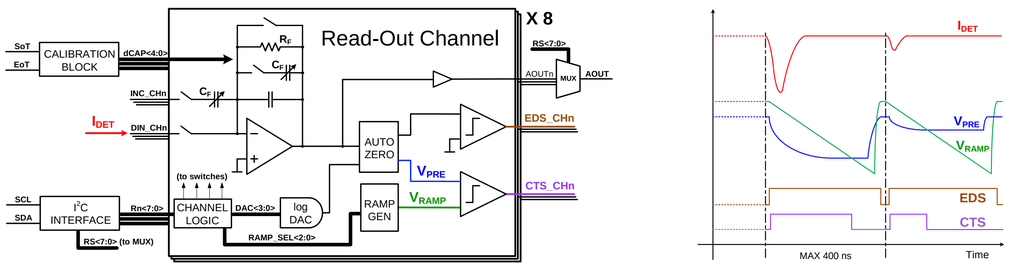
GEMMA and GEMINI, two integrated frontends for the Triple-GEM detector are presented. The ASICs aim to improve detector readout performance in terms of count rate, adaptability, portability and power consumption. GEMMA target is to embed counting, timing and spectroscopic measurements in a single 8-channel device, managing a detector capacitance up to 15 pF. GEMINI is dedicated to counting measurements, embedding 16 channels with a detector capacitance up to 40 pF. Both prototypes, fabricated in 130 nm and 180 nm CMOS respectively, feature an automatic on-chip calibration circuit, compensating for process/temperature variations.

GEMMA (GEM Mixed-signal Asic)

Target

- Performing Timing and Charge Measurements with 8 Channels
- Including post-processing elaboration on-chip
- Improving count rate, noise performance and system portability with a low-power approach
- Managing up to 15 pF detector pixel capacitance

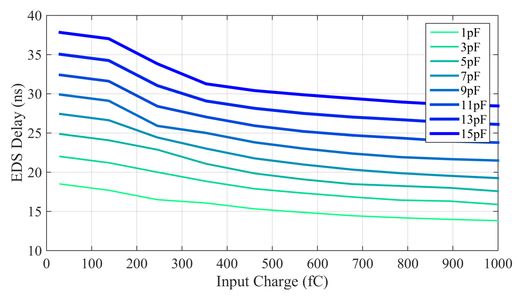
Block Scheme



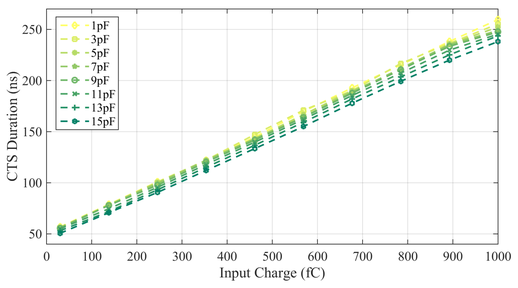
Overall Structure

- Two Digital Outputs: Event-Detection Signal (EDS) and Charge-Time Signal (CTS)
- One Analog Output: Preamplifier Output Signal, selectable among the 8 channels
- Charge-Sensitive Preamplifier based on 3-stage Nested-Miller-Feedforward Opamp architecture
- Automatic calibration of capacitances, compensating for process and environmental variations
- Comparators based on mirrored structure and Auto-Zero block to optimize performance
- 3-bit Log Resistive Ladder DAC to set the threshold
- I^2C interface for channel settings and a Logic Unit to control ramp slope, threshold and reset

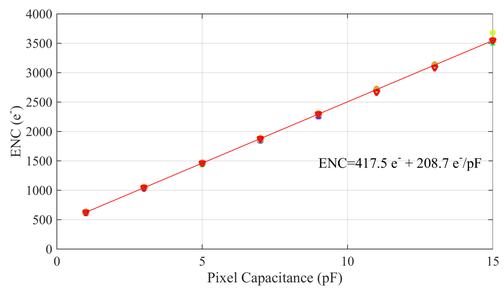
EDS Delay vs. Input Charge



CTS Duration vs. Input Charge

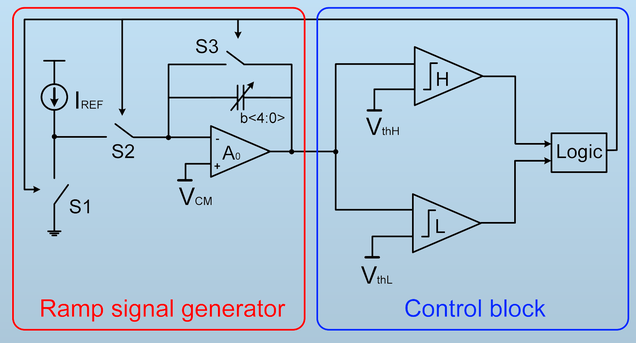


ENC vs. Pixel Capacitance

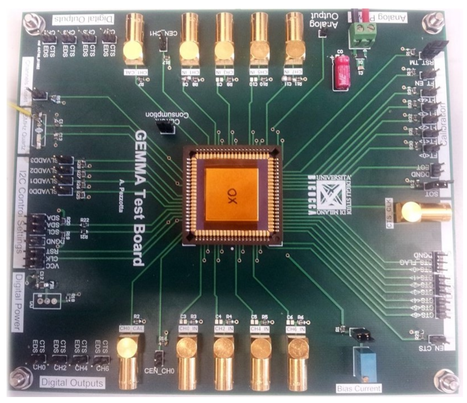


Automatic Calibration System

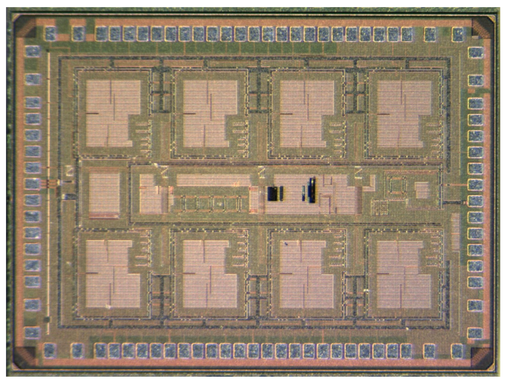
- CMOS fabrication process leads to capacitors value spread, reaching 40% w.r.t. nominal value
- Binary-weighted capacitor arrays included, with a tuning algorithm
- Sets the precision of sensitivity up to 5% w.r.t. nominal value



Test Board



Chip Photo & Performance Resume



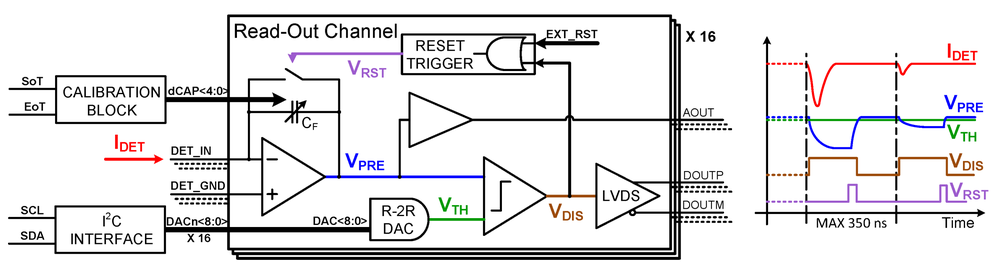
Parameter	Value
CMOS Technology	130 nm
Supply Voltage	1.8 V
Channel Number	8
Input Parasitic Capacitance	15 pF
Maximum Count Rate	$4{\cdot}10^6$ cps
Area	4.67 mm^2
Power Consumption	3.8 mW/ch.

GEMINI (GEM INtegrated Interface)

Target

- Devoted to Counting/Time-of-Flight Measurements with 16 compact-structure channels
- High-resolution thresholds setting
- Event-Triggered Reset, with no Logic Units inside the channels preventing clock couplings
- Managing up to 40 pF detector pixel capacitance

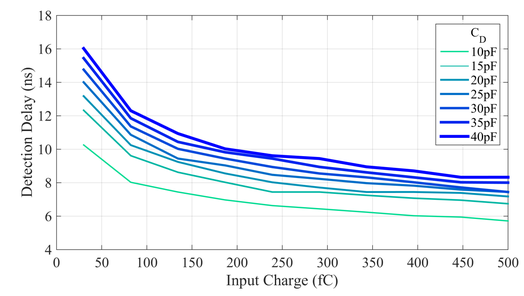
Block Scheme



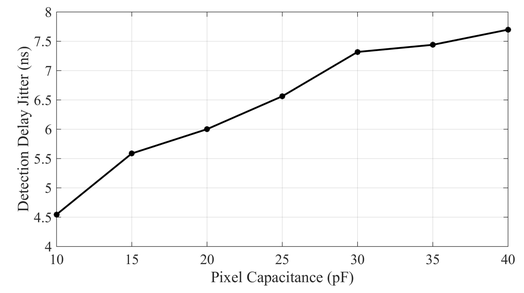
Overall Structure

- One Digital Output: LVDS Event-Detection Signal (EDS) for Time measurements
- One Analog Output: Preamplifier Output Signal (all channels in parallel)
- Charge-Sensitive Preamplifier with no feedback resistor, based on a 2-stage Miller Opamp
- Automatic calibration of capacitances, compensating for Process and Environmental variations
- Comparators based on mirrored structure, optimizing offset performance
- 9-bit Resistive R-2R DAC to set threshold, managed via the I^2C interface
- Reset Signal generated from the Digital Output

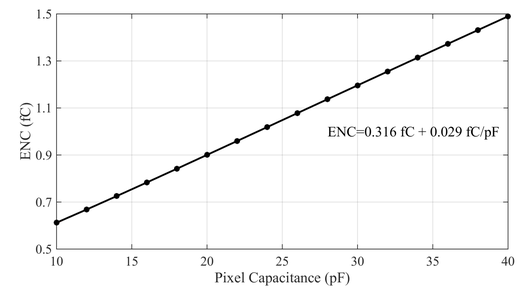
Detection Delay vs. Input Charge



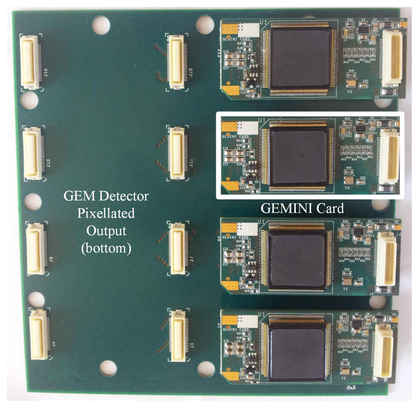
Detection Jitter vs. Pixel Capacitance



ENC vs. Pixel Capacitance



Readout System



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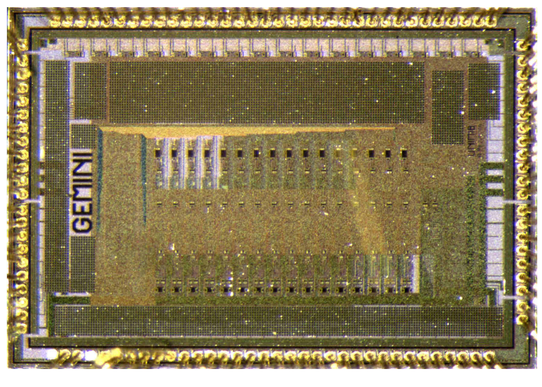

Parameter	Value
CMOS Technology	180 nm
Supply Voltage	2 V
Channel Number	16
Input Parasitic Capacitance	40 pF
Maximum Count Rate	5 Mcps
Area	6.74 mm^2
Power Consumption	2.7 mW/ch.

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