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GEMMA and GEMINI, two dedicated mixed-signal ASICs for Triple-GEM detectors readout

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GEMMA and GEMINI, two integrated frontends for the Triple-GEM detector are presented. The ASICs aim to improve detector readout performance in terms of count rate, adaptability, portability and power consumption. GEMMA target is to embed counting, timing and spectroscopic measurements in a single 8-channel device, managing a detector capacitance up to 15pF. GEMINI is dedicated to counting measurements, embedding 16 channels with a detector capacitance up to 40pF. Both prototypes, fabricated in 130nm and 180nm CMOS respectively, feature an automatic on-chip calibration circuit, compensating for process/temperature variations.

Summary

One of the most active research branches in GEM detectors is frontend performance improvement, employing dedicated CMOS integrated solutions, suitable to sustain overall count rate while reducing power consumption, and at the same time increasing system portability. In fact, the development of an ASIC can afford several advantages with respect to other common solutions, i.e. PCBs. For instance, the inclusion of a digital-based data elaboration can greatly increase performance reducing the overall readout system complexity, limiting the necessity of off-chip devices like FPGAs or standard microcontrollers. Then, silicon implementation allows dedicated circuital/system-level choices, optimizing the system to cope with detector performance. Improvement in portability are also crucial, since the detector pixelated output includes hundreds of pads, manufactured in different size factors. These represent a primary issue in readout design, in terms of noise and efficiency.

In this scenario, two prototypes with different targets have been developed.

The aim of GEMMA (GEM Mixed-signal Asic) is to measure the arrival time and the amount of charge from the Triple-GEM detector. It composes of 8 detecting channels including a Charge Sensitive Preamplifier (CSP) and a Charge-Time Converter (CTC). It is able to manage up to 15pF of pixel parasitic capacitance. The embedded calibration system tunes all channels' CSP feedback capacitances, to match the target sensitivity of 0.5mV/fC within a 5% tolerance. The CTC converts the CSP output voltage signal into digital domain. In detail, the CTC gets the CSP output and generates two logic output signals. The first, named Charge-Time Signal (CTS), includes information into its time duration, directly proportional to the input charge. The second, named Event Detection Signal (EDS) gives information about the arrival time of the incident particle. In channel 6, for prototyping concern, the CTS is also converted into a 7-bit digital word by a 250MHz clocked counter (the clock is off-chip). In order to control and stabilize comparators performance, an effective circuital block named Auto-Zero acts as an adjustable level shifter for the CSP output signal, adapting it separately for the two comparators. The shifting is set by a 4-bit logarithmic DAC, representing the actual channel threshold for measurements. The device is able to sustain a count rate up to 4Mcps consuming 3.8mW/ch.

On the other hand, GEMINI (GEM INtegrated Interface) target application includes time-of-flight and counting measurements, with the option to make spectroscopic analysis externally via the analog preamplifier output. The GEMINI has a mixed signal capability, with analog and digital outputs available in parallel for each one of the 16 channels included, also with automatic on chip calibration acting on channel capacitors, keeping performance constant against CMOS process, supply voltage and environmental variations. This allows managing a count rate up to 5Mcps and an input pad capacitance up to 40pF, while consuming 2.7mW/ch. As a

whole, GEMINI channels include a charge-sensitive preamplifier (CSP) with a sensitivity of 1mV/fC. Then, a discriminator (DISC) with a channel-specific threshold set by a 9 bit R-2R Resistive DAC, generates the Event Detection Signal (EDS), then converted to LVDS. The CSP composes of a Class-A Miller Opamp with a capacitor and a switch in parallel connected in feedback. The reset generation is event triggered, without the inclusion of a clock signal.

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