Transmission Lines Implementation on HDI Flex Circuits for the CMS Tracker Upgrade

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Abstract

The upgrade of the CMS tracker at the HL-LHC relies on hybrid modules build on high density interconnecting flexible circuits. These hybrids contain several flip chip readout ASICs having high speed digital ports required for configuration and data readout, implemented as SLVS differential pairs. This paper presents the connectivity requirements on the CMS tracker hybrids; it compares several transmission line implementations in terms of board area, achievable impedances and expected crosstalk. The properties obtained by means of simulations are compared with measurements made on a dedicated test circuit. The different transmission line implementations are also tested using a custom 65nm SLVS driver and receiver prototype ASIC.

Introduction to the CMS tracker upgrade for the HL-LHC

The planned luminosity of the High Luminosity LHC (HL-LHC) requires a major upgrade of the CMS detector in order to meet the new requirements. New modules being developed featuring higher granularity, lower mass and capability for the high data rate as a result of the increased luminosity. The new electronics introduce the ability to correlate locally the signals from a pair of silicon sensors to enable the rejection of low momentum tracks. At the same time a new level 1 (L1) track triggering functionality is implemented to reduce the L1 trigger rate.

The upgraded tracker is made of a barrel and endcap geometry with two different module types and sensor separations dependent on the installation region. One module type consists of two silicon strip sensors (2S module) with a separation of 1-4mm depending on the radial position. The other module type consist of a silicon strip sensor (PS module) and a pixelated strip sensor to provide additional Z axis information for the track triggering functionality.

The 2S modules will contain the CBC3 flip chip ASICs currently under development for the hybrids. Flip chip dies allow for a significant size reduction and have less inductive parasitic compared to wire bonded dies, but they impose the use of High Density Interconnection (HDI) technology on the front-end hybrids.

Modules, front-end hybrids and IO requirements

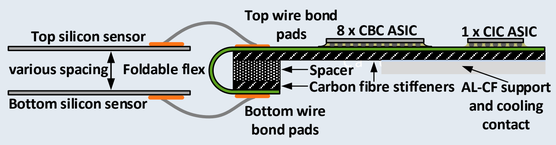

Fig.1: 2S module cross section view at fold-over

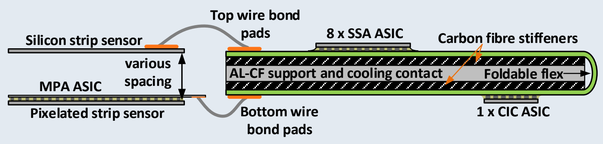

Fig.2: PS module cross section view at fold-over

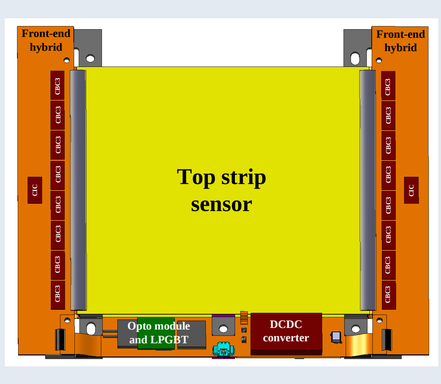

Fig.3: 3D view of 2S module assembly design.

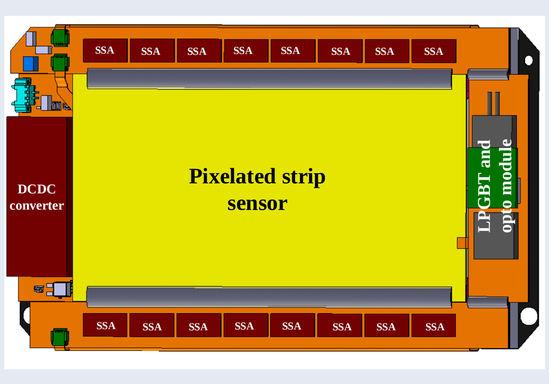

Fig.4: 3D view of PS module assembly design.

Each module type contains two front-end hybrids to interconnect the silicon sensors with the read out ASICs. In order to adjust the wire bonding level to obtain the shortest wire bond length the hybrids are folded (figure 1, figure 2). To keep the circuits sufficiently flexible at the fold-over areas and to achieve the lightest circuit the dielectric thickness is reduced as much as possible. The input-output signaling of the front-end ASICs is implemented in custom SLVS differential drivers and receivers operated at 320Mbps. To reduce the power consumption of the corresponding line drivers the target characteristic impedance of the differential traces is set to 100 Ω. Due to the thin dielectric thickness and the circuit manufacturer design rules it is very difficult to obtain the desired impedance values.

The front-end ASICs on the 2S module are using six differential signal traces per chip to send the trigger and L1 data to the Concentrator ASIC (CIC) which forwards the conditioned data to the Low Power Gigabit Transmitter (LPGBT) using four differential signals for downlink and seven for uplink communication (figure 5). The 2S hybrid has to host all together 62 differential signal traces (up to 320 Mbps) and 5 single-ended traces.

For what concerns the PS module hybrids, the Short Strips ASIC (SSA) on the PS module hybrid is designed to read, serialize and send the uncorrelated data from the silicon strip sensors. The SSA uses two differential signal lines to transmit its data to the Macro Pixel ASIC (MPA) chip. The MPA will correlate the SSA data with the pixelated silicon strip sensor signals where it is bump bonded to. The correlated data is forwarded to the CIC ASIC using 12 differential signal traces (figure 6). The PS hybrid all together has to host 80 differential traces (up to 320 Mbps) and 3 single-ended traces for slow control and reset.

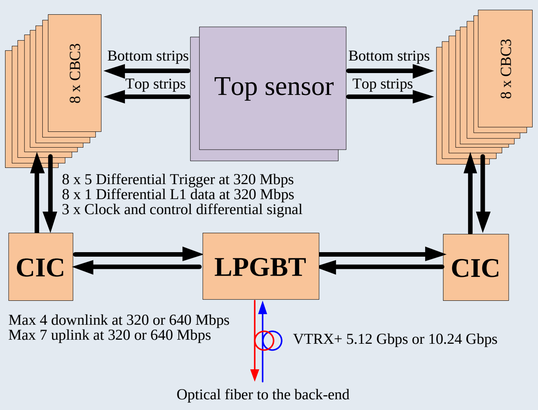

Fig.5: 2S module data flow architecture

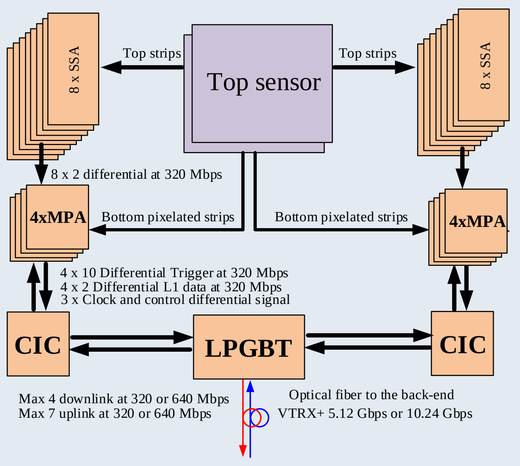

Fig.6: PS module data flow architecture

Possible buildup topologies using four layers

The low mass requirement and the very demanding feature size of the hybrids are setting a four layers build-up arrangement. Considering the need for one ground plane and one power plane, few varieties of differential pair geometries can be implemented, while preserving the copper area of the build up to stay symmetric (figure 7). All of these traces have different properties that we have to consider during the design of the hybrids.

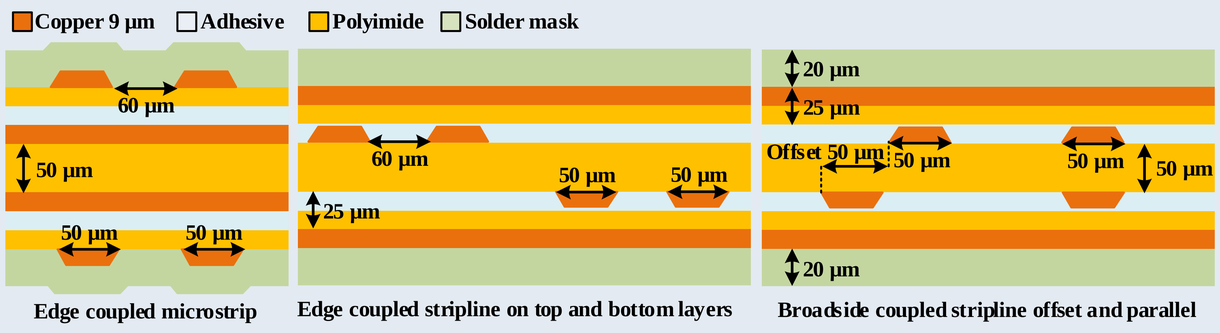

Fig.7: Possible differential pair topologies using four layers buildup

Edge coupled microstrip: This differential pair geometry couples to one plane layer, leading to higher impedance when compared to the other topologies shown here. The pairs are not shielded from the circuit environment, therefore more noise can be emitted and the traces are more noise sensitive. A careful design is needed to avoid signal integrity and EMC problems.

Edge coupled stripline: This geometry is coupled to two plane layers leading to a lower impedance when compared to the microstrip geometry. The signal traces are well shielded, however a large spacing between parallel pairs is required to avoid significant cross talk. This results in a worse routing efficiency of the circuit.

Broadside coupled striplines: This geometry implements differential pairs vertically through two routing layers, themselves coupled to two plane layers. The traces are strongly coupled and therefore a much lower impedance is expected when compared to the other geometries. The layer usage of this geometry is excellent and the copper area of the layers is symmetric. The impedance can be artificially increased by applying an offset between the two tracks of the pair, compromising however the routing layer usage. Due to the strong coupling and to the presence of external shield layers, this geometry has good noise rejection.

Impedance calculations

Due to the very small feature size and the very thin dielectric used in the hybrids, the calculators based on IPC equations are not providing accurate results. To estimate precisely the impedance values a 3D field solver is required. The Ansys Siwave field solver and the Polar Instruments 9000E field solver based calculator were used to carry out the calculations. These different tools provided different results for a given geometry (Table 1). A test board was then designed and measured to validate the simulation results.

Simulator	Edge coupled microstrip	Edge coupled stripline	Broadside coupled stripline	Broadside coupl. Stripline offset
IPC Equations	83 Ω	100 Ω	27 Ω	-
Polar SI 9000	92 Ω	71 Ω	58 Ω	62 Ω
Ansys SiWave	88 Ω	80 Ω	69 Ω	76 Ω

Table 1: Impedance simulation results

Multi purpose impedance test board

An impedance test board was designed to measure the simulated differential pair geometries and test a custom SLVS driver designed for the SSA and MPA chips. The test board consists of the four differential pair geometries illustrated on figure 7, routed in two different lengths (6.7 cm and 12.7 cm). Each pair can be driven by one SLVS driver ASIC and is received by another one on the opposed side (figure 9). Micro coaxial connectors are placed at the beginning and at the end of the lines to enable probing the signals.

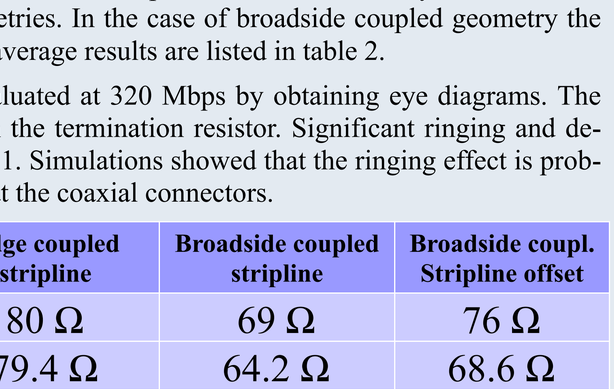

Fig.8: Picture of the assembled impedance test board

Crosstalk pick up lines are also routed next to every pair, terminated on both ends and fitted with micro coaxial probe ports, in order to compare the EMC emissions and risk of crosstalk of the tested topologies.

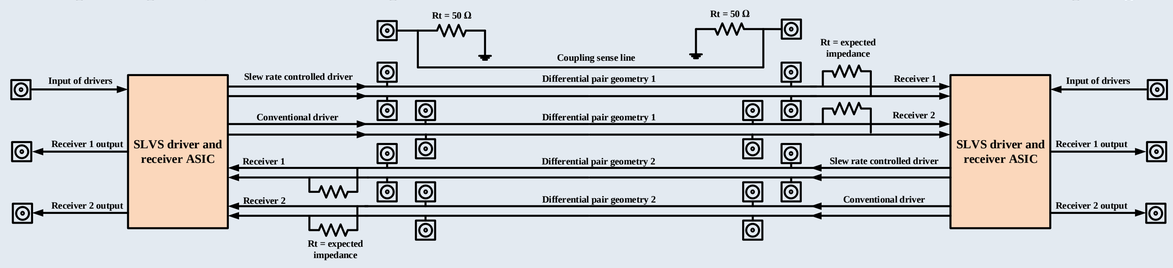

Fig.9: Schematic diagram of one test block of the impedance test board.

Impedance and driver measurements

A Vector network Analyzer was used to obtain the S parameters of the differential transmission lines. The measured S parameters were transformed to time domain and the resistivity of the lines was compensated. The average value of the measurement is well in line with the expected value obtained by SiWave in the case of edge coupled microstrip and stripline geometries. In the case of broadside coupled geometry the values are lower than the expected impedance. The average results are listed in table 2.

The performance of the SLVS drivers was also evaluated at 320 Mbps by obtaining eye diagrams. The eye diagram was measured close to the receiver on the termination resistor. Significant ringing and degraded eye crossing percentage is visible on figure 11. Simulations showed that the ringing effect is probably due to the stray capacitance of the solder pads at the coaxial connectors.

	Edge coupled microstrip	Edge coupled stripline	Broadside coupled stripline	Broadside coupl. Stripline offset
Expected from Siwave	88 Ω	80 Ω	69 Ω	76 Ω
Measurement results	86.9 Ω	79.4 Ω	64.2 Ω	68.6 Ω

Table 2: Average impedance values calculated from measurement

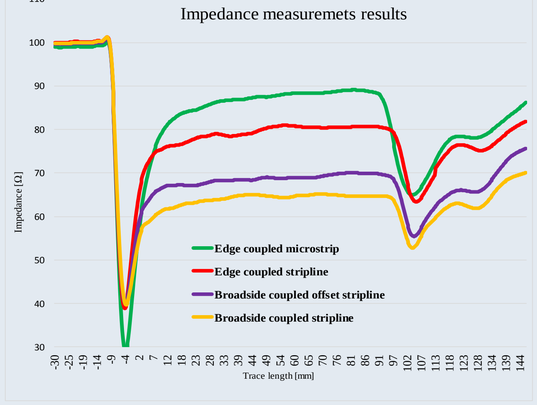

Fig.10: Impedance plot obtained from VNA measurement

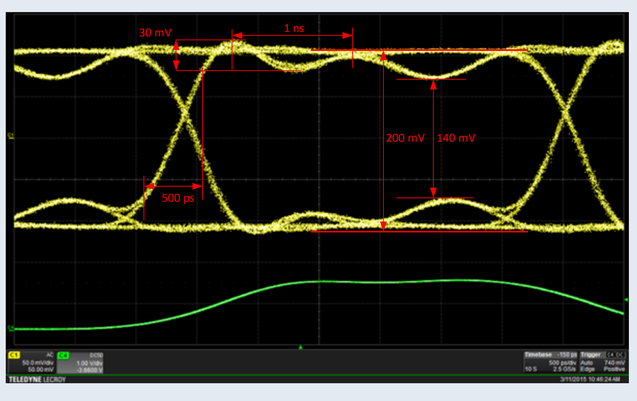

Fig.11: Eye diagram measured on R_t of conventional drove edge coupled stripline

Conclusions

The planned upgrade of the CMS detector requires the development of new hybrid circuits. The hybrids are using the latest circuit manufacturing processes, therefore limited amount of information was available about the electrical performance. An impedance test board was created to measure the properties of differential transmission lines and a custom SLVS driver. The measured impedance values were in line with previous simulations carried out using 3D field solver tools. The performance of the SLVS drivers was also measured and signal quality problems were identified. A new ASIC was designed and it will be tested with an improved test board.