Prototyping of an HV-CMOS demonstrator for the High Luminosity-LHC upgrade

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on behalf of the collaboration between
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Outline

1. Introduction
2. Demonstrator floorplan and main features
3. In-pixel schematics and layouts
4. Simulations
5. Digital block
6. Conclusion and future plans

Introduction

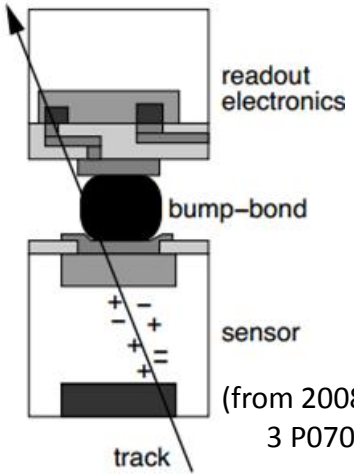
- We are developing **HV-CMOS sensors** to be used as a replacement of the **standard planar detectors** in the High Luminosity-LHC ATLAS upgrade.

Standard planar detectors:

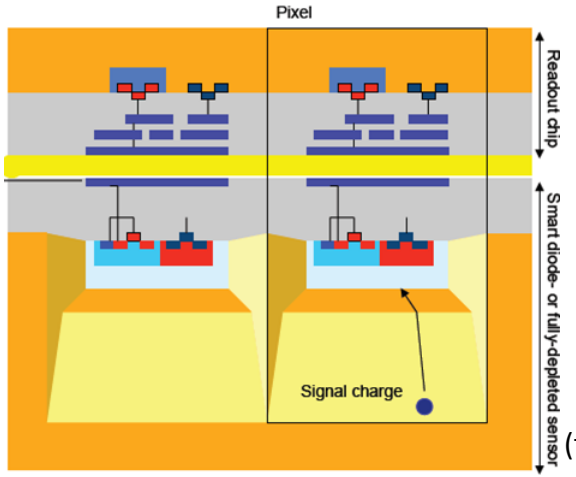
- Good radiation tolerance
- Dedicated process
- Expensive
- Complicated chip-to-chip connection
- Large amount of material

HV-CMOS sensors:

- Commercial technologies
- Small cell areas with amplification
- Low-cost & Reduced thickness
- Radiation hardness after HL-LHC levels needs to be confirmed



(from 2008 JINST 3 P07007)

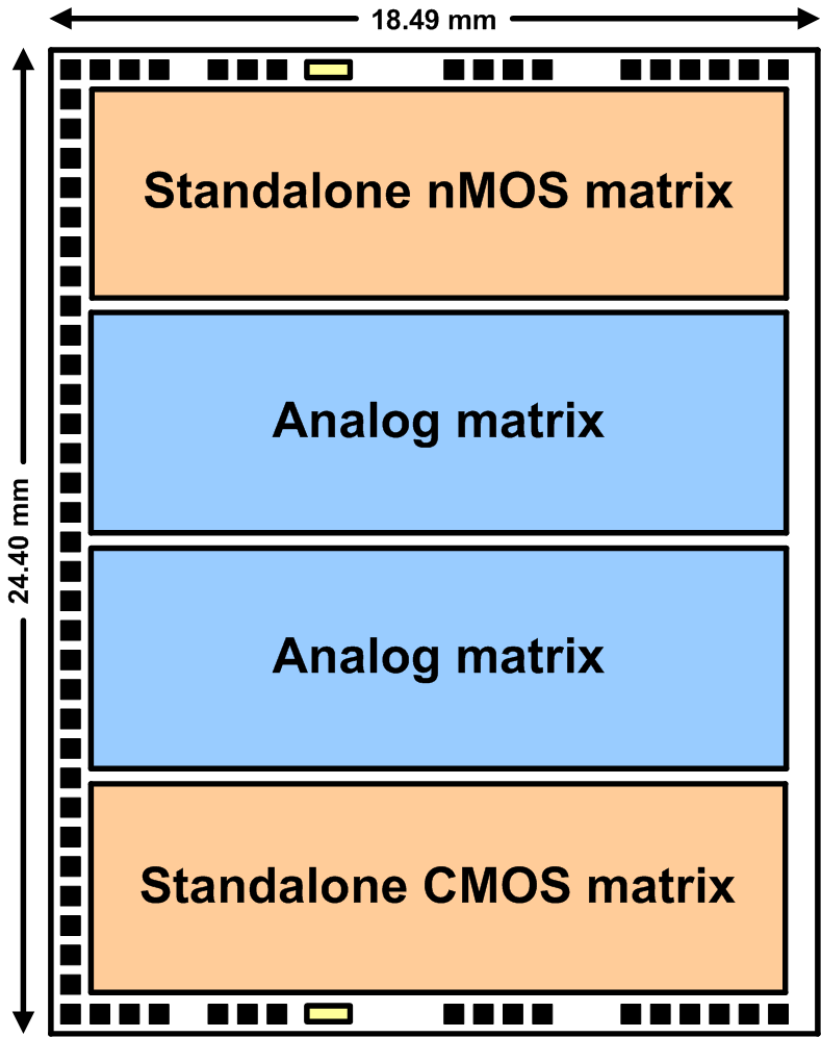


(from I. Peric)

Introduction

- Research on HV-CMOS sensors was started by I. Peric in 2006.
- **Several prototypes** have been fabricated in **different standard technologies**.
  - AMS-H35, AMS-H18 and UMC 65 nm LV.
  - Also developments in ESPROS, LFoundry, STM, TowerJazz, X-FAB…
- **Different sensor features** have been explored.
  - Different pixel sizes, electronics and readout type.
- **Different application fields** are considered.
  - ATLAS pixels/strips, CLIC, Mu3e experiment and Transmission Electron Microscopy.
- HV-CMOS sensors have demonstrated to be a **feasible candidate** for the HL-LHC upgrade.
- However…
  - The resistivity of the substrate is low (20 Ω·cm), which leads low SNR.
  - The depletion region is around 15 µm and MIP signals are weak.
  - Crosstalk.

H35DEMO - Floorplan



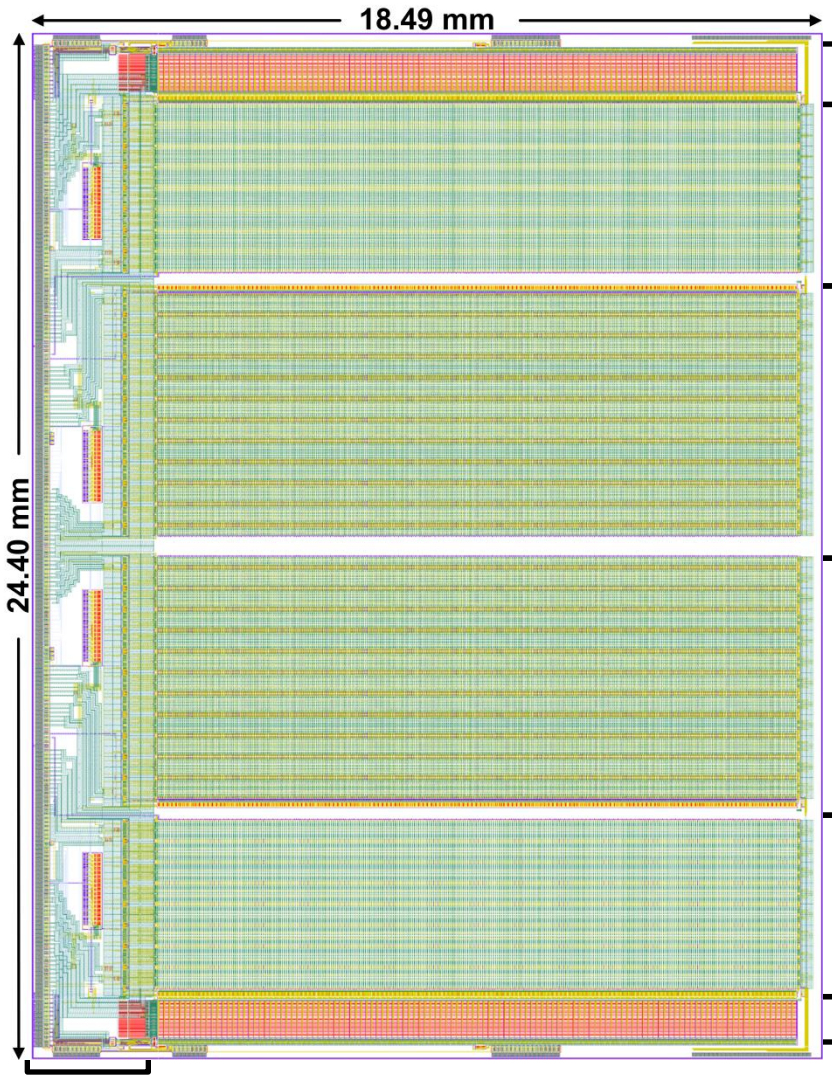
Main features:

- ams 0.35 µm High-Voltage CMOS (H35)
- submission through an engineering run
  - submission in September 2015
- different substrate resistivities to improve SNR
  - 20 Ω·cm (standard), 80 Ω·cm, 200 Ω·cm, 1k Ω·cm

Areas (from top to bottom):

- standalone nMOS matrix
  - digital pixels with in-pixel nMOS comparator
  - standalone readout
- analog matrix (2 identical arrays)
  - different flavours in terms of gain and speed
- standalone CMOS matrix
  - analog pixels with off-pixel CMOS comparator
  - standalone readout

H35DEMO - Layout



← digital and control circuits (15 mm x 1.45 mm)

← 16 rows x 300 cols **standalone nMOS matrix** (15 mm x 4 mm)

← 500 µm gap (it includes config. reg.)

← 23 rows x 300 cols **analog matrix** (15 mm x 5.9 mm)

← 500 µm gap

← 23 rows x 300 cols **analog matrix** (15 mm x 5.9 mm)

← 500 µm gap (it includes config. reg.)

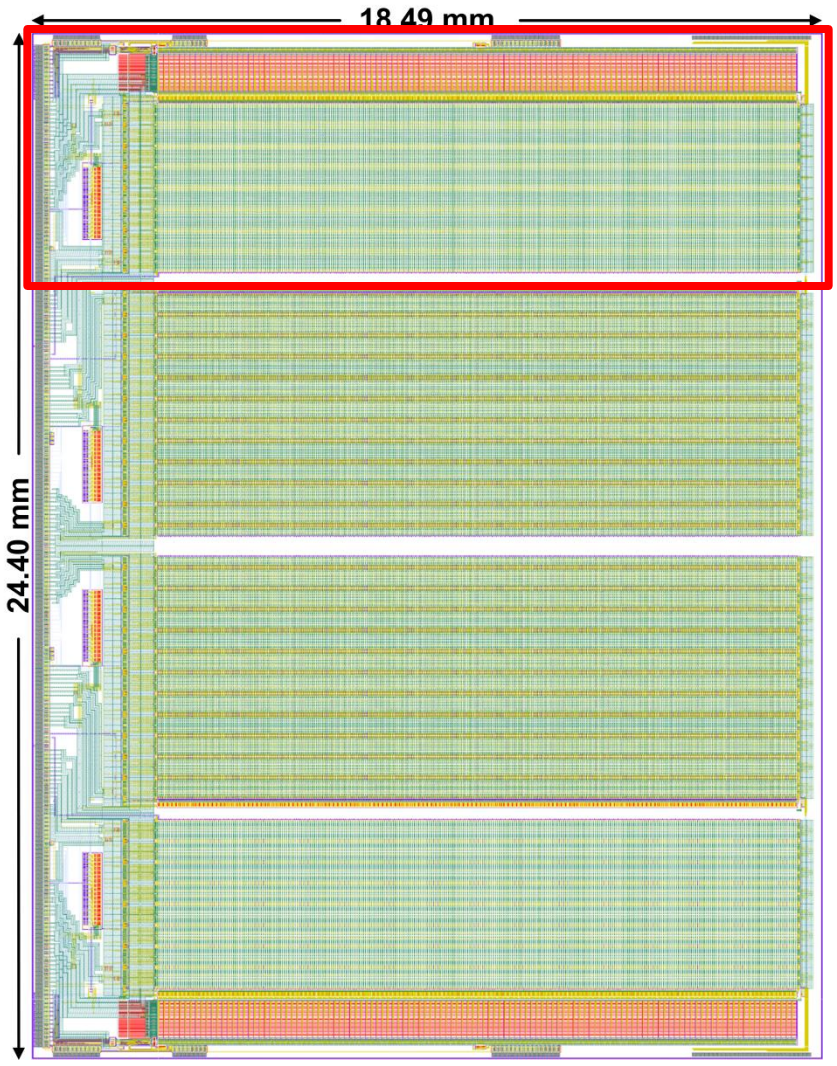
← 16 rows x 300 cols **standalone CMOS matrix** (15 mm x 4 mm)

← digital and control circuits (15 mm x 1.45 mm)

← Pads and bias blocks (2.97 mm x 24.40 mm)

Each matrix has its own pads and bias block

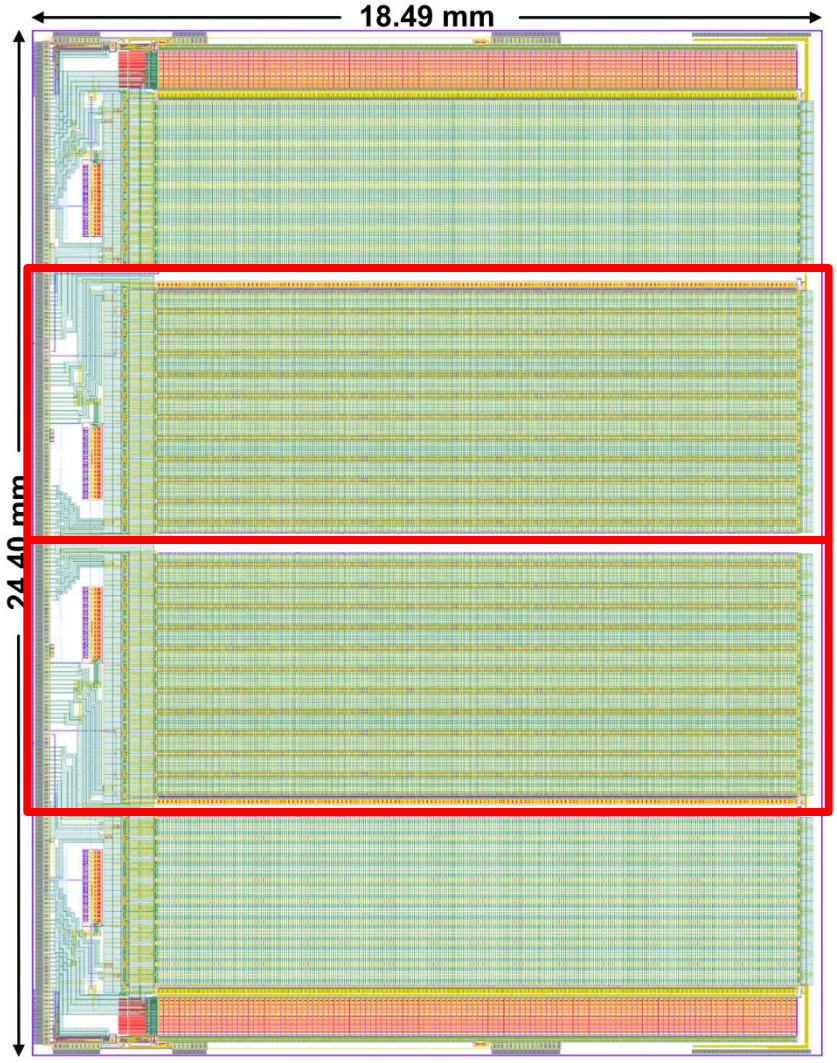
H35DEMO - Features



Standalone nMOS matrix:

- 16 rows x 300 columns standalone pixels
- in-pixel amplifier and nMOS comparator
- 2 flavours (150 columns each)
  - nMOS comparator
  - nMOS comparator with TW compensation
- readout with FEI4 (bump/capacitive coupling) or with digital block in the periphery of the matrix
- 1-to-1 connection of each pixel to its digital cell in the periphery
- digital block with same functionality as in FEI3
  - time-stamp storage
  - pixel address generation
- test features
  - amplifer output connected to monitor line
  - comparator output connected to hit buts

H35DEMO - Features

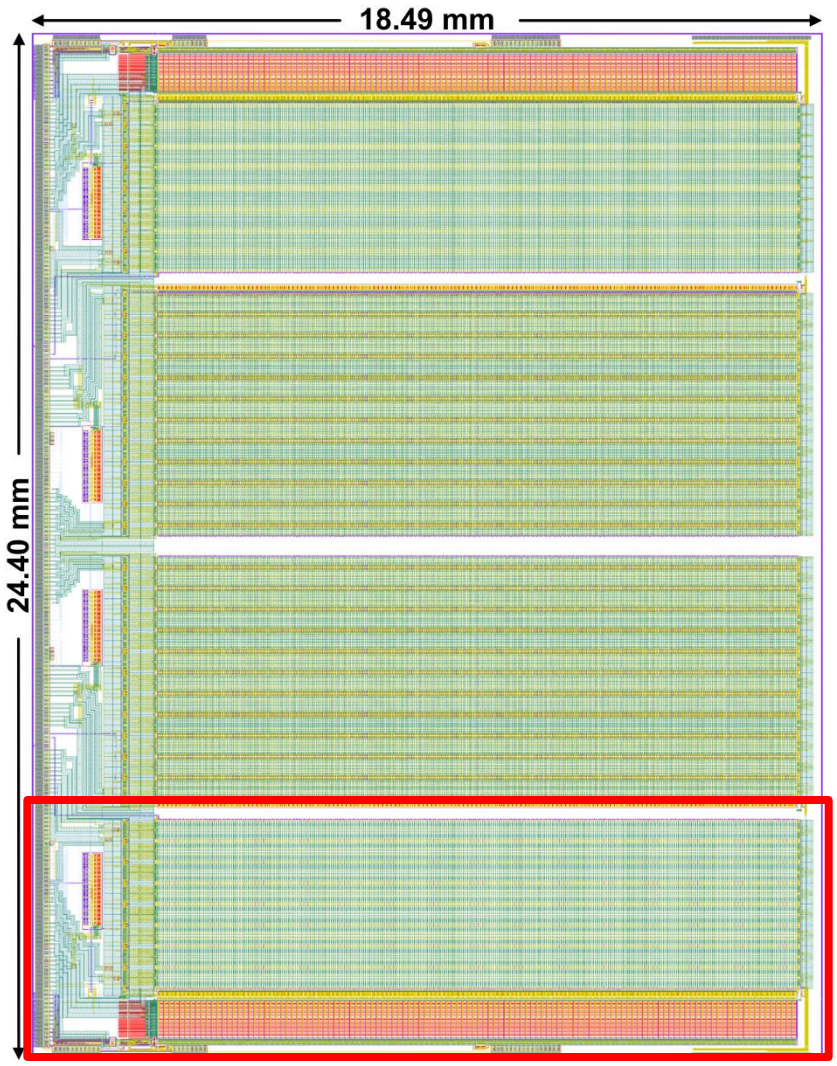


Analog matrix:

- 2 analog matrices, same idea, mirrored

- 23 rows x 300 columns analog pixels
- in-pixel amplifier
- different flavours
  - gain
  - speed
- readout with FEI4 (bump/capacitive coupling)
- test features
  - amplifer output connected to monitor line

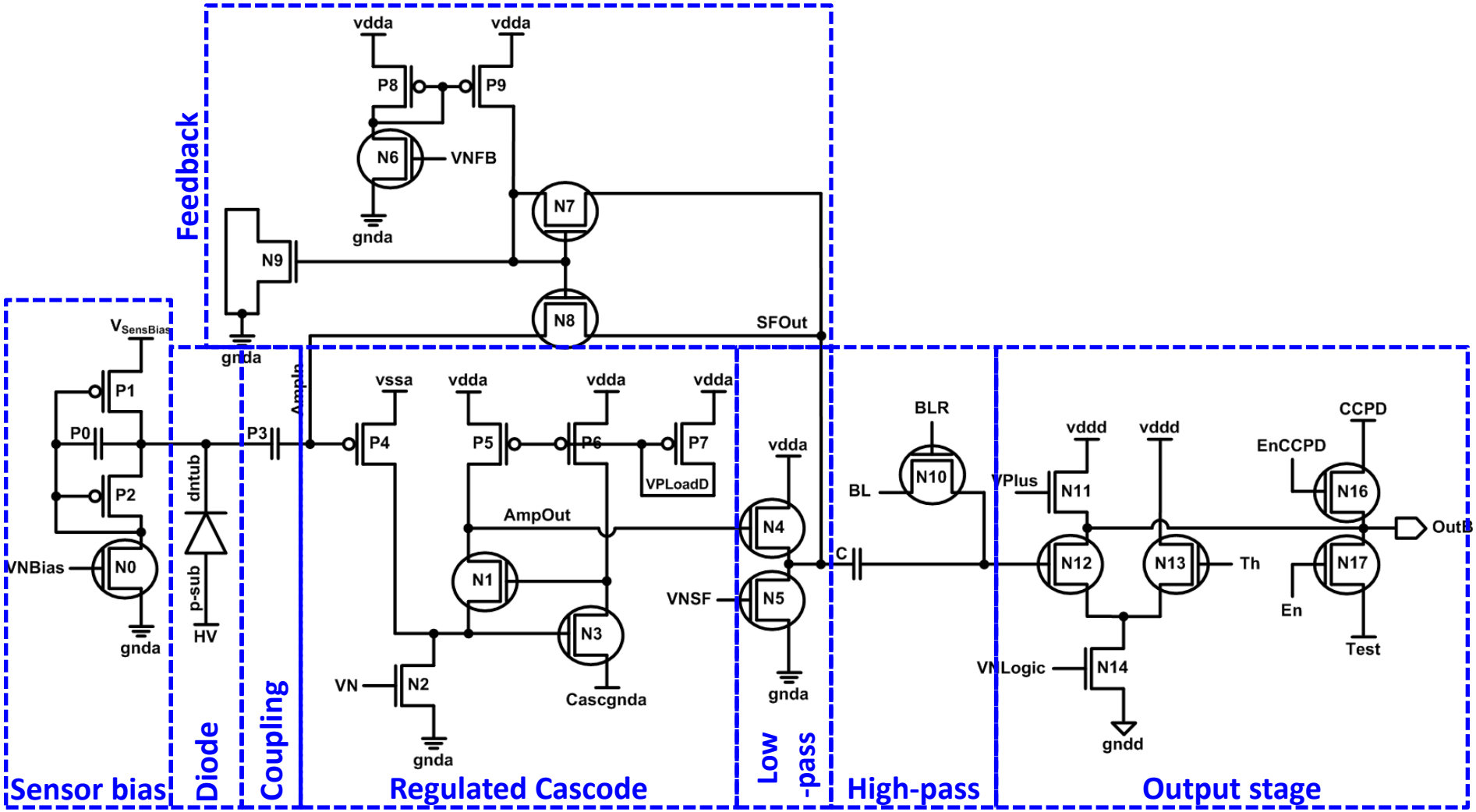
H35DEMO - Features



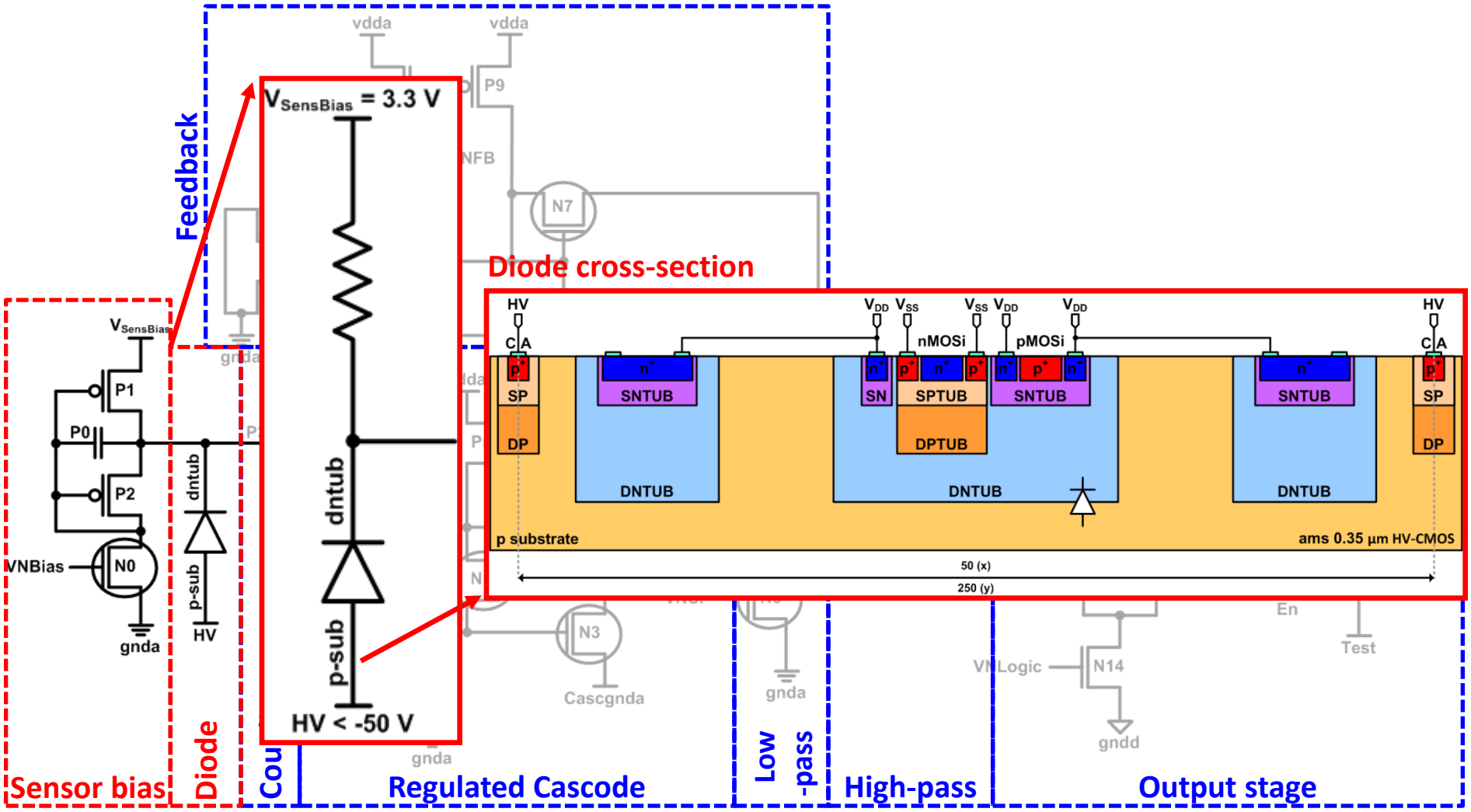
Standalone CMOS matrix :

- 16 rows x 300 columns analog pixels for standalone readout
- in-pixel amplifier and CMOS comparator in the periphery
- readout with FEI4 (bump/capacitive coupling) or with digital block in the periphery of the matrix
- 1-to-1 connection of each pixel to its digital cell in the periphery
- digital block with same functionality as in FEI3
  - time-stamp storage
  - pixel address generation
- test features
  - amplifer output connected to monitor line
  - comparator output connected to hit buts

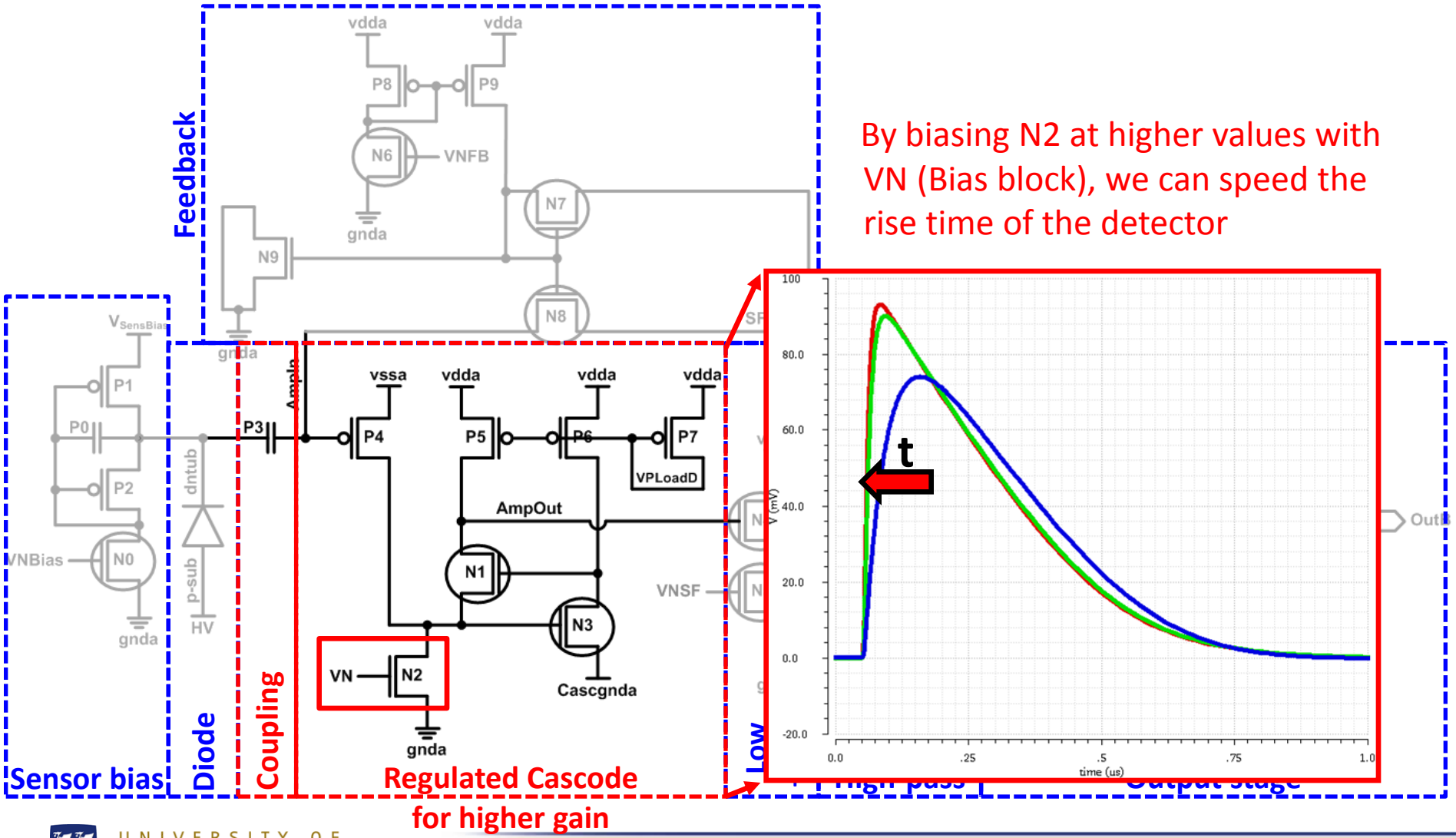
H35DEMO - Schematic analog pixel



H35DEMO - Schematic analog pixel

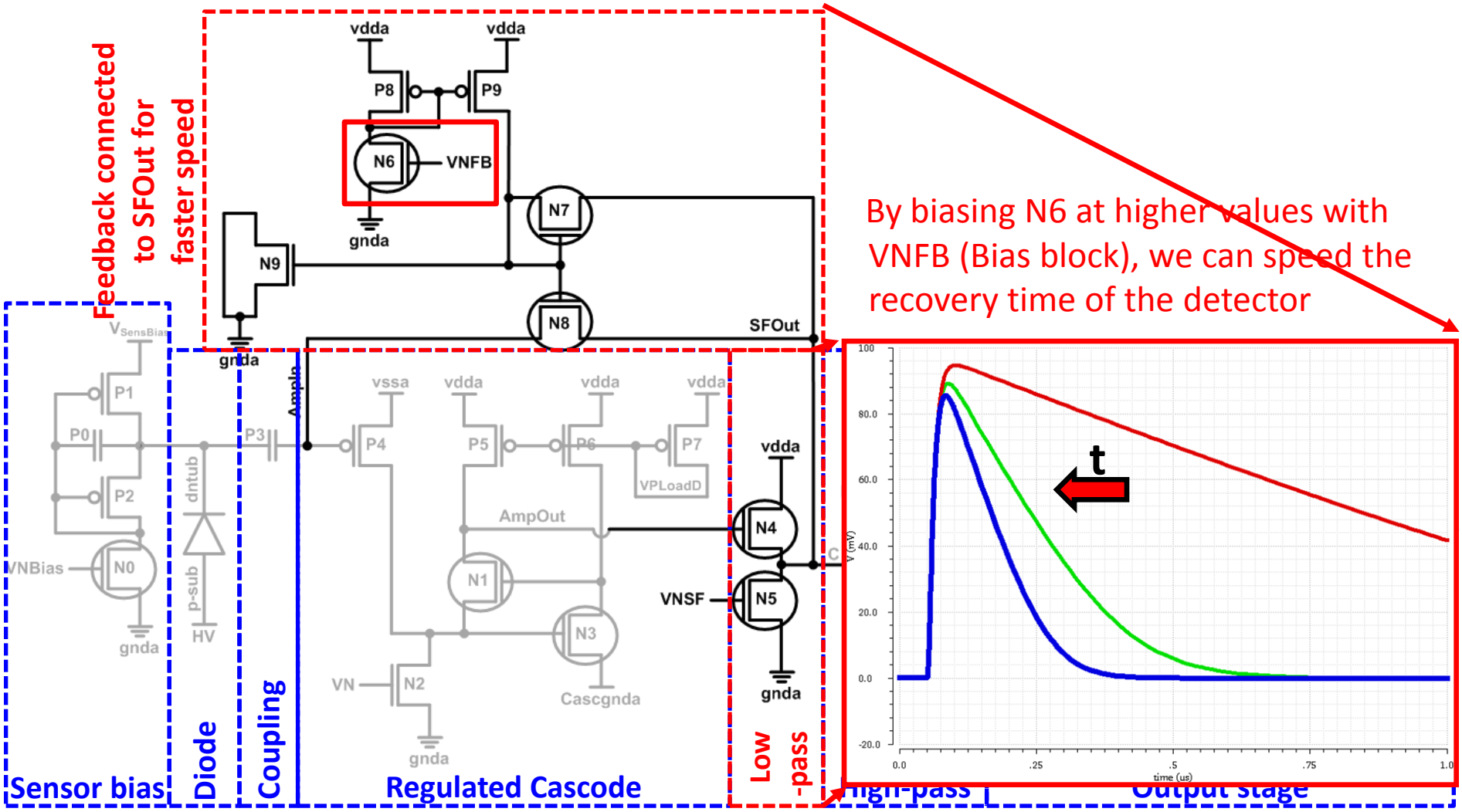


H35DEMO - Schematic analog pixel

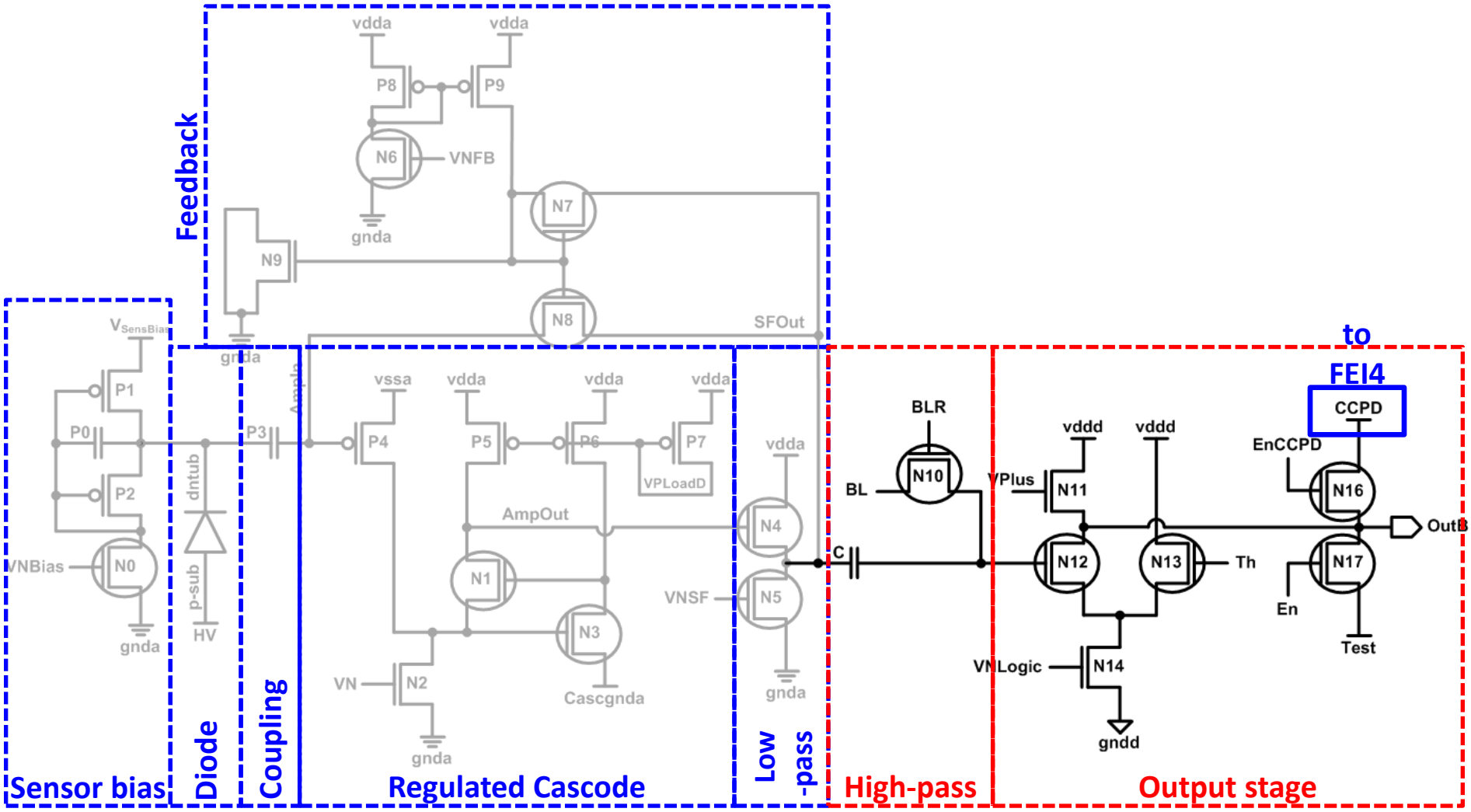


By biasing N2 at higher values with VN (Bias block), we can speed the rise time of the detector

H35DEMO - Schematic analog pixel



H35DEMO - Schematic analog pixel



H35DEMO - Layout analog pixel

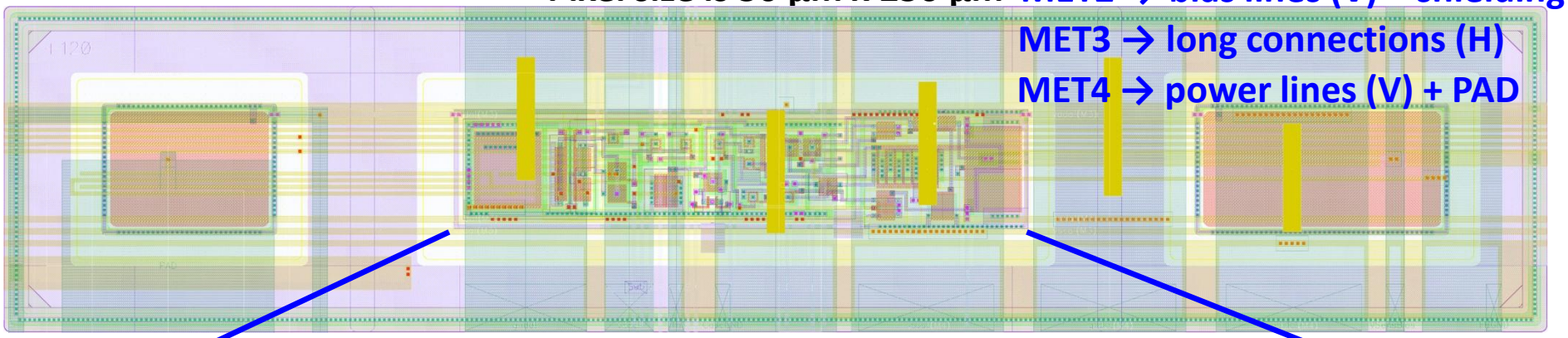
MET1 → in-pixel connections

Pixel size is 50 µm x 250 µm

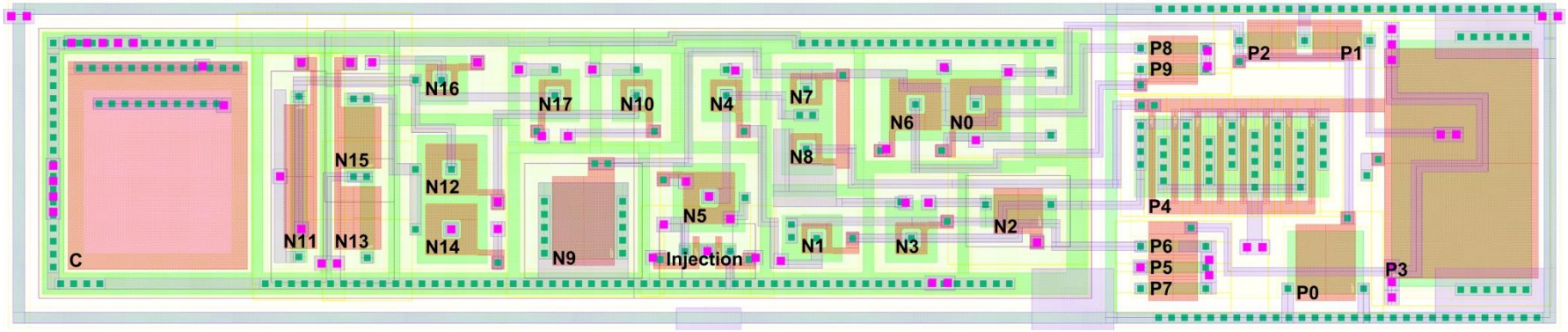
MET2 → bias lines (V) + shielding

MET3 → long connections (H)

MET4 → power lines (V) + PAD

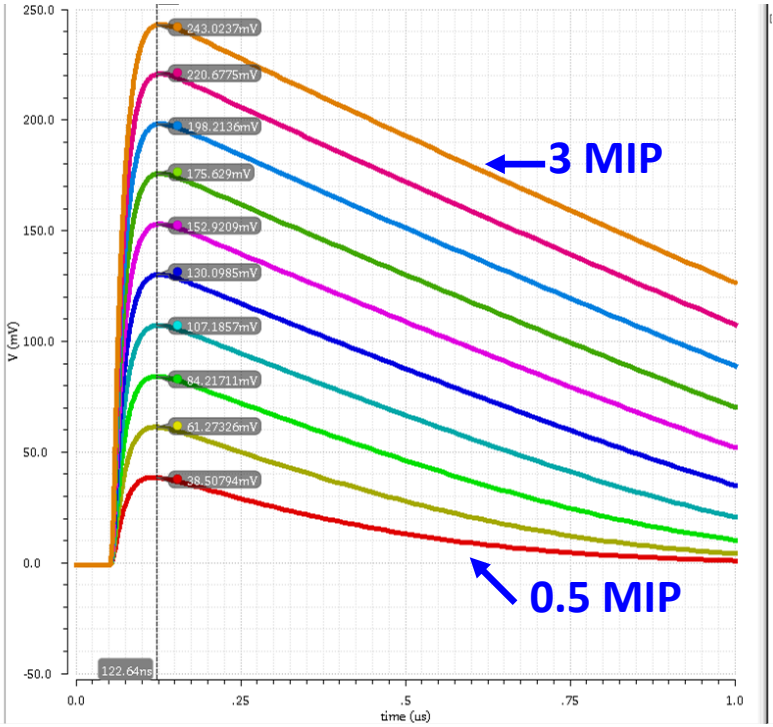


Transistors area is 20.25 µm x 95.05 µm

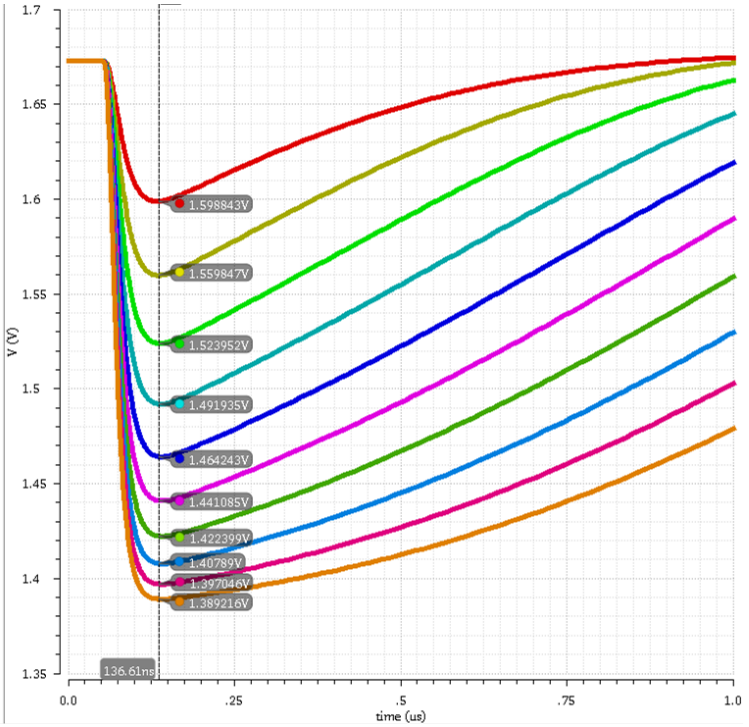


H35DEMO - Post-layout simulation

SFOut



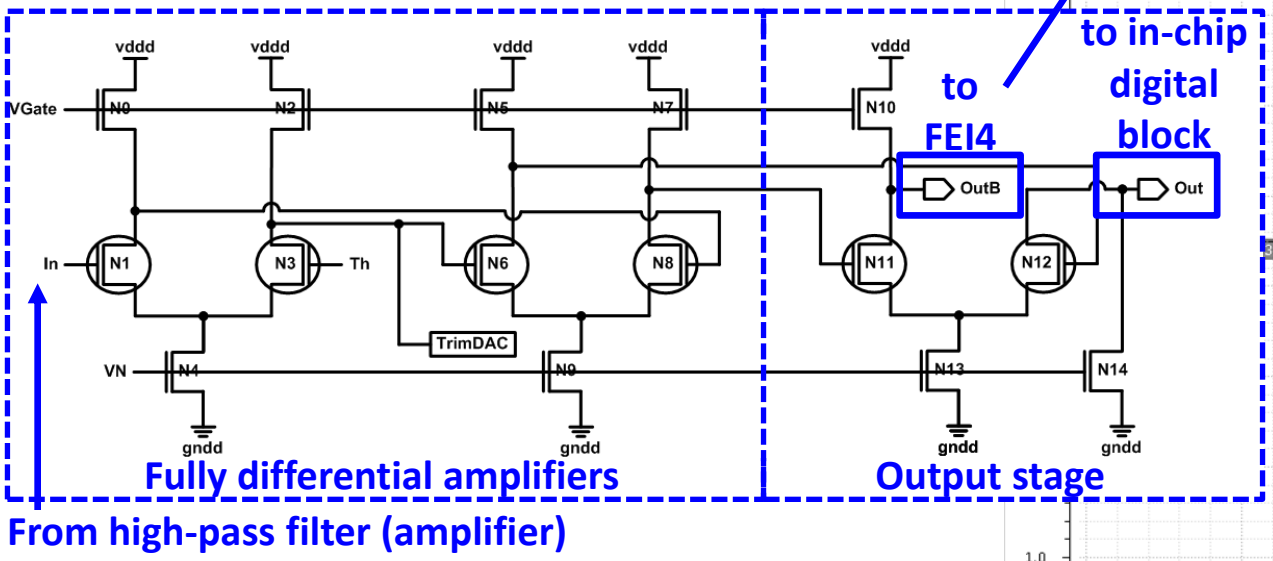
CCPD

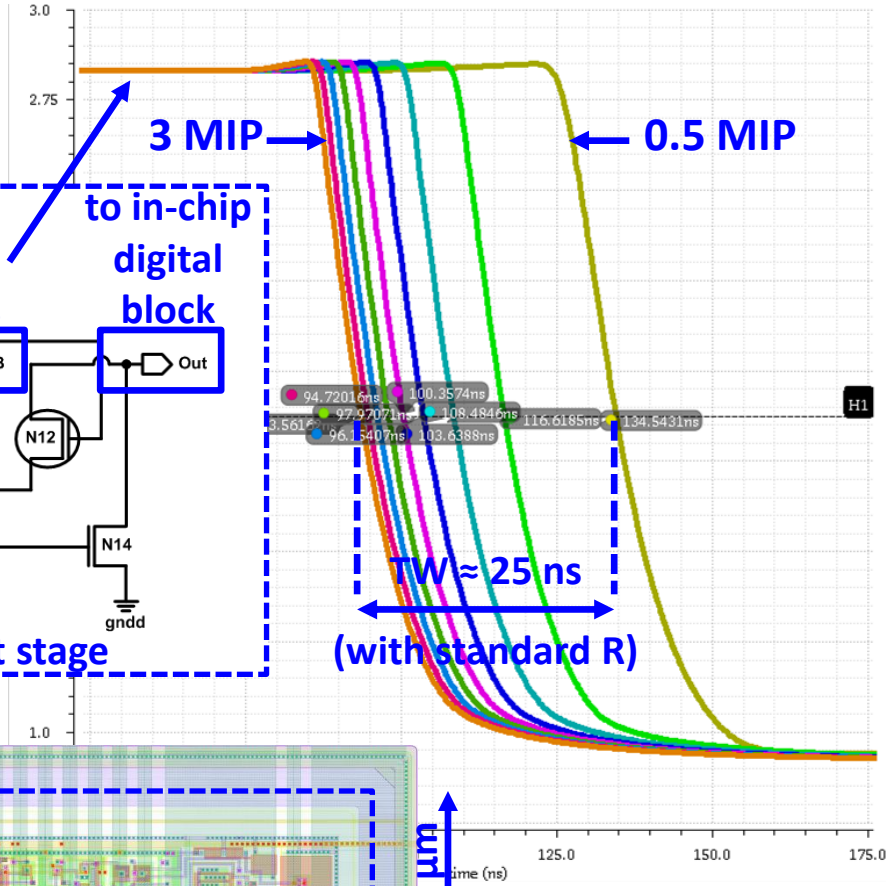


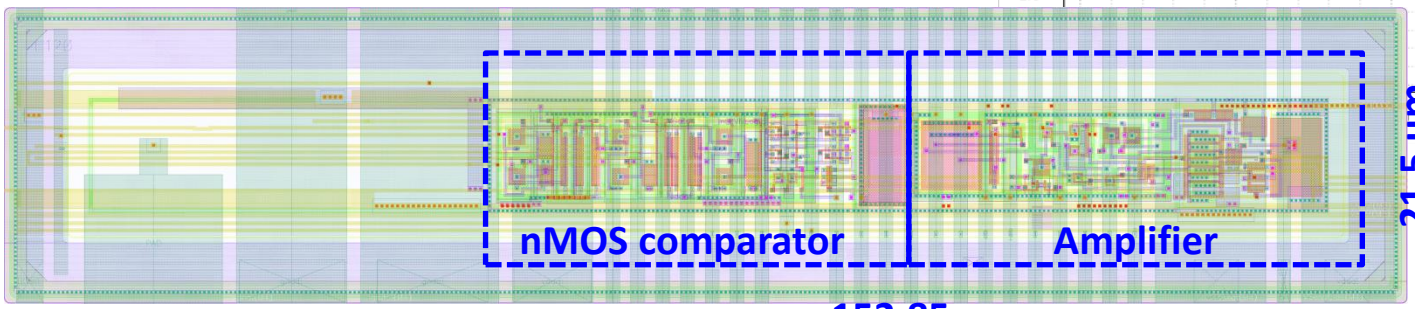
- The gain ranges between 38 mV (0.5 MIP) and 243 mV (3 MIP).
- The rise time is ≈ 31 ns.
- The recovery time ranges between ≈ 600 ns (0.5 MIP) and ≈ 1.6 µs (3 MIP). It can be reduced to ≈ 80-100 ns with more aggresive settings.
- The noise is 8 mV.

H35DEMO - Standalone nMOS pixel

- All nMOS comparator (in-pixel):



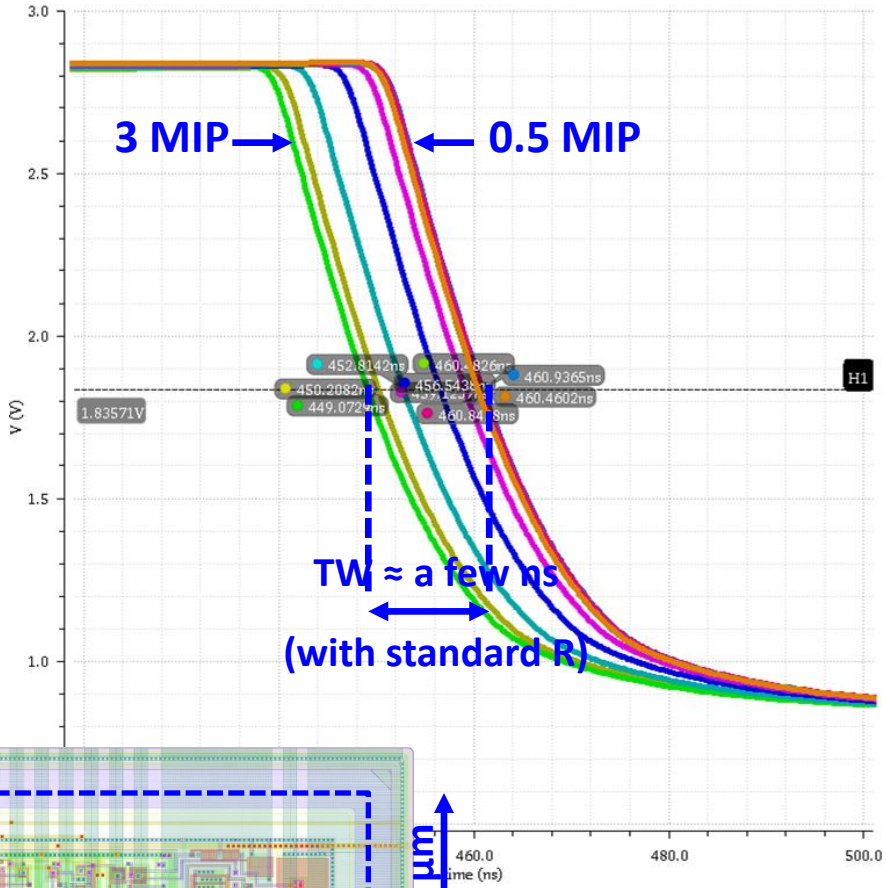


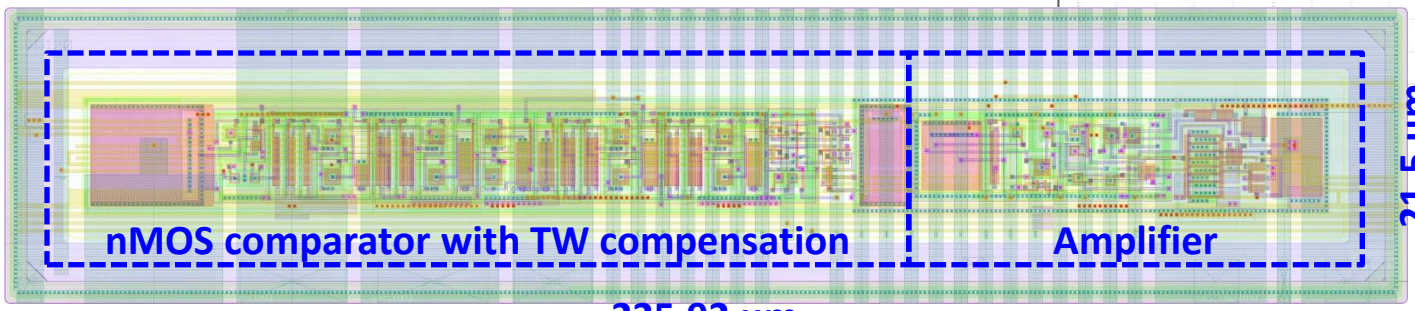


H35DEMO - Standalone nMOS pixel TW free

- All nMOS comparator (in-pixel):

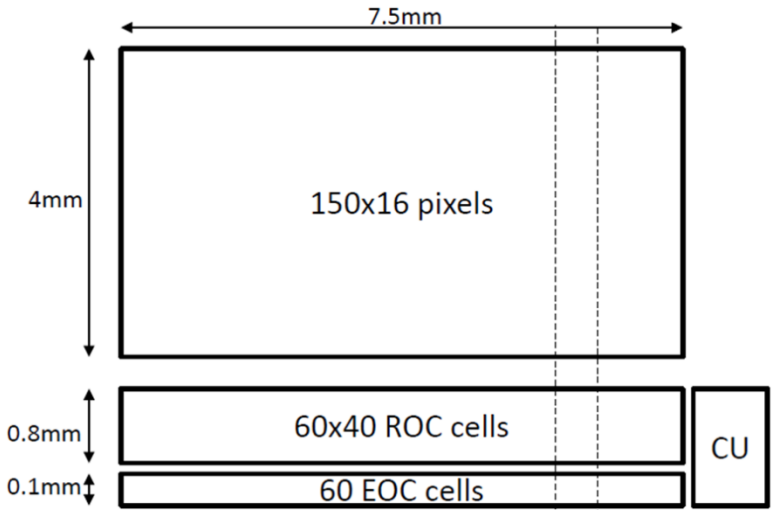
- Fully differential amplifiers
- Compensation system
- Output stage
  - To FEI4
  - To in-chip digital block





H35DEMO - Digital block

- It is placed in the periphery of the standalone nMOS and CMOS matrices.
- It consists of:
  - ROCs (ReadOut Cells)
    - CMOS comparator
    - pixel address ADDROM[7:0]
    - time-stamp TSRAM[7:0] upon particle hit
    - ADDR and TS are stored until readout
  - EOCs (End Of Columns) sample the data at 40 MHz. They transmit it to:
    - Par2SerTS. TS is serialized at 320 MHz.
    - Par2SerADDR. ADDR is serialized at 320 MHz.
  - Control Unit (CU)
    - It generates the control signals
    - Possibility to generate and monitor the control signals externally



(from R. Casanova)

Conclusion and future plans

- **H35DEMO submitted in September 2015**
  - Submission through an engineering run
  - Different substrate resistivities to improve SNR
  - It includes 4 matrices with different pixel flavours
    - standalone nMOS matrix
    - analog matrix (2 identical arrays)
    - standalone CMOS matrix
- **Future plans**
  - Demonstrator delivery will be ≈ 3 months after submission
  - Probing, flip-chip, assembly on PCB and wire-bonding
  - Bump bonding and/or gluing for measurements with FEI4
    - CARIBOu system for HV-CMOS control and powering
  - Test beam