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Prototyping of an HV-CMOS demonstrator for the High Luminosity-LHC upgrade

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HV-CMOS sensors can offer important advantages for large area tracking systems in high energy physics experiments. Their use in future collider experiments (HL-LHC) will depend on the capacity to sustain the anticipated radiation levels. This contribution presents the design and preliminary measurements of an HV-CMOS pixel demonstrator in the ams 0.35 μm HV-CMOS technology for the ATLAS upgrade. The readout is compatible with the FEI4 ASIC. To increase the depletion region, wafers with moderate/high resistivities have been used. Various alternatives are implemented with different gain, speed, number of readout stages and output type.

Summary

The high track density and extreme radiation fluence that the High Luminosity-LHC (HL-LHC) project will entail require an upgrade of the current hybrid tracking system of the ATLAS experiment. Amongst others, a novel detector concept based on standard HV-CMOS technologies has already demonstrated to be a feasible candidate. Advantages of HV-CMOS devices include the possibility of small cell areas, reduced thickness and lower cost than standard planar sensors. These advantages refer also to their use in combination with readout ASICs, like the existing FEI4 designed for the ATLAS experiment. Their capacity to retain the detection efficiency after HL-LHC level of radiations needs to be confirmed.

After a number of multi-project wafer runs from different vendors, the submission of an HV-CMOS demonstrator through an engineering run seems to be the natural next step in the R&D of this detector. The goal of the submission is to prototype an HV-CMOS sensor with a large area (full reticle size) that can serve as a technical foundation for qualifying these detectors as a serious contender for the HL-LHC. The chosen technology is the ams 0.35 μm HV-CMOS process and the radiation hardening solutions are pursued while respecting the ams standard processing rules. The use of moderate/high resistivity substrates, which is a selectable parameter for engineering runs, is explored for increasing the depletion region and improve the signal-to-noise ratio of the detector. The floorplan of the full size reticle presents several areas with different designs for comparative studies. These designs have a detector cell size of 50 μm x 250 μm to be readout by the FEI4 (with the same pixel dimensions) or standalone. The pixels comprise the sensor and first stages of signal conditioning, which in their majority are placed inside the collecting electrode. The analogue pixels have a charge sensitive amplifier, whilst the digital pixels also have a discriminator. To explore different options, pixels with different flavours to include conservative and more performing solutions have been included, ranging from medium/high amplification gain, slow/fast rise/shaping time to in/off-pixel comparators. In addition, key aspects at the layout level that allow to improve the behaviour of the detector, such as splitting the collecting area within one pixel into a few smaller areas to reduce the sensor capacitance and techniques to avoid electric field peaks and achieve better shielding have been implemented. We also foresee the possibility of using AC and DC coupling between the prototype and the readout ASIC by means of bump-bonding and gluing.

With this submission, we expect to learn which pixel topology suits better the HV-CMOS technology in order to fulfill the HL-LHC requirements. Details about the design of the demonstrator, together with simulated and first measured results, will be provided in this contribution. Special emphasis will be given on the gain, readout speed and noise of the detector upon particle hit. The results achieved with the different resistivity substrates and pixel types will also be analyzed.

Primary authors: VILELLA, Eva (University of Liverpool); CASSE, Gianluigi (University of Liverpool); PERIC, Ivan (Karlsruhe Institute of Technology); VOSSEBELD, Joost (University of Liverpool)

Co-authors: FERRERE, Didier (University of Geneva); IACOBUCCI, Giuseppe (University of Geneva); BENOIT, Mathieu (University of Geneva); CASANOVA, Raimon (IFAE)

Presenter: VILELLA, Eva (University of Liverpool)

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