Design of a constant fraction discriminator for the VFAT3 front-end ASIC of the CMS GEM detector

F. Loddo[1], T. Maerschalk[2]

[1]INFN Sezione di Bari, Bari, Italy

[2]Université Libre de Bruxelles, Brussels, Belgium

on behalf of the CMS GEM Collaboration

Abstract

In this work the design of a constant fraction discriminator (CFD) to be used in the VFAT3 chip, currently under design for the read-out of the triple-GEM detectors of the CMS experiment [1], is described. Simulations show that it is possible to extend the front-end shaping time to fully integrate the detector signal charge and maintain optimal timing resolution using the CFD technique. A prototype chip containing 8 CFDs was implemented using 130nm CMOS technology to prove the effectiveness of the proposed architecture before its integration in the VFAT3 chip. The CFD design and test results are shown.

Simulation

The time resolution, which is an important parameter for the use of the GEM detectors at the first CMS trigger level, has been studied with Monte Carlo simulations. The simulations are based on the GARFIELD [2] software to compute the CMS triple-GEM signals, taking into account the ionization statistics, the charge drift and amplification processes inside the gas volume of the detector. A typical triple-GEM signal is shown in Fig.1.

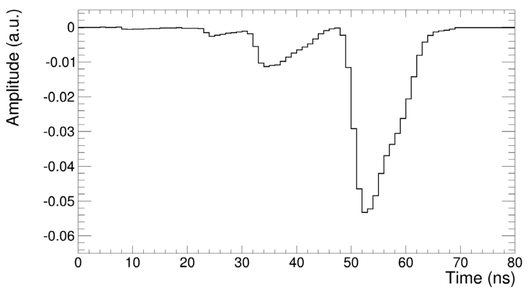

Fig. 1. Typical triple-GEM signal.

The detector signal is then convoluted with the expected transfer function of the front-end amplifier of VFAT3 chip, and the time resolution (Fig. 2) and latency (Fig. 3) for various VFAT3 peaking times are computed using the CFD and the time-over-threshold (TOT) techniques.

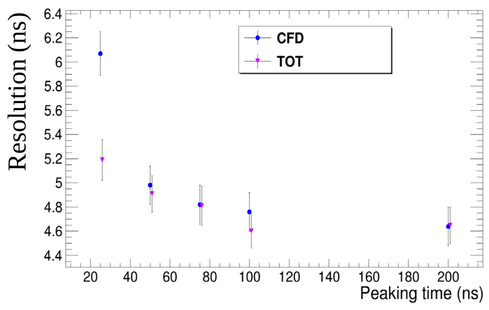

Fig. 2. Time resolution vs peaking time

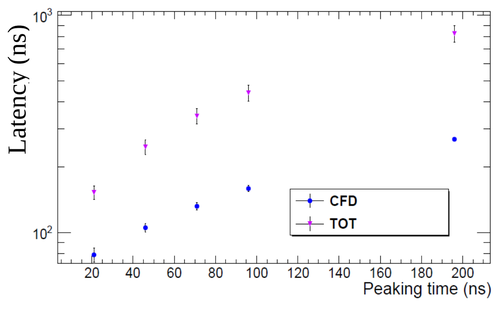

Fig. 3. Latency vs peaking time

The simulation study shows that it is possible to extend the VFAT3 front-end shaping time in order to fully integrate the GEM detector signal charge and avoid ballistic deficit and that the most efficient method, in terms of combined time resolution and latency is the CFD method. Using this technique, for a peaking time of 50 ns and a gas mixture of $Ar/CO_2/CF_4$ of 45:15:40, the simulated time resolution is 4.98 ± 0.16 ns with a total latency of 100 ± 5 ns.

CFD implementation

Constant fraction discrimination is a technique to provide amplitude-independent information about arrival time of an event. The principle operation is based on detecting the zero-crossing of the bipolar pulse obtained by subtracting a fraction of the input unipolar signal to its delayed copy (Fig.4). It can be demonstrated that the bipolar pulse crosses the baseline at a fixed time with respect to the start of the pulse.

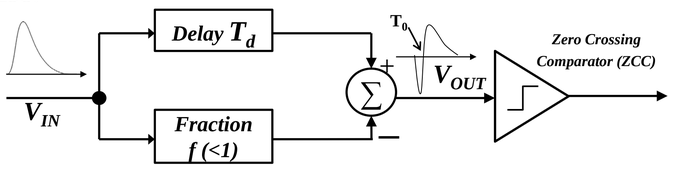

Fig. 4. Scheme of CFD principle of operation

Several practical implementations of integrated CFD have been proposed in literature. In this project, the solution proposed by S. Garbolino et al. [3] has been adopted. It is based on a fully differential architecture for better noise rejection and the delay and fraction implementation is realized using a shaping network with the cross-coupling topology shown in Fig.5.

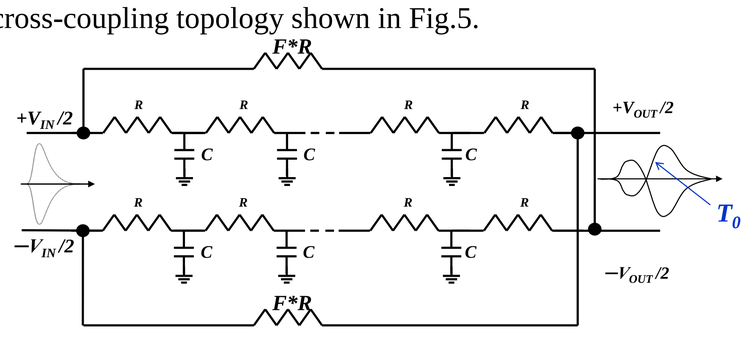

Fig. 5. Shaping network with cross-coupling topology

CFD implementation (cont.)

Since the VFAT3 analog front-end will have a programmable shaping time ranging between 25 ns and 100 ns, the same programmability has been introduced in the time constants of the CFD shaping network, in order to fully exploit the CFD technique for each VFAT3 shaping time. The resulting shaping network parameters are listed in Tab.1.

T_{peak} [ns]	Delay time T_d [ns]	f (fraction factor)
25	15	0.39
50	29	0.42
75	43.4	0.42
100	57.8	0.42

Tab.1. Shaping network parameters

The CFD block diagram is shown in Fig.6. The differential input signals are sent to the shaping network and the resulting bipolar pulses are amplified by the "post amplifier" that recovers the signal attenuation introduced by the passive shaping network and also applies a dynamic offset compensation. Finally, the differential bipolar pulses are sent to the zero-crossing (ZC) comparator that produces a digital pulse whenever its differential input crosses the baseline.

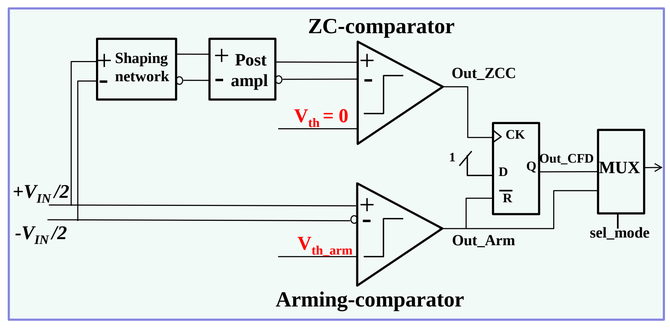

Fig. 6. CFD block diagram

The input signals are sent in parallel to an arming circuitry, in order to enable the CFD output only when the input signal is larger than the programmed threshold provided by a global 8-bit digital-to-analog-converter (DAC) . Moreover, each comparator has its own 6-bit DAC for fine tuning to compensate mismatches among channels.

Prototype test results

A prototype chip containing 8 CFDs has been produced using 130 nm CMOS technology to prove the effectiveness of the proposed technique before its integration in the VFAT3 chip. The biases and thresholds are provided by internal DACs remotely controlled by an SPI interface. The test setup, shown in Fig.7, consists of an arbitrary waveform generator (Lecroy Arbstudio 1102) capable of injecting into the chip inputs two semi-gaussian differential signals with tunable amplitude, peaking time (25 ns to 100 ns) and offset, and a 10 GS/s oscilloscope to perform the measurement on the outputs. Finally, a custom SPI controller allows to write/read the internal DACs, while a multimeter can be used to monitor internal voltages/currents. First of all, the local DACs have been set to equalize the channel thresholds. Then, using a global threshold of 10 mV, a set of time measurements have been performed injecting differential pulses with amplitude ranging between 10 mV and 1 V for different peaking time. In Fig. 8 a comparison between the timing response of the arming comparator (on the left) and the CFD (on the right) for T_{peak} = 100 ns are shown: it can be noticed that, skipping the point at the threshold of 10 mV, the arming comparator exhibits an amplitude time walk in the order of some tens of ns, while the CFD time response is almost independent of the input amplitude, showing a residual time walk < 1 ns for the individual channel and < 2 ns considering the 8 channels of the chip. Similar results are obtained also for the other peaking times.

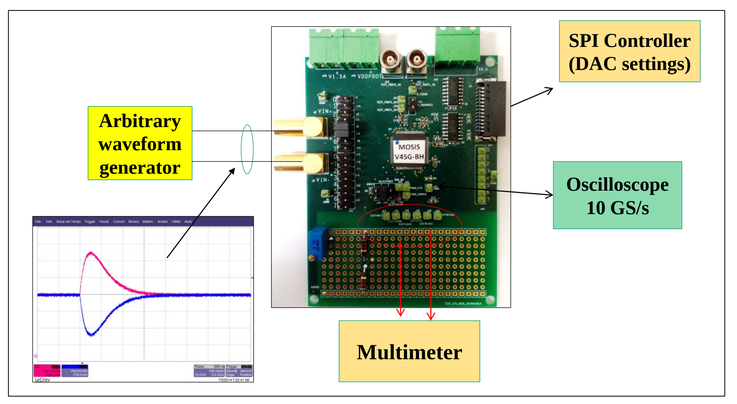

Fig. 7. Test setup

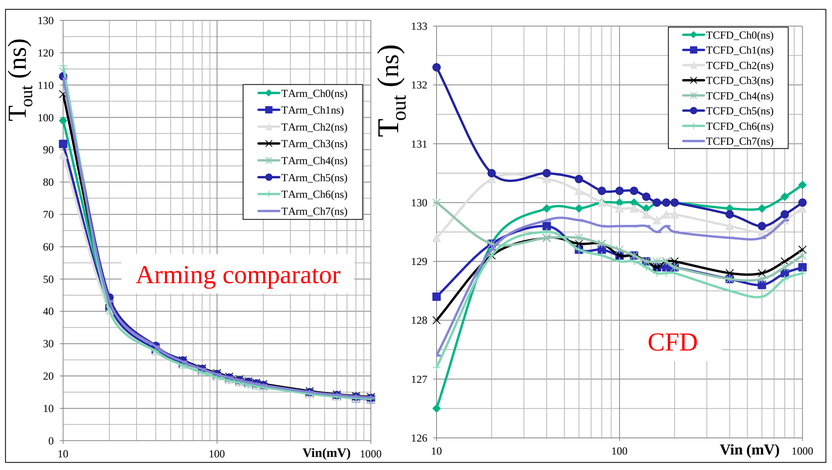

Fig. 8. Arming comparator and CFD time response for T_{peak} = 100 ns

The rate capability depends on the peaking time and ranges between 400 kHz for T_{peak} = 100 ns and 1 MHz for T_{peak} = 25 ns.

Another set of measurements was performed to evaluate the double pulse resolution. Two consecutive pulses with different amplitude and different time spacing ΔT (Fig.9) were sent to the CFD :

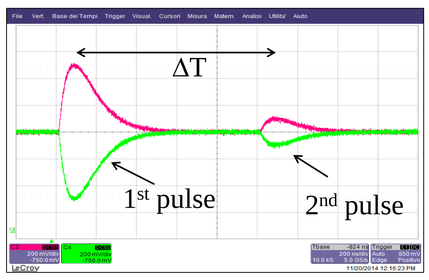

Fig. 9. Input signals for double pulse test

@ Tpeak = 75 ns, a large pulse (1 V) can be followed by small pulse (20 mV) within 1.5 μs with no timing degradation

@Tpeak = 25 ns, a large pulse (1 V) can be followed by small pulse within 800 ns with no timing degradation

Conclusions

The measurements on the CFD prototypes confirm the effectiveness of the proposed implementation and encourage us to use it in the VFAT3 chip for time walk correction when using peaking time longer than 25 ns.

References

[1] CMS GEM Collaboration, CMS-TDR-013, CERN-LHCC-2015-012

[2] R. Veenhof, garfield.web.cern.ch/garfield

[3] S. Garbolino et al., "*Implementation of Constant-Fraction-Discriminators (CFD) in Sub-micron CMOS Technologies", p*resented at 2011 IEEE NSS-MIC Conference, pp. 1530-1535