Contribution ID: **17** Type: **Poster**

Design of a Constant Fraction Discriminator for the VFAT3 front-end ASIC of the CMS GEM detector

Wednesday 30 September 2015 16:30 (1 minute)

In this work the design of a Constant Fraction Discriminator (CFD) to be used in the VFAT3 chip, currently under design for the read-out of the Triple-Gem detectors of the CMS experiment, is described. Simulations show that it is possible to extend the front-end shaping time to fully integrate the detector signal charge whilst maintaining optimal timing resolution using the CFD technique. A prototype chip containing 8 CFDs was implemented in 130nm CMOS technology to prove the effectiveness of the architecture before its integration in the VFAT3 chip. The CFD design and test results will be shown.

Summary

In this work the design of a Constant Fraction Discriminator (CFD) to be used in the VFAT3 chip, currently under design for the read-out of the Triple-Gem detectors of the CMS experiment, is described.
The time resolution, that is an important parameter for the use of the GEM detectors at the first CMS trigger level, has been studied with Monte Carlo simulations. The simulations are based on the GARFIELD software to compute the CMS Triple-Gem signals, taking into account the ionization statistics, the charge drift and amplification processes inside the gas volume of the detector. The detector signal is then convoluted with the expected transfer function of the front-end amplifier of VFAT3 chip and the time resolution is then computed using the CFD technique. The simulations allow to compare the time resolution for different detector gas mixtures, various VFAT3 peaking times as well as to compare with other techniques like the Time-Over-Threshold. Among the results, the simulations show that it is possible to extend the VFAT3 front-end shaping time in order to fully integrate the GEM detector signal charge and avoid ballistic deficit whilst maintaining optimal timing resolution using the CFD technique.
In the proposed implementation, the front-end unipolar signal is filtered by a shaping network that converts it into a bipolar pulse with amplitude-independent zero-crossing, with programmable time constants in order to fully exploit the CFD technique for each VFAT3 shaping times. Then, a first comparator detects the zero-crossing time while an arming threshold comparator enables the CFD output only when the signal is larger than the programmed threshold. Moreover, each comparator has its own 6-bit Digital-to-Analog-Converter for fine tuning to compensate mismatches among channels. The whole chain is implemented using a fully differential architecture for better noise rejection. A prototype chip containing 8 CFDs was implemented in 130 nm CMOS technology to prove the effectiveness of the proposed architecture before its integration in the VFAT3 chip. The CFD design and test results will be shown.

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Session Classification: Poster

Track Classification: ASICs