



Contribution ID: 19

Type: Poster

TOFPETv2: a high-performance ASIC for time and amplitude measurements of SiPM signals in time-of-flight applications

Tuesday, 29 September 2015 16:34 (1 minute)

We present the design and simulation of a readout and digitization ASIC for radiation detectors using Silicon Photomultipliers. The circuit, designed in standard CMOS 110 nm technology, has 64 independent channels optimized for time-of-flight measurement in PET or other applications. The chip has quad-buffered TDCs and charge integration ADCs in each channel with linear response in the range 0-1500 pC and 600 kHz maximum event rate per channel. Simulation results show that for an impulse charge of 200fC the circuit has 25 dB SNR, 93 ps r.m.s. time resolution, and 5 mW power consumption.

Summary

The TOFPETv2 ASIC is a low-power, low-noise, readout and digitization chip implemented in 110nm CMOS technology for fast radiation detectors used in Time-of-Flight applications. The chip integrates signal amplification circuitry, discriminators, charge integrators and high-performance TDCs for each of 64 independent channels. The circuit is an evolution of the TOFPET ASIC, which was developed in 130nm CMOS technology for Positron Emission Tomography (PET) applications using ToF information. In the new version of the ASIC, each channel performs a measurement of the Time-of-Arrival (ToA) as well as a measurement of the charge of the input pulses (ADC). The chip can also be configured to provide the Time-over-Threshold (ToT) of the pulses.

In PET applications, the ToA measurements allows the determination of the time difference of the two 511keV photons. The charge measurement provides a linear estimation of the photon energy. Future application in the readout of the timing detectors of the CMS-TOTEM Precision Proton Spectrometer at LHC is also foreseen.

The channel cell includes a low input impedance low-noise current conveyor and two trans-impedance amplifier branches separately optimized for time resolution and charge integration. Three voltage mode discriminators are used. One of them generates a fast trigger for accurate time measurement using a low threshold. The other two discriminators have configurable higher thresholds: one threshold is used for dark counts rejection and to start the integration window, and the second threshold is used to trigger the event data readout.

For each channel the digitization of the fast trigger is done by low-power quad-buffered analogue interpolation TDCs providing coarse and fine time stamps saved into local registers. The chip has configurable time binning of 40ps or 20ps. Used with silicon photomultiplier (SiPM) with 320 pF terminal capacitance and gain 1.25 (3.5) 106, the chip has SNR of 25 (30) dB for an input charge $Q_{in}=200$ (550) fC expected from a single photoelectron signal. From simulations, the expected contribution to Single Photon Time Resolution (SPTR) is less than 100 (40) ps rms.

Quad-buffered charge integration followed by a Wilkinson ADC provides a linear measurement of the pulse amplitude. The range of the charge integration can be adjusted according to the application requirements. The two main settings allow charge measurement from 4 pC to 500 pC and from 10 pC to 1500 pC.

A global chip controller builds-up the event data and runs the interface with the data acquisition back-end. The chip uses an external clock with frequency up to 400 MHz and works in push mode sending out the data of all events above the trigger threshold. The rate capability of the ASIC is of about 600kHz of triggered events per channel, being this rate limited by the maximum rate of the digital output (3.2 Gbit/s). In addition,

a dark count rate up to 2 MHz can be handled by each channel with negligible dead time while using a timing threshold at the level of one photoelectron. The power dissipation is in the range of 5-8 mW per channel depending on the configuration settings.

The chip tape-out is planned for June 2015.

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Session Classification: Poster

Track Classification: ASICs