Design of a 10-bit segmented current-steering digital-to-analog converter in CMOS 65 nm technology for the bias of new generation readout chips in high radiation environment

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Abstract

A new pixel front end chip for HL-LHC experiments in CMOS 65nm technology is under development by the CERN RD53 collaboration together with the Chipix65 INFN project. This work describes the design of a 10-bit segmented current-steering Digital-to-Analog Converter (DAC) to provide a programmable bias current to the analog blocks of the circuit. The main requirements are monotonicity, good linearity, limited area consumption and radiation hardness up to 10 MGy. The DAC was prototyped and electrically tested, while irradiation tests will be performed in Autumn 2015.

DAC implementation

The DAC is based on an array of matched current sources using a segmented architecture (Fig. 1): the two least significant bits are implemented with binary weighted current sources while the eight most significant bits are implemented with unary-decoded current cells controlled by a binary-to-thermometer decoder. This solution represents a trade-off between power consumption, area and optimization of Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) [1]. The design was optimized for an LSB = 100 nA, but different reference currents can be used with slight degradation of performance in terms of DNL and INL. In TABLE I a summary of the characteristics is listed.

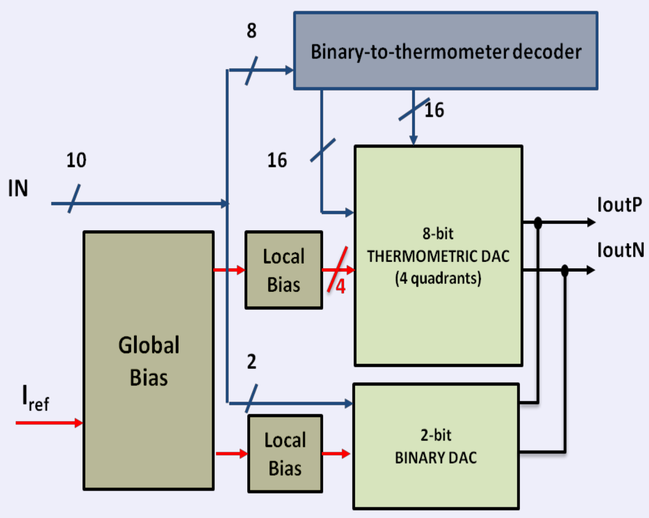

Fig.1 DAC block diagram

In order to withstand the expected high radiation environment, no minimum size transistors are used also in the implementation of the decoder, thus a set of custom digital cells has been designed. Anyway, in the prototype two different versions of decoder (with custom cells and standard cells) have been implemented, in order to compare their eventual degradation with the irradiation tests.

Supply voltage	**1.2 V ± 10%**
Resolution	**10 bits**
Size	**140 um x 240 um**
Temperature range	**-20, +50 C**
LSB (typ)	**100 nA**
DNL	**< ± 0.4 LSB**
INL	**< ± 1 LSB**
Power consumption (typ)	**150 uW**

Table I. DAC characteristics

A prototype chip was submitted in October 2014 and ten samples have been tested and characterized. In Fig. 2, the chip layout is shown and the two DACs are clearly visible.

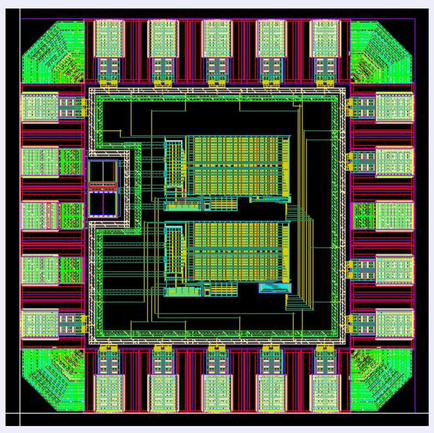

Fig.2 Chip layout

Test of prototypes

10 prototypes, for a total of 20 DACs, were tested using a custom test board (Fig.3) providing a stable (with T) reference current and an Ethernet controlled input code driver, while the output currents were read with an external multimeter. All the active components of the board were housed on piggy back daughter boards, in order to unplug them during the irradiation tests.

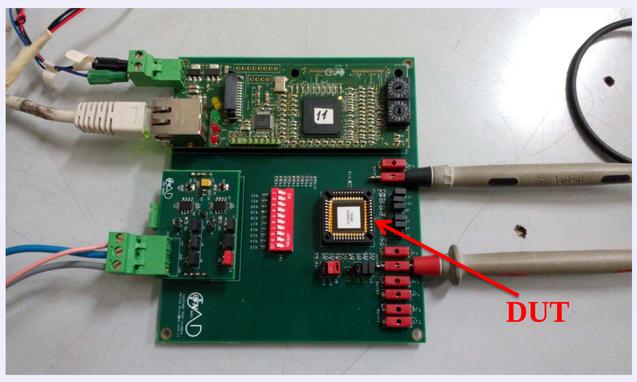

Fig.3 Test board

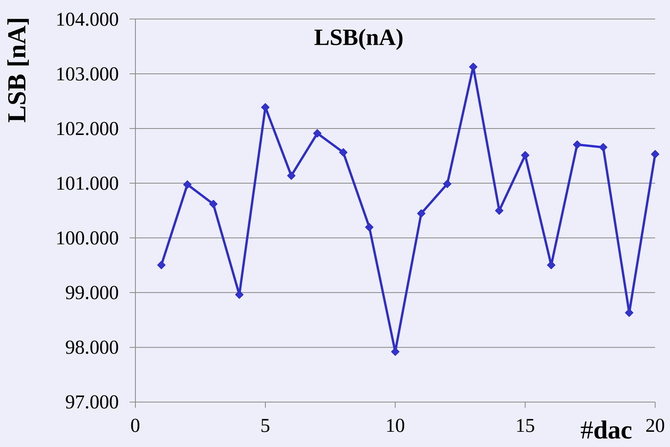

Fig.4 Measured LSB vs #dac

First of all, using the same reference current for all the DACs, the I_{LSB} was measured (Fig.4) and compared with the nominal one:

Nominal I_{LSB} = 100 nA

I_{mean} = 100.74 nA
σ = 1.31 nA (1.3%)

Then, the differential and integral non-linearities (DNL and INL) were measured and compared with the mismatch Monte-Carlo simulations performed during the design. In Table II the results are summarized while, in Fig.5 and Fig.6, the INL curves for MC simulations and test results are displayed and show the good agreement between simulations and tests.

LSB = 100nA	**DNL_{rms}(LSB)**	**DNL_{max}(LSB)**	**INL_{rms}(LSB)**	**INL_{max}(LSB)**
Test results (20 DACs)	**< 0.15**	**< 0.4**	**< 0.45**	**< 1**
MC simulation (500 pts)	**< 0.11**	**< 0.45**	**< 0.45**	**< 1.5**

Table II. Summary of DNL and INL test results

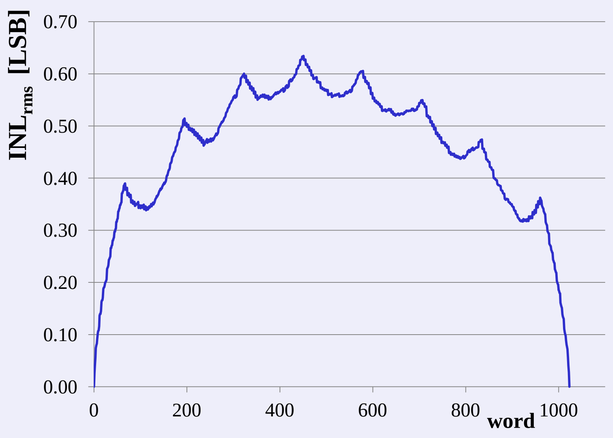

Fig.5 INL_{rms} from mismatch MC simulations (500 pts.)

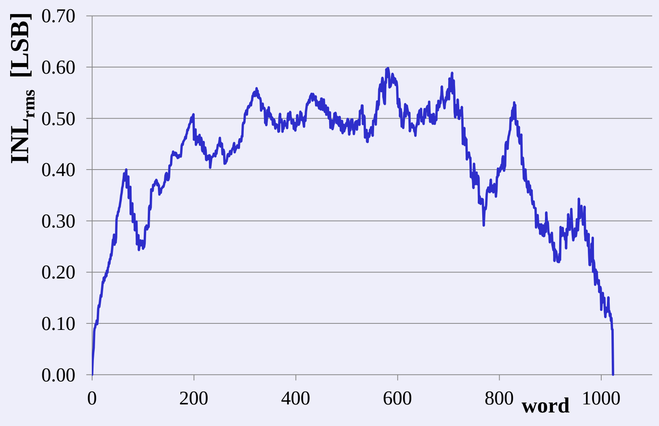

Fig.6 INL_{rms} from test results (20 DACs)

Conclusions

A 10-bit current DAC has been developed in CMOS 65 nm technology to provide programmable bias currents to analog blocks of the new pixel front end chip for HL-LHC experiments, presently under development by the CERN RD53 collaboration together with the Chipix65 INFN project.
A segmented 8+2 architecture has been proposed and prototyped in October 2014.
Test results on 10 prototypes show good performance of the DAC, with DNL and INL, in good agreement with Monte Carlo simulations.
The next step is to perform irradiation test using X-rays and low energy protons to check the radiation hardness up to a total dose of 10 Mgy.

References

[1] Chi-Hung and Klaas Bult, “A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2,” IEEE Journal of solid state circuits, vol. 33, No. 12, pp. 1948-1959, December 1998