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# Design of a 10-bit segmented current-steering Digital-to-Analog Converter in CMOS 65nm technology for the bias of new generation readout chips in high radiation environment

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A new pixel front end chip for HL-LHC experiments in CMOS 65nm technology is under development by the CERN RD53 collaboration together with the Chipix65 INFN project. This work describes the design of a 10-bit segmented current-steering Digital-to-Analog Converter (DAC) to provide a programmable bias current to the analog blocks of the circuit. The main requirements are monotonicity, good linearity, limited area consumption and radiation hardness up to 10 MGy. The DAC was prototyped and electrically tested, while irradiation tests are foreseen for summer 2015. The implementation and test results will be shown.

## Summary

A new pixel front end chip for HL-LHC experiments in CMOS 65nm technology is under development by the CERN RD53 collaboration together with the Chipix65 INFN project. The chip will be exposed to the unprecedented radiation level of 1 10 MGy and 10E16 neutrons/cm2 particle flux and a CMOS 65nm technology will be used for the first time in HEP community.
This work describes the design of a 10-bit current-steering Digital-to-Analog Converter (DAC) to provide a programmable bias current to the analog blocks of the circuit. The main requirements are monotonicity, good linearity, limited area consumption and radiation hardness up to 1 Grad.
The DAC is based on an array of matched current sources using a segmented architecture: the two least significant bits are implemented with binary weighted current sources while the eight most significant bits are implemented with unary-decoded current cells controlled by a binary-to-thermometer decoder. This solution represents a trade-off between power consumption, area and optimization of differential non-linearity.
In order to withstand the expected high radiation environment, no minimum size transistors are used also in the implementation of the decoder, thus a set of custom digital cells has been designed and used.
A prototype chip containing two DACs was submitted and ten samples have been tested and characterized, while irradiation tests with X-rays will be performed in summer 2015 in order to check the radiation hardness of the circuit. The proposed implementation and test results will be shown.

**Primary author:** LODDO, Flavio (INFN-BARI)

**Co-authors:** TAMMA, Camillo (Universita e INFN (IT)); DE ROBERTIS, Giuseppe (Universita e INFN, Bari (IT)); PACHER, Luca (Universita e INFN Torino (IT))

**Presenter:** LODDO, Flavio (INFN-BARI)

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