Pixel front-end with synchronous discriminator and fast charge measurement for the upgrades of HL-LHC experiments

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Introduction

Pixel detectors for HL-LHC experiments require the development of a new generation front-end chip to stand unprecedented radiation levels, very high hit rates and increased pixel granularity (see the table).

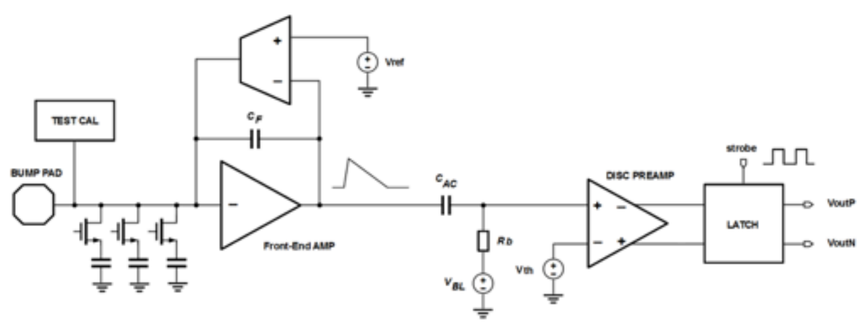
A very compact, low power, low threshold analog front-end in 65nm CMOS technology is described. It contains an offset compensated synchronous comparator that can be turned into few hundred MHz local oscillator to implement fast Time-over-Threshold (ToT) counting.

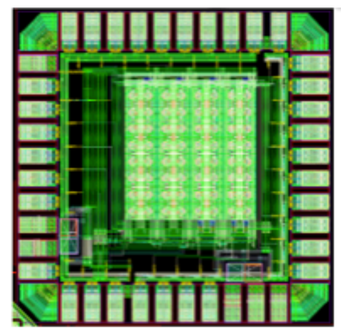
A first prototype has been submitted in October 2014 and characterized: the results of the measurements are presented. A second version has been submitted in May 2015.

This work has been performed in the framework of the CERN RD53 Collaboration and has been funded by the CHIPIX65/INFN project.

	1st generation LHC phase 0	2nd generation LHC phase 1	3rd generation LHC phase 2 – HL-LHC
Maximum pixel flux	200 MHz/cm²	600 MHz/cm²	2 GHz/cm²
Radiation hardness	150 MRad	350 MRad	1 GRad
Signal threshold	2500-3000 e⁻	1500-2000 e⁻	≤1000 e⁻

Analog Front-End overview



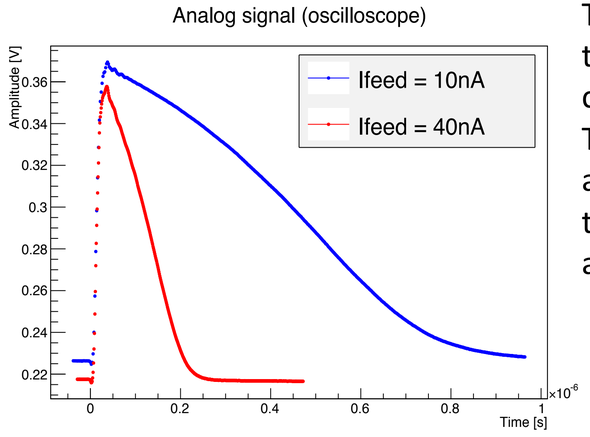


8x8 pixel matrix submitted and tested
Analog readout of CSA and Discriminator (via buffers)

- **PREAMPLIFIER**
  - One stage CSA with Krummenacher feedback
- **Synchronous DISCRIMINATOR**
  - (AC coupled to CSA)
  - offset compensated diff.amplif. + latch;
  - **FAST Time-over-Threshold**
    - Local oscillator strobing Latch (to 800MHz)
- **Calibration circuit**
  - digital signal + DC calibration level

Performance SUMMARY
- Compact: ~25um x 40 um
- Low power: ~ 4 uA (with ToT logic)
- Low noise: ENC=100e⁻ @C_{det}=100 fF
- Leakage compensation: up to 50nA/pixel
- Fast Charge measurement:
  - 30 ke⁻ in <300ns (or 800ns)
  - up to 7-8bit (125-250e⁻/ADC) - no ext clock
- NO Threshold-Trimming:
  - autozeroing made by hardware

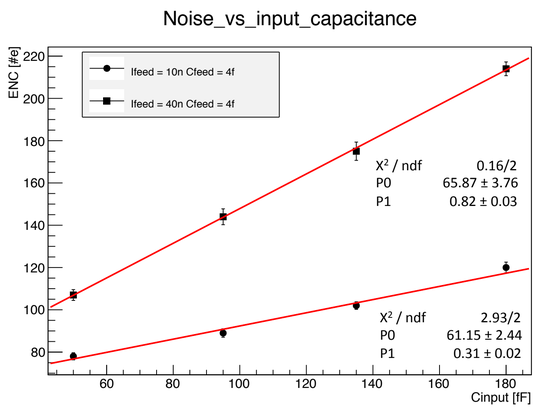
Analog signal



The preamplifier signal has been measured with two different configurations of the feedback current linked to the speed of the ToT discharge. The peaking time, similar in the two cases, is around 25 ns for an input capacitance of 50 fF. In the second version of the chip it is reduced of around 3 ns.

Feedback current	ToT for a 10ke⁻ input charge	Noise with C_{input} = 50 fF
10 nA	90 ns	78 e⁻
40 nA	300 ns	107 e⁻

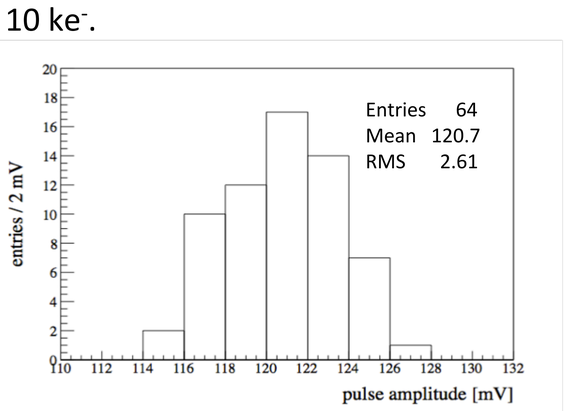
Noise performance

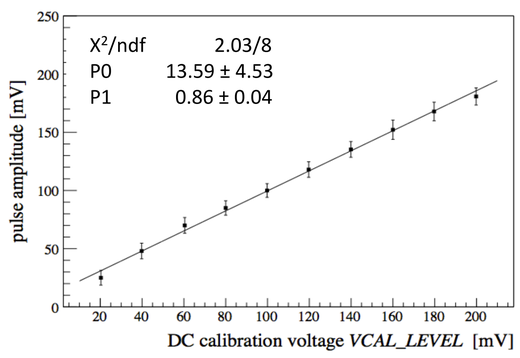


The noise of 16 pixels has been measured through S-curves in different conditions of feedback current and input capacitance.
The figure shows the expected linear trend of the Equivalent Noise Charge as a function of the input capacitance. High values of the feedback current, which correspond to a fast ToT, lead to an increase of the noise of around 20%.

Voltage gain

With the calibration circuit used in this chip a calibration voltage of 20 mV corresponds to a signal of 1 ke⁻. The linearity has been measured up to 10 ke⁻.

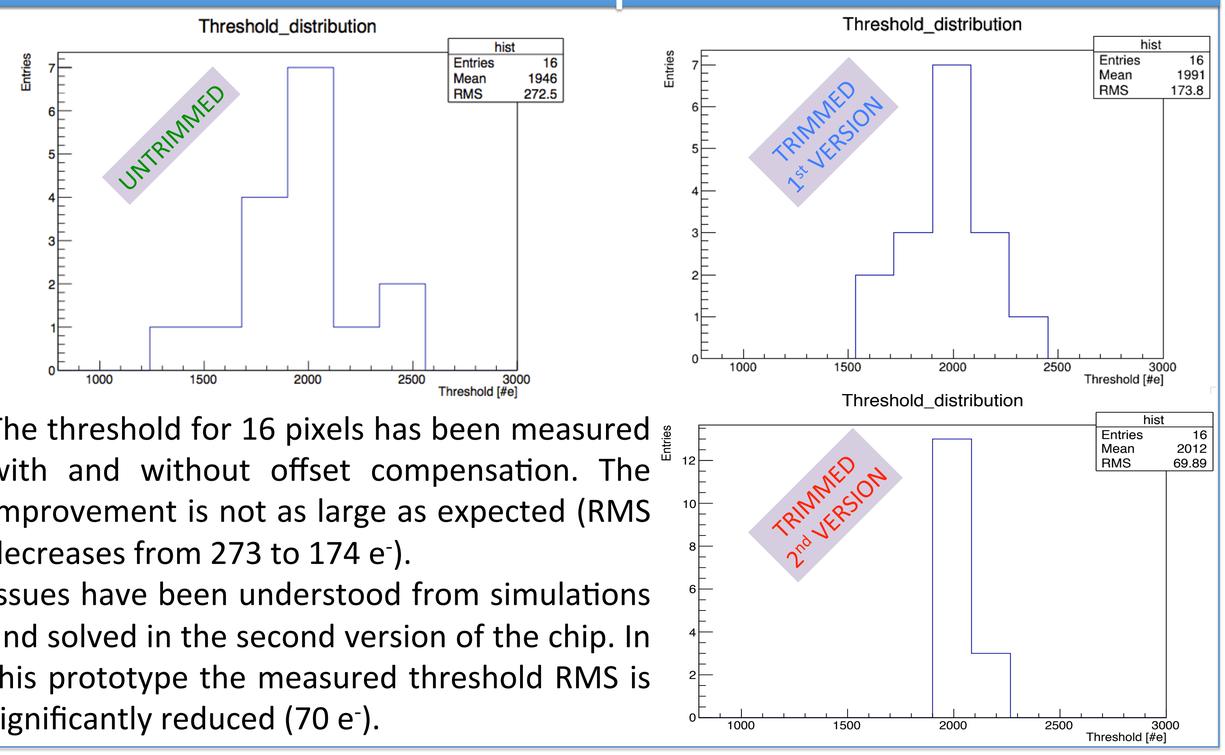




The signal amplitude has been measured for each of the 64 pixels in the matrix for a signal of 6 ke⁻, which is around the mean value of the expected signals.

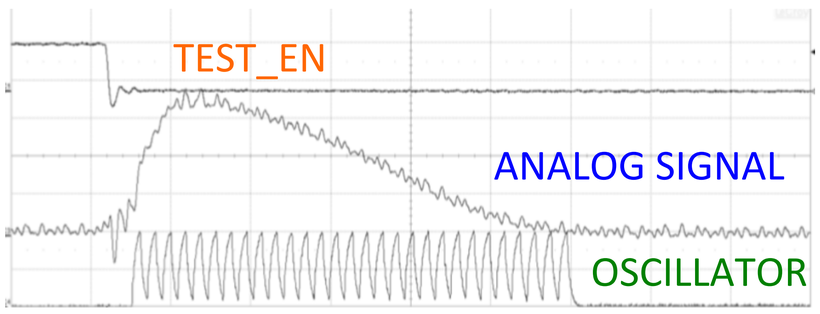
The histogram shows that the spread of the gain between different channels is small, in fact the RMS of the distribution is equal to the 2.2% of the mean value.

Offset compensation



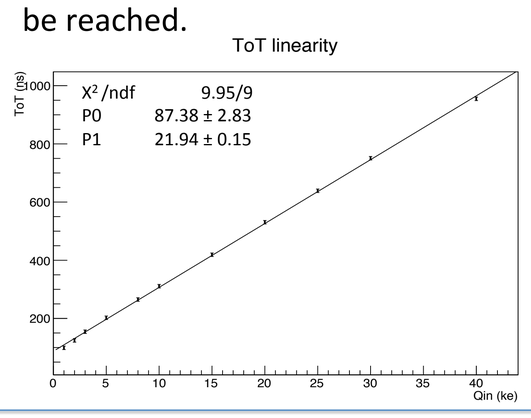
The threshold for 16 pixels has been measured with and without offset compensation. The improvement is not as large as expected (RMS decreases from 273 to 174 e⁻).
Issues have been understood from simulations and solved in the second version of the chip. In this prototype the measured threshold RMS is significantly reduced (70 e⁻).

Time-over-Threshold (ToT)



The measurement of the ToT linearity has been performed on the analog signal, fixing a threshold on the oscilloscope. The picture shows the very good linearity of this architecture up to an input signal of 40 ke⁻, which is beyond the maximum signal which is expected in the sensor.

Here the latch is turned into a local oscillator. During the measurements the frequency has been kept equal to 100 MHz due to setup limitations, but simulations showed that at least 500 MHz can be reached.



Conclusions

- First version of a synchronous front-end with offset compensation designed and tested
  - ➢ Small spread of the gain between channels
  - ➢ Idea of “self-oscillating” comparator for the fast ToT measurement works
  - ➢ Offset before trimming not bad
  - ➢ Offset after trimming issues understood
- Second version submitted in May 2015
  - ➢ Offset compensation performance improved