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Pixel front-end with synchronous discriminator and fast charge measurement for the upgrades of HL-LHC experiments

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Pixel detectors for HL-LHC experiments require the development of a new generation front-end chip to stand unprecedented radiation levels, very high hit rates and increased pixel granularity. A very compact, low power, low threshold very front-end design in 65nm CMOS technology is described. It contains a synchronous comparator with output offset storage threshold compensation technique. The latch can be turned into few hundred MHz local oscillator using an asynchronous logic feedback loop to implement fast time-over-threshold counting. A first prototype has been submitted in October 2014 and characterized: measurements and first irradiation results are presented.

Summary

The HL-LHC experiments will be exposed to particle fluxes at least five times larger compared to LHC and to a total radiation dose about ten times higher. In pixel detectors the silicon sensors and the front-end electronics will be facing new challenges, more importantly: unprecedented radiation fluence (around 1 Grad in 10 years), very high hit rates (2 GHz/cm^2), smaller pixel cell size (50x50 or 25x100 μm^2) to increase the granularity with almost no change in the power budget per unit area with respect to present detectors. In order to meet all these requirements, the HEP community has chosen CMOS 65nm technology for the new generation pixel chip.

In this paper the design of a new analog readout front-end chain is described. The first prototype has been realized with a $1x1\ mm^2$ chip containing a 8x8 matrix of $50x50\mu m^2$ pixel cells, where around half space is taken by the analog chain. A one-stage Charge Sensitive Amplifier with nominal peaking time of 25 ns is used. The value of the feedback capacitor is selectable among 2.5,4 and 6.5 fF. A Krummenacher feedback has been adopted to compensate sensor leakage currents up to 50 nA and also to have a constant current discharge of the feedback capacitor, in order to implement charge measurement with the time-over-threshold technique (ToT). The front-end can be configured such to have a fast ToT of 100 ns for a $10ke^-$ input charge.
Test capacitors have been added to mimic different values of sensor capacitance among 25 and 150 fF. A calibration circuit is used to inject a charge at the preamplifier input node.

The preamplifier is AC coupled to the discriminator. A synchronous discriminator architecture has been chosen in order to have no contribution to the time walk, and it is composed of a low gain differential amplifier and a latch. The discriminator takes decisions at 40 MHz frequency. The latch of this stage can be turned into a local oscillator (up to 500 MHz) by an asynchronous logic feedback loop, allowing fast signal digitization using time-over-threshold. The offset of the differential amplifier is compensated using the output offset storage technique implemented with capacitors. This choice allows to do a local threshold trimming without need of a DAC correction.

The front-end is designed to have a noise at the latch input of around $100e^-$ for a sensor capacitance of 100fF, in order to have a threshold smaller than $1ke^-$. The total power consumption of the analog front-end is about 5 μW.

This design has been submitted in October 2014 and the testing procedure started in February 2015. Results in terms on gain, noise, ToT and offset compensation are presented. First irradiation results up to few hundred

MRad will be shown. This work has been performed in the framework of CERN RD53 Collaboration and has been funded by the CHIPIX65/INFN project.

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