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A Fast Turn-on ADC Scheme and its Engineering Validation

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In underground neutrino experiments, waveform digitization is often demanded at Giga-samples per second with occasional possible high instantaneous hit rate up to MHz range. As an alternative of regular flash ADC, a fast turn-on ADC scheme is presented in this paper. The ADC hibernates most of time during normal operation when the PMT is not hit and wakes up immediately to digitize the waveform once the detector channel is hit, which reduces total operating power significantly. The fast turn-on ability of a ramp-and-compare ADC implemented in an FPGA is tested.

Summary

For underground neutrino experiments, waveform digitization at Giga-samples per second is needed. Although the average hit rate is very low, it must prepare for certain high rate moments such as Supernova events that could bring the hit rate up to MHz level. A flash ADC will fulfill these requirements, but with large power consumption. The flash ADC digitizes input continuously while only very small fractions of sampling points become useful.

It will be ideal if the ADC can be kept sleep when there is no detector hit and be turned on immediately when the detector hit is present. This way the average power consumption of the ADC can be reduced significantly for the low duty cycle applications.

The fast turn on ability is tested in an ADC based on ramp-and-compare scheme. A pair of differential I/O pins of an Altera Cyclone III family FPGA are configured as the Bus LVDS bi-directional port. The port remains quiet during hibernating. Once the digitization process is started, the pins outputs 0 and 1 alternatively at 4 ns per step. The outputs with a programmable current limit drive a capacitor causing the voltages at the pins to ramp up and down. Both single ended and differential versions of the ADC has been implemented. In the single ended version, one pin is driven to ramp while the other pin is connected to the input signal. The input LVDS buffer inside the FPGA becomes the comparator and the flipping times of the comparator provide the crossing time of the input and the ramping voltage which is further digitized with TDC blocks implemented inside the FPGA. For differential version, the input voltages are coupled to the capacitor via two resistors causing the ramping voltages to move up or down and the crossing times to change.

The 4 ns upward or downward ramping samples the input voltage at 250 Ms/s and an ADC with 1 Gs/s can be implemented using 4 such channels with interleaving clocks. To reach a nominal 8-bit measurement precision, the TDC bin width of 16 ps is required which is not a challenge even in many FPGA devices today, and is a lot easier if implemented in ASIC. The measurement precisions can be further improved by ganging a few TDC channels together and making averages of there measurements.

Finer measurement precision sometimes is motivated by measuring small signals which can be alternatively fulfilled with non-linear ramping voltage. The ramping voltage is essentially a non-linear RC charging curve with different slopes at different voltages. The slower slope can be arranged near the input baseline so that very small input pulses can be digitized with finer effective measurement precisions.

The FPGA based ADC discussed in this paper consumes as few as one pair of I/O pins plus a capacitor per channel. Regardless fast turn-on feature, the ADC alone can be used in many cost and power sensitive applications.

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