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A 12bits 40MSPS SAR ADC with a redundancy algorithm and digital calibration for the ATLAS LAr calorimeter readout

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We present a SAR ADC with a generalized redundant search algorithm offering the flexibility to relax the requirements on the DAC settling time. The redundancy allows also a digital background calibration, based on a code density analysis, to compensate the capacitors mismatching effects. The total of capacitors used in this architecture is limited to a half of the one in a classical SAR design. Only 211 unit capacitors were necessary to reach 12bit resolution, and the switching algorithm is intrinsically monotonic. The design is fully differential featuring 12-bit 40MS/s in a CMOS 130nm 1P8M process.

Summary

Particle detectors, such as liquid argon (LArg) calorimeter used in ATLAS experiment at the LHC (Large Hadron Collider), generate very large dynamic signals which require a sophisticated front-end electronics. This readout includes the noise optimization stages (low noise preamplifier, and analog multi-gain filters), but one critical element is the following stage of Analog to Digital Converter (ADC). The requirements for our converter are 40MS/s at 12bits resolution. In this configuration pipeline architecture was widely used during this last years. But following the scaling of CMOS process, Successive Approximation Register (SAR) architecture appears to be more suitable in term of power dissipation. But the main limitations to deal with are the DAC settling time and the capacitors mismatching issue. This paper presents a SAR ADC with a generalized redundant search algorithm to relax the requirements on the DAC settling time and also allowing a digital background calibration to compensate the capacitors mismatching effects. The proposed architecture uses a DAC with a limited total capacitor (only 211 unit capacitors, for 12-bit resolution). A monotonic switching algorithm is used to minimize the dynamic power consumption compared to the conventional switching algorithm. The design is a fully differential 12bits SAR ADC working at 40MSPS with a 2Vpp full-scale input range. The conversion requires 14 steps for redundancy purposes. The digital background calibration algorithm for this ADC is based on a statistical approach. It uses only the original ADC core without adding any extra analog hardware on-chip or any additional reference channel in the design. The effectiveness of this calibration has been tested regarding capacitor mismatching. With a 5% capacitors mismatch error simulated in the DAC the INL errors found without calibration were +56.5/-56.8LSB and the ADC achieves 38.25dB of SNR, 40.53dB of SFDR and 5.56b ENOB. After calibration the improved INL errors are reduced to +1.6/-1.7LSB and the ADC achieves 69.54dB of SNR, 64.23dB of SFDR and 11.15b ENOB.

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