Past and Future of Microelectronics in HEP

A roadmap for R&D in microelectronics for Detector Builders

A. Marchioro
CERN/PH-ESE

Topics

- "Scaling": the mantra for industrial microelectronics 1965-2015
  - Where is industry going
- How did microelectronics benefit HEP for LHC 1.0
- How can microelectronics benefit HEP for the next 20 years
- Conclusions

The external environment

SCALING AND TRENDS

50th anniversary of G. Moore's paper

Electronics, Volume 38, Number 8, April 19, 1965

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

machine instead of being concentrated in a ce
addition, the improved reliability made possible
circuits will allow the construction of larger pro
Machines similar to those in existence today v
lower costs and with faster turn-around.

Present and future

By integrated electronics, I mean all the
nologies which are referred to as microelectro
well as any additional ones that result in elec

COMPUTER CONSOLES AT HOUSTON'S MANNED SPACECRAFT CENTER

From silent revolution come Hellenic hopes and Herculean challenge.

TECHNOLOGY

The Cybernated Generation

(See Cover)

Purring like contented kittens, the most remarkable support crew ever assembled kept unceasing vigil last week as Gemini spun through space with its two passengers. At Cape Kennedy and at the space complex in Houston, at Goddard Space Flight Center in Maryland and at 14 other sites from the Canary Islands to the South Indian Ocean, dozens of electronic computers guided, watched, advised and occasionally admonished the two astronauts. In fact, the Space Age's first orbiting digital computer, a hatbox-sized model that can make 7,000 separate calculations a second, went along for the ride in Gemini. No space effort—American or Russian—had ever before made such extensive use of the computer, or depended more on it.

swept forward by a great wave of technology, of which the computer is the ultimate expression, human society is surely headed for some deep-reaching changes.

"The electronic computer," says Dr. Louis T. Rader, a vice president of General Electric, "may have a more beneficial potential for the human race than any other invention in
As viewed by Sir Leon B
thoughtful head of Britair
Automation, the computer
mation will bring "the greate
in the whole history of mank
public, too, has begun to sens
er of the computer for good
Cartoonists delight in giving
robotlike stature and minds
own that like to play tricks o
mortals, and computers have
the mute but decisive villain
recent bestselling novels. Tl
of computers, called cybern
k word for steersman, is the
of an endless round of study
ussion devoted to pondering
problems and opportunities
front what social scientists call
ernated generation."

Caesar, unto God. As the most
ated and powerful of the tools
by man, the computer has al-

ready affected whole areas of society, opening up vast new possibilities by its extraordinary feats of memory and calculation. It is changing the world of business so profoundly that it is producing a new era in Arnold Toynbee's "permanent industrial revolution." It has given new horizons to the fields of science and medicine, changed the tech-

element in the technical arsenal of the world's most technologized nation. In 1951 there were fewer than 100 computers in operation in the U.S.; today 22,500 computers stand in offices and factories, schools and laboratories—four times as many as all the computers that exist elsewhere in the free world. Only eleven years ago, U.S. industry bought its first computer; today some single companies use as many as 200 computers.

The computer already has been put to work at more than 700 specific tasks, both mundane and exotic, from bookkeeping to monitoring underground nuclear explosions. Computers control the flow of electric current for much of the nation, route long-distance telephone calls, set newspaper type, even dictate just how sausage is made. They navigate ships and planes, mix cakes and cement, prepare weather forecasts, check income tax returns, direct city traffic and diagnose human—and machine—ailments. They render unto Caesar by sending out the monthly bills and reading the squiggly hieroglyphics on bank checks, and unto God by counting the ballots of the world's Catholic bishops at sessions of the Ecumenical Council in St. Peter's Basilica.

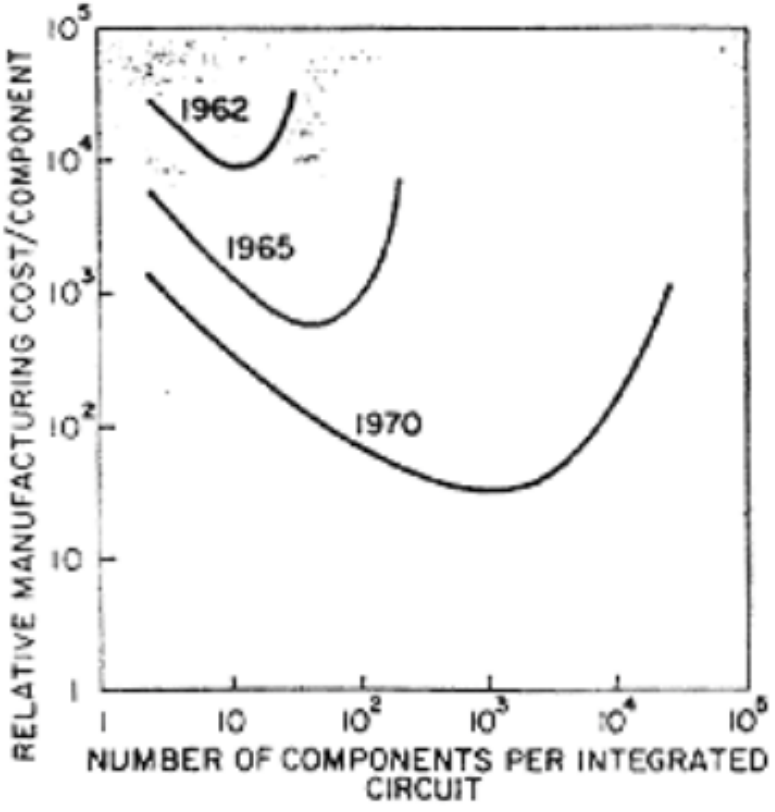
"SURE, SURE, I CAN SEE THE LABOR SAVING POSSIBILITIES, BUT HOW DO WE COPE WITH ALL THE LEISURE TIME IT'S BOUND TO PRODUCE?"

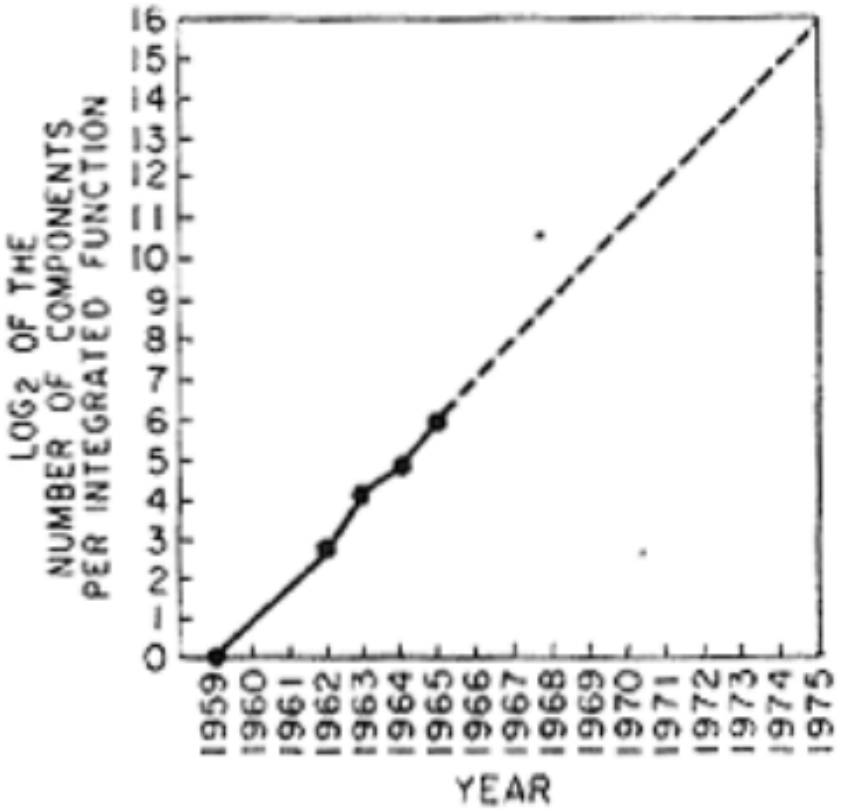
While man's exploration of space would be impossible without computers, the biggest changes worked by these remarkable machines are taking place right on earth. Just out of its teens, the computer is beginning to affect the very fabric of society, kindling both wonder and widespread apprehension. Is the computer a friend or enemy of man? Will it cause hopeless unemployment by speeding automation, that disquieting term that it has brought into the language? Will it devalue the human brain, or happily free it from drudgery? Will it ever learn to think for itself? The answers will not be in for quite a while, but one thing is already clear:

world's most technologized nation. In 1951 there were fewer than 100 computers in operation in the U.S.; today 22,500 computers stand in offices and factories, schools and laboratories—

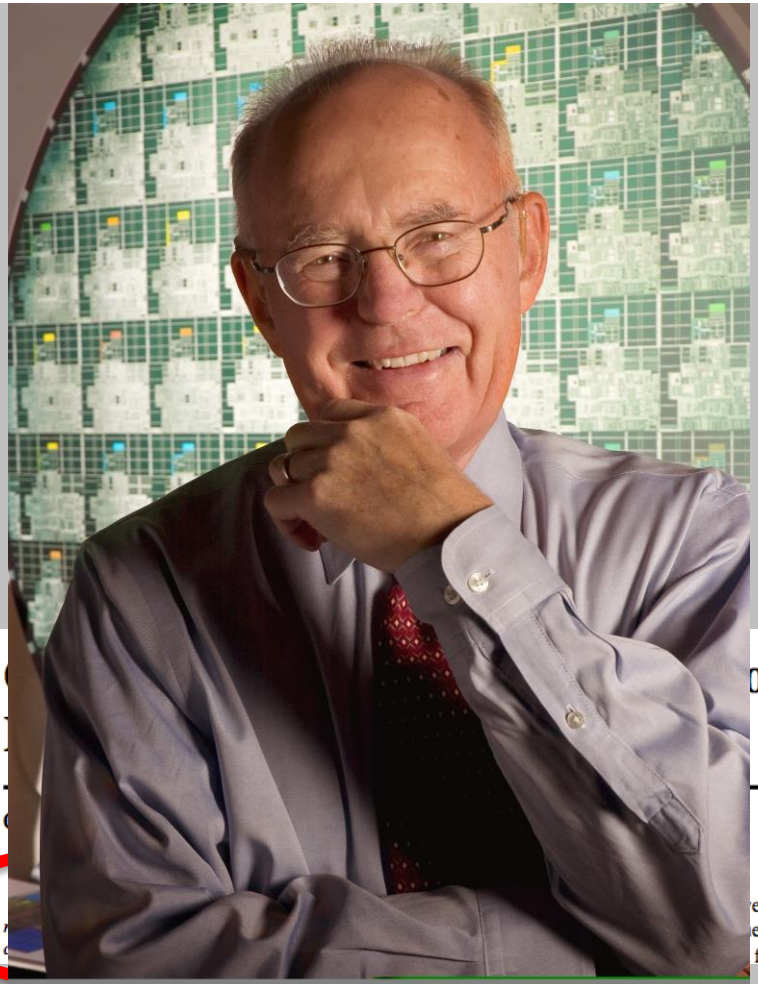
monished the two astronauts. In fact, the Space Age's first orbiting digital computer, a hatbox-sized model that can make 7,000 separate calculations a second, went along for the ride in

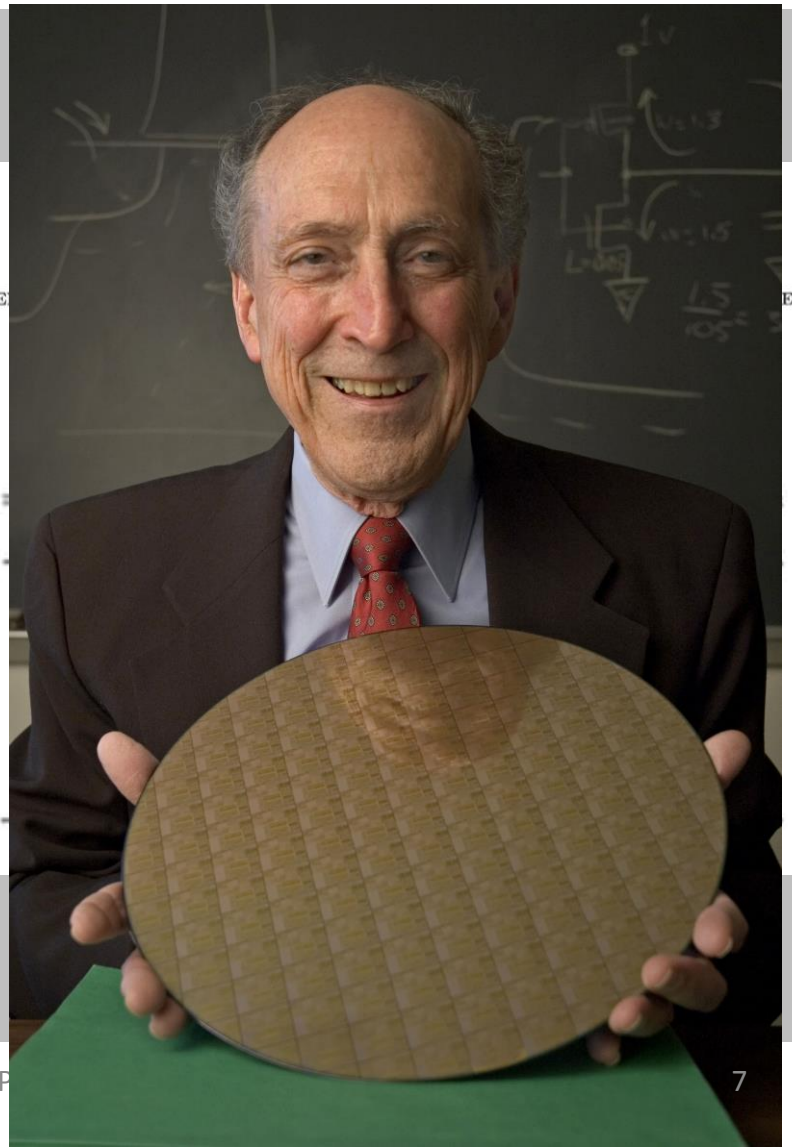
50th anniversary of G. Moore's paper



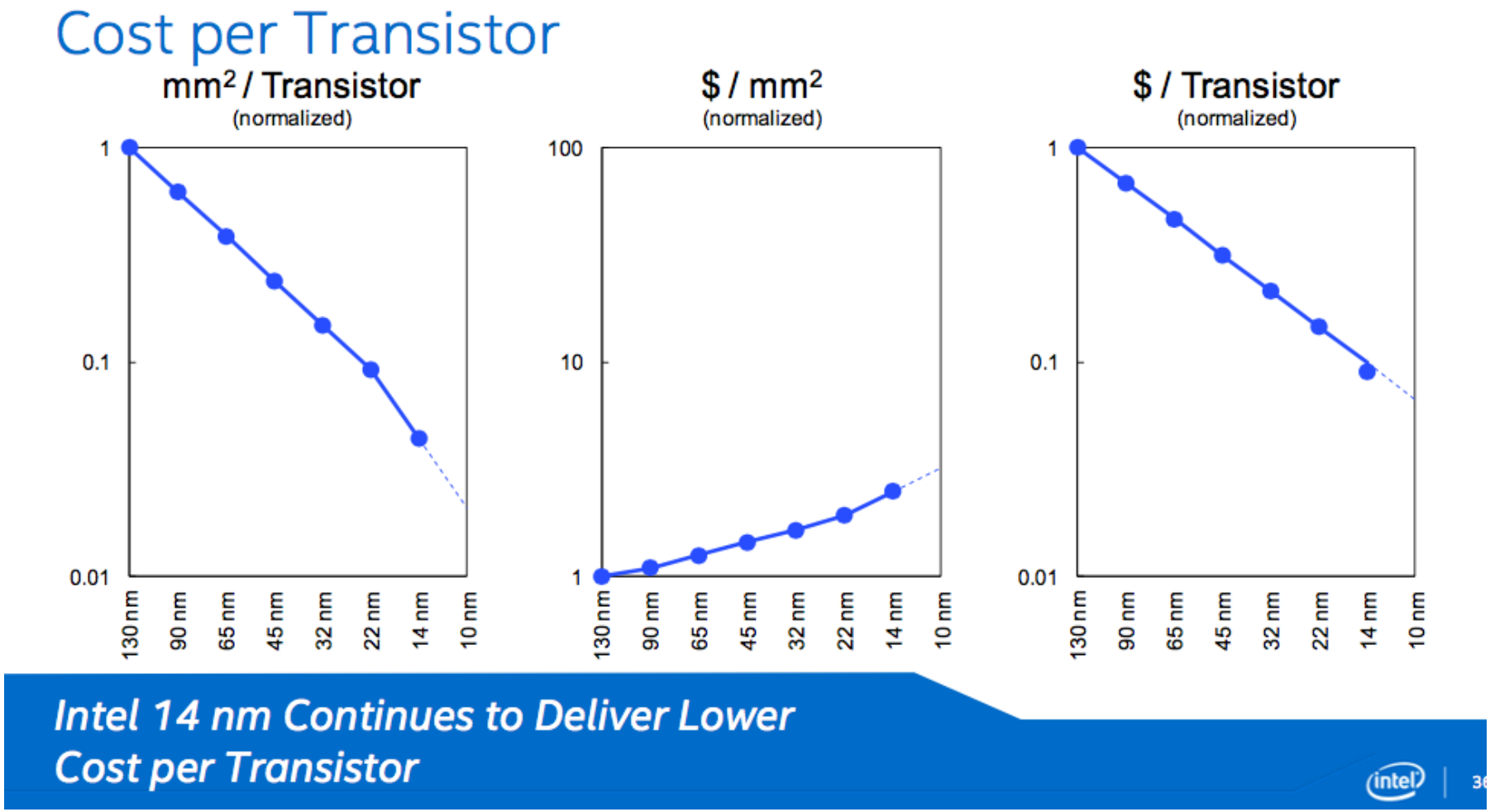


Who's scaling





1965 statement still true in 2014



from M. Bohr, Intel IDF 2014

Scaling revisited

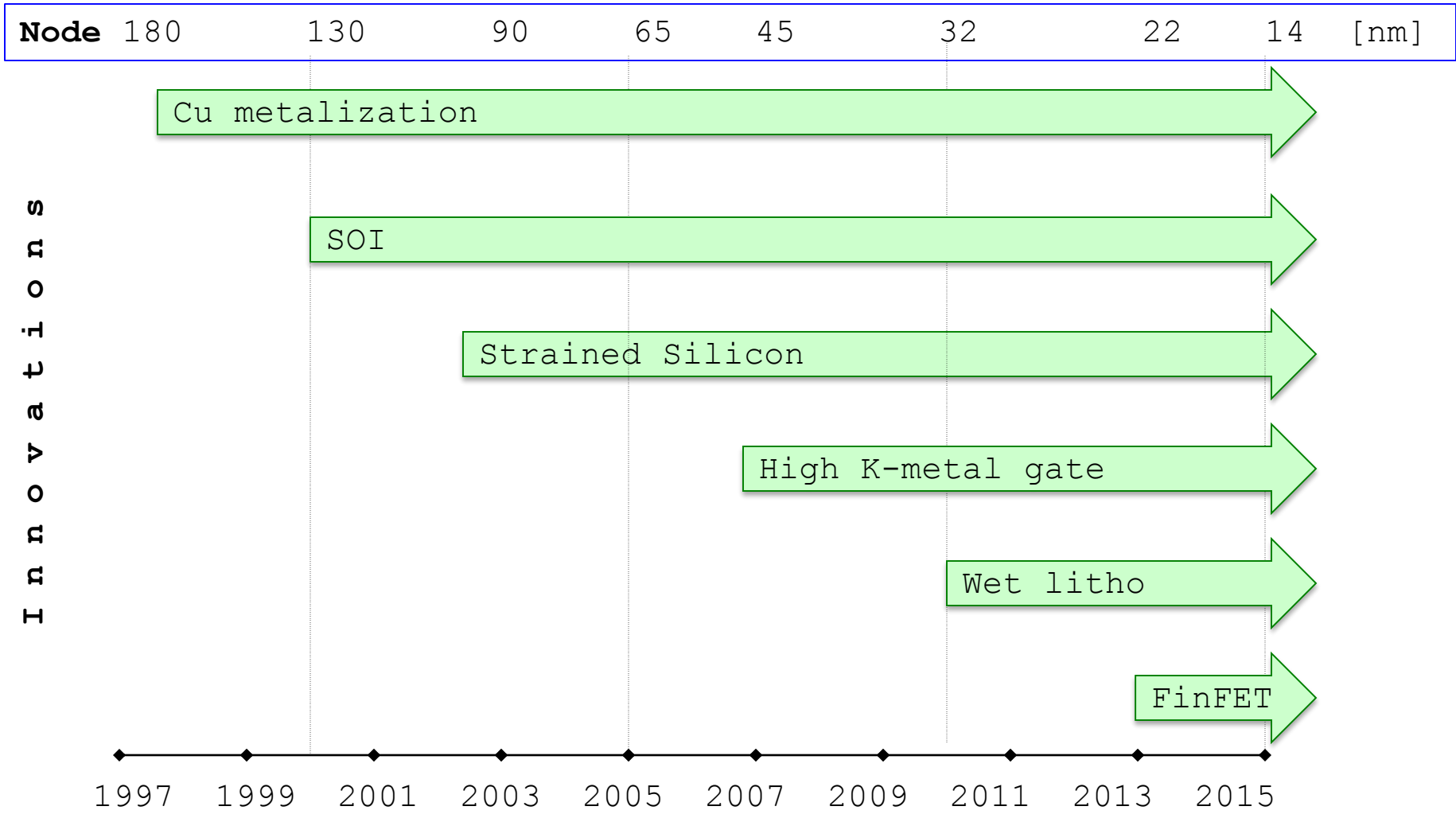
The fundamental objective that the microelectronics industry has pursued in the past 50 years may not have been:

"How to make transistors smaller and smaller at each new generation"

but rather:

"How to make transistors cheaper and cheaper at each new generation"

Timeline of significant innovations



Integrated Circuits at the (Energy-Constrained) End of Silicon Scaling

Rob A. Rutenbar

THE END OF CMOS SCALING

TECH

Moore's Law Shows Its Age

Intel's former chief architect: Moore's law will be dead within a decade

By Joel Hruska on August 30, 2013 at 8:30 am | 50 Comments

DARK SILICON AND THE END OF MULTICORE SCALING

Thomas Skotnick
H.-S. Philip Wong

Appears in the Proceedings of the 38th International Symposium on Computer Architecture (ISCA '11)

Dark Silicon and the End of Multicore Scaling

A KEY QUESTION FOR THE MICROPROCESSOR RESEARCH AND

WHETHER SCALING MULTICORES WILL PROVIDE THE PERFORM

Surviving the End of Scaling of Traditional Micro Processors in HPC

Robert G. Clapp
Mencer,

THE END OF DENNARD SCALING

APRIL 15, 2013 ADRIAN MCMENAMIN

The End of Moore's Law?

The current economic boom is likely due to increases in computing speed and decreases in price. Now there are some good reasons to think that the party may be ending.

MYSEMICONDAILY

Semiconductor News and Social Connections

BLOG PHOTOS PARTNERS ABOUT US CONTACT

Posted on July 9, 2014 by sdavis

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The End of Scaling?

By Jeff Dorsch

Are we reaching the end of scaling?

Yes and no.

TECH 11/13/2011 @ 5:42PM | 1,300 views

The End of Semiconductor Scaling

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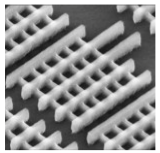

I have repeatedly heard that there is a brick wall facing the world of semiconductors ever since I first worked for National Semiconductor in the late 1970s. Scaling was destined to end, and once it did, the economic force behind the world of semiconductors would come to a grinding halt.

In the early 1980s a co-worker explained to me with conviction that

Replica-of-first-transistor (Photo credit: Revol-web)

Technologies around the corner

- FinFet
- FDSOI
- TSVs
- Wafer-to-wafer stacking
- Truly 3D monolithic CMOS
- New materials (III-IV, Ge, GaN, SiC, etc.)
- New phenomena: non kT/q controlled thresholds slopes

FinFET: a new device with a long incubation

Solid-State Electronics Vol. 27, Nos. 8/9, pp. 827–828, 1984
Printed in Great Britain

0038-1101/84 $3.00 + .00
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CALCULATED THRESHOLD-VOLTAGE CHARACTERISTICS OF AN XMOS TRANSISTOR HAVING AN ADDITIONAL BOTTOM GATE

(*Received* 30 *May* 1983; *in revised form* 24 *August* 1983)

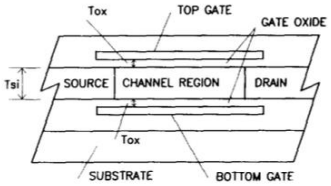


Fig. 1. Schematic cross-sectional structure of an XMOS transistor having an additional bottom gate which is symmetrically placed to a top gate with a channel region between them. "*X*" originates from Greek capital letter of xi as this structure resembles its shape.

Electronic Device Division, Electrotechnical Laboratory, Sakura-mura, Ibaraki, 305, Japan

T. SEKIGAWA and Y. HAYASHI

Hitachi(?)– 1984

NEW EFFECTS OF TRENCH ISOLATED TRANSISTOR USING SIDE-WALL GATES

K. Hieda, F. Horiguchi, H. Watanabe, K. Sunouchi, I. Inoue and T. Hamamoto

VLSI Research Center, Toshiba Corporation
Komukai, Saiwai-ku, Kawasaki, 210 Japan

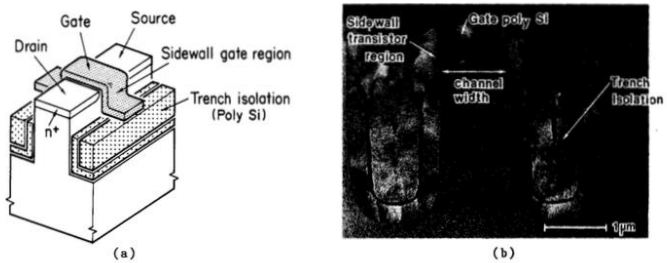


Fig. 1. (a) Schematic cross section of trench isolated transistor using side-wall gates (TIS). (b) SEM micrograph of the cross section along the direction of gate width.

32.2

IEDM 87-737

Toshiba– 1987

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 38, NO. 6, JUNE 1991 1419

Impact of the Vertical SOI "DELTA" Structure on Planar Device Technology

Digh Hisamoto, *Member, IEEE*, Toru Kaga, *Member, IEEE*, and Eiji Takeda, *Senior Member, IEEE*

***Abstract*—A fully depleted lean channel transistor (DELTA) with its gate incorporated into a new vertical ultra-thin SOI structure is presented. In the deep-submicrometer region, selective oxidation produces and isolates an ultra-thin SOI MOSFET that has high crystalline quality, as good as that of conventional bulk single-crystal devices. Experiments and three-dimensional simulations have shown that this new gate structure has effective channel control, and that the vertical ultra-thin SOI structure provides superior device characteristics: reduction in short-channel effects, minimized subthreshold swing, and high transconductance.**

is required. Moreover, it is evident that these st
are difficult to contact to the substrate, and thus suf
a substrate floating effect.

The second concept makes the device thickness
than the depletion-layer width to intentionally dep
channel. This can be done with thin-film SOI tech
such as SIMOX and recrystallization [7], [8]. T
cept is ideal because the structure has the same n
conventional MOSFET's, however, it requires
ultra-thin SOI substrates, a difficult task. Still, a

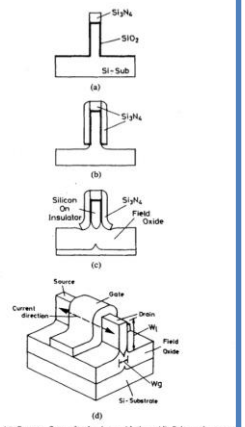


Fig. 1. (a)–(c) Process flow of selective oxidation. (d) Schematic cross section of DELTA.

Hitachi – 1991

Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?

D. J. Frank, S. E. Laux and M. V. Fischetti

IBM Research Division, T. J. Watson Research Center
P.O. Box 218, Yorktown Heights, NY 10598

Conclusions

In summary, it appears that high performance Si MOSFETs can be scaled down to gate lengths of order 30 nm. Such devices are still suitable for digital circuitry, and may have transconductances as high as 2300 mS/mm and ring oscillator speeds near 1 ps. The technology needed to do this includes thickness control of very thin layers, dual gate alignment, very abrupt doping profiles and gate work function control. A high thermal conductivity method of removing heat from such devices would also need to be found.

References

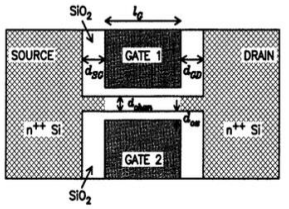
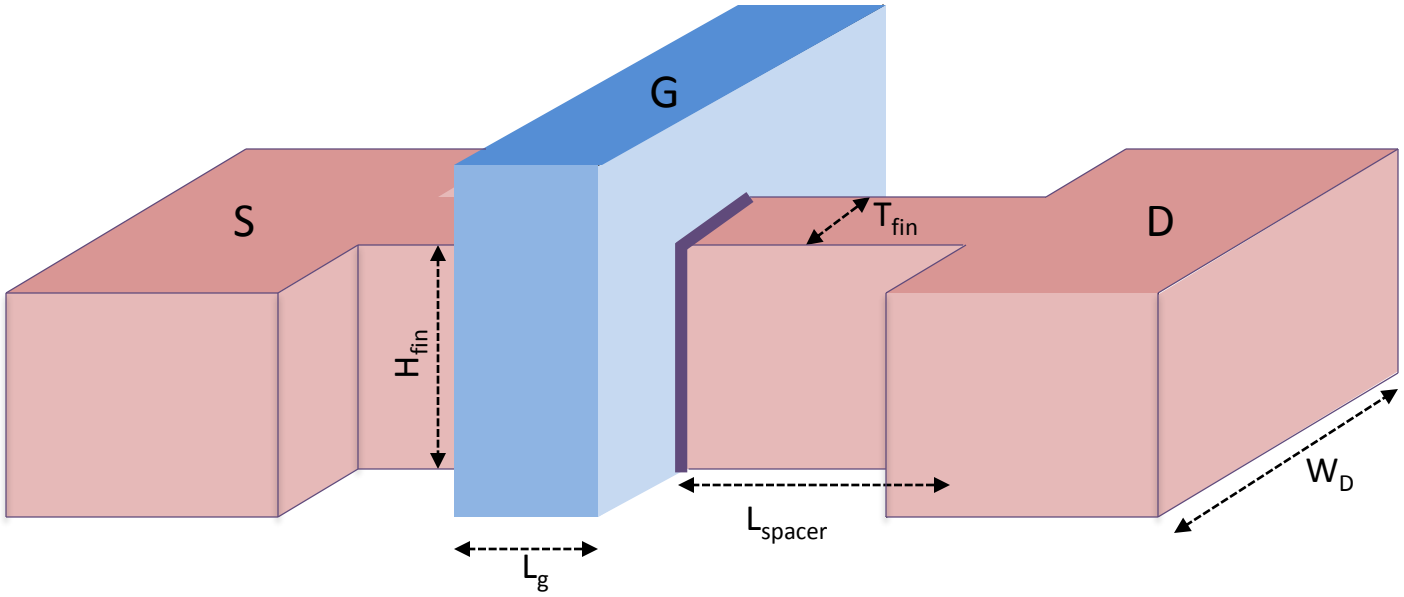


Fig. 1. Dual-gate MOSFET cross-section. Our simulations all use $d_{ox} = 3$ nm, $d_{SD} = d_{GD} = 0.3 \times l_G$, and 10^{20} cm^{-3} n-type source and drain doping.

21.1

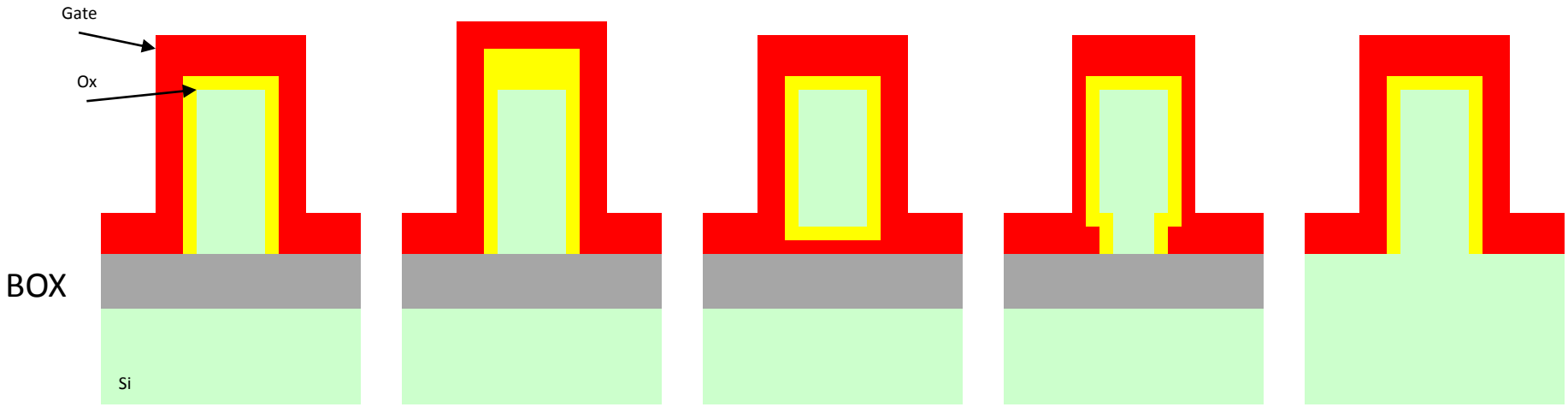
IBM – IEDM 1992

FinFET Detail

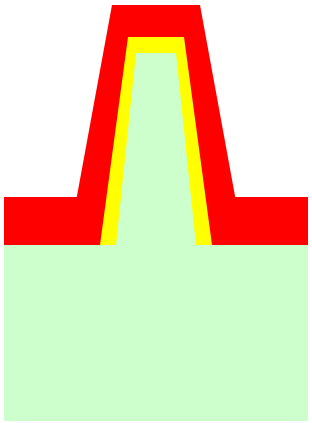


- L_g same for all devices
- H_{fin} >> Tfin
- Top Ox same as Lateral Ox -> Tri-Gate,
  - if >> Lateral Oxide -> FinFET
- $W_{fin} = 2 * L_{fin} (+T_{fin})$
- $W_{S,D} >> T_{fin}$

Multi-Gate variations

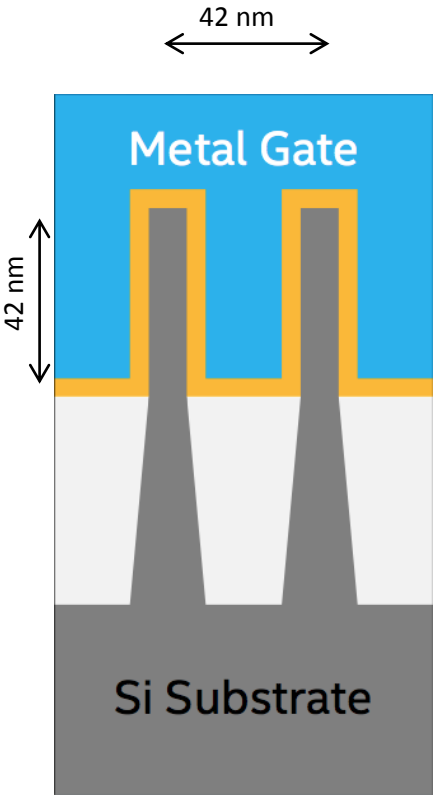


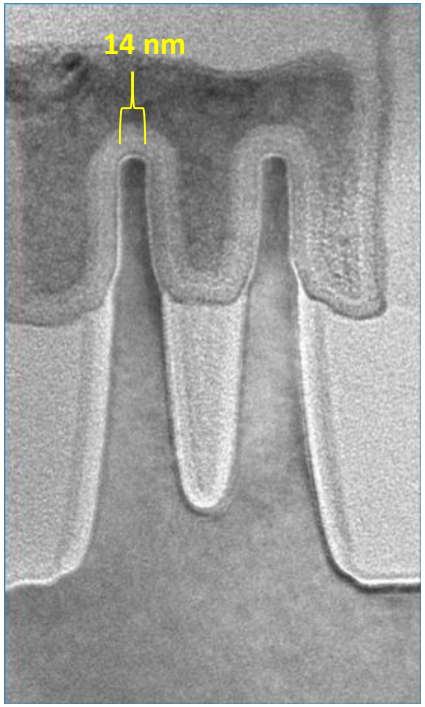
SOI tri-gate | SOI two-gate | Gate-All-Around | Omega-gate | Si-bulk tri-gate

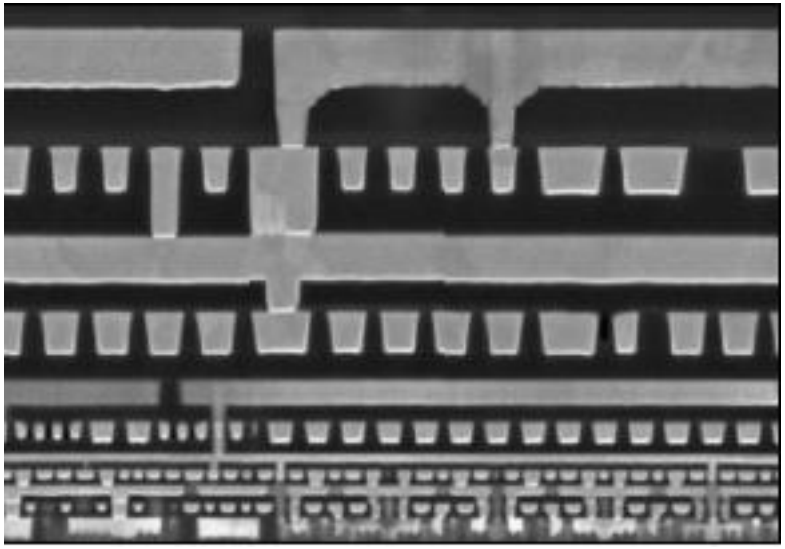


Intel's tri-gate

Intel TRI-Gate





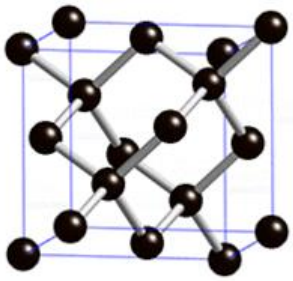


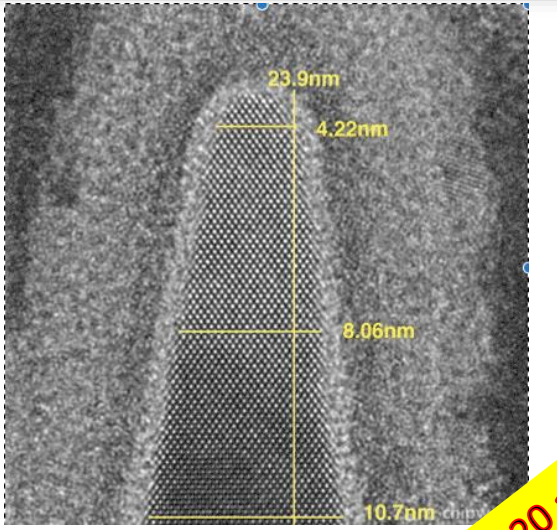
Metalization detail

Source: Intel

Typical FinFET dimensions

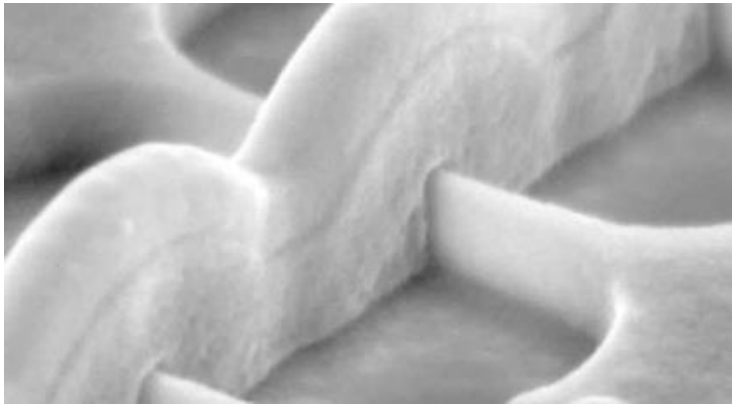
Year of Production	2013	2015	2017	2019	2021	2023	2025	2028
FinFET Fin Width (new) (nm)	7.6	7.2	6.8	6.4	6.1	5.7	5.4	5.0



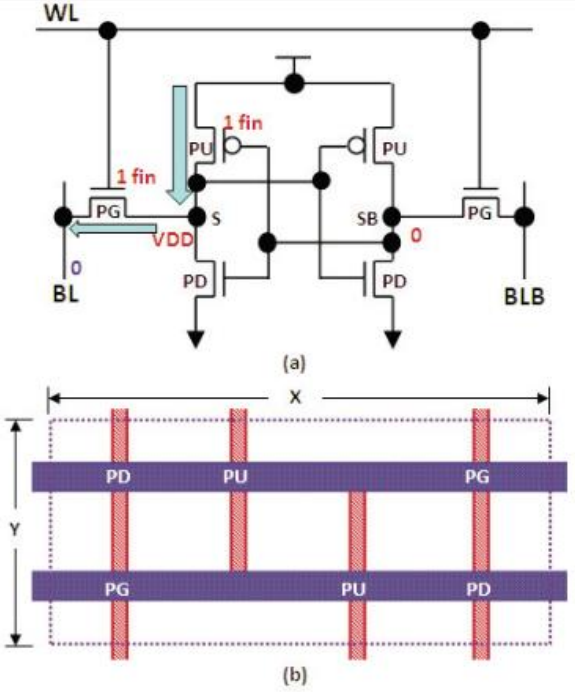


This FinFET has EXACTLY 20 atoms across at half-height

TSMC FinFET



16 nm FinFET from TSMC



FinFET based SRAM,
0.07 μm^2 per bit,
presented at ISSCC 2014

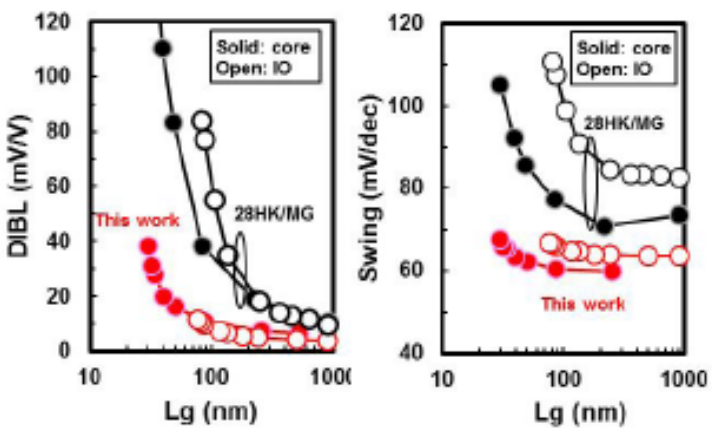
FinFET @ TSMC

An Enhanced 16nm CMOS Technology Featuring 2nd Generation FinFET Transistors and Advanced Cu/low-k Interconnect for Low Power and High Performance Applications

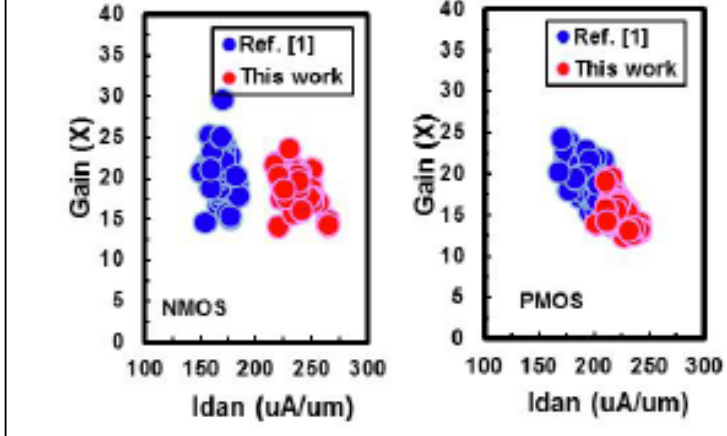
Shien-Yang Wu, C.Y. Lin, M.C. Chiang, J.J. Liaw, J.Y. Cheng, S.H. Yang, S.Z. Chang, M. Liang, T. Miyashita, C.H. Tsai, C.H. Chang, V.S. Chang, Y.K. Wu, J.H. Chen, H.F. Chen, S.Y. Chang, K.H. Pan, R.F. Tsui, C.H. Yao, K.C. Ting, T. Yamamoto, H.T. Huang, T.L. Lee, C.H. Lee, W. Chang, H.M. Lee, C.C. Chen, T. Chang, R. Chen, Y.H. Chiu, M.H. Tsai, S. M. Jang, K.S. Chen, Y. Ku

168, Park Ave. 2, Hsinchu Science Park, Hsinchu, Taiwan, R.O.C., Email: shien-yang_wu@tsmc.com

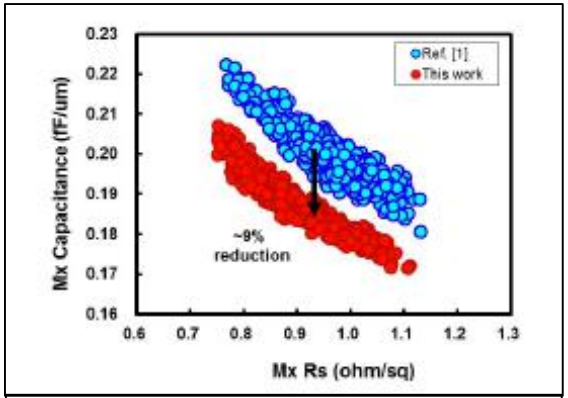
Taiwan Semiconductor Manufacturing Company



TSMC: 16nm FinFET vs. 28nm HKMG

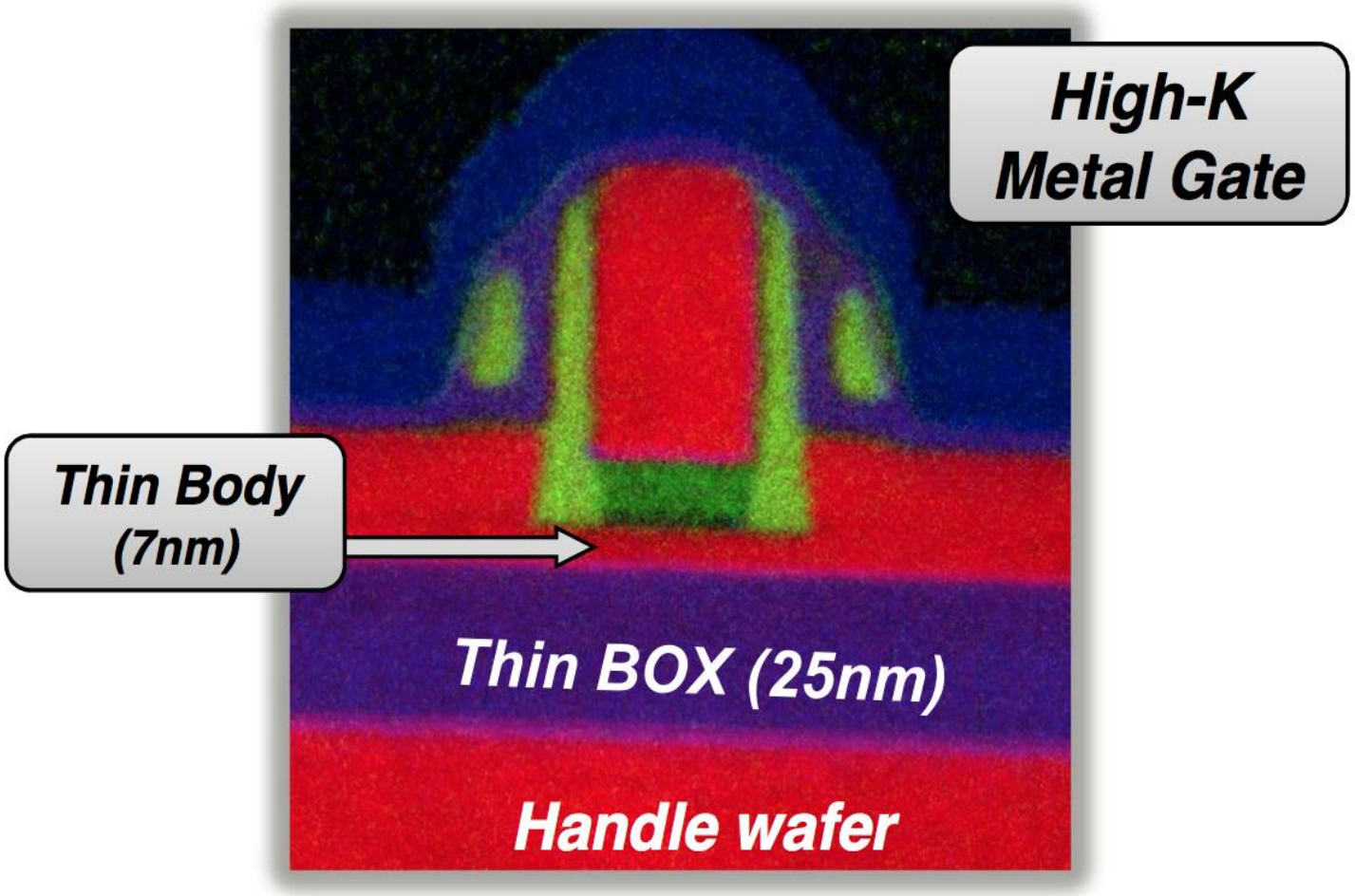


TSMC: 16nm FinFET gain



TSMC: 16nm FinFET Low Intermetal C

STM FDSOI



28nm FDSOI from ST

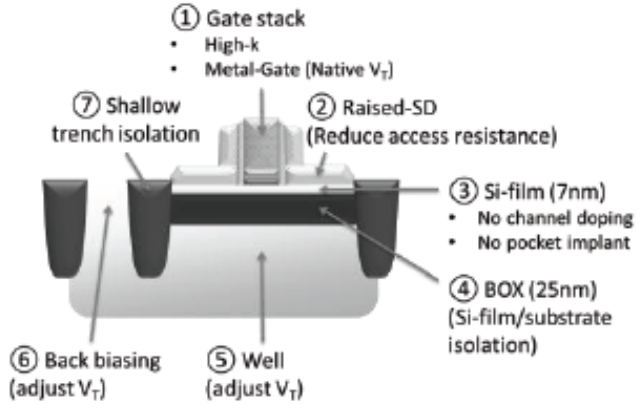


Fig.1: UTBB FD-SOI cross section view. Device V_T is set by the gate stack and adjusted by well doping type [2-3]. Wide V_T tuning is feasible by back-biasing changing the well bias.

Dynamic Single-P-Well SRAM bitcell characterization with Back-Bias Adjustment for Optimized Wide-Voltage-Range SRAM Operation in 28nm UTBB FD-SOI

O. Thomas[1,2], B. Zimmer[1], S. O. Toh[1], L. Ciampolini[3], N. Planes[3], R. Ranica[3] P. Flatresse[3] and B. Nikolić[1]

[1] Berkeley Wireless Research Center, Berkeley, CA, United States, email : olivier.thomas@cea.fr – [2] CEA-LETI Minatec Campus, 38054 Grenoble Cedex 9, France, Crolles – [3] ST Microelectronics, 38926 Crolles, France

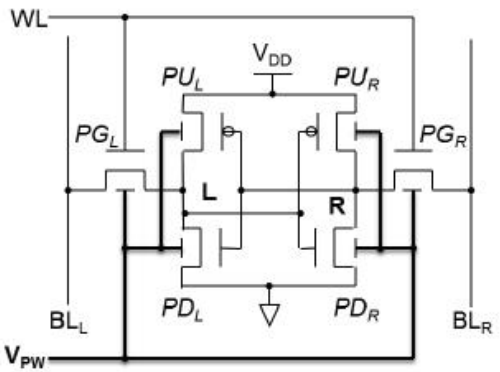


Fig.3: SPW bitcell schematic. Back gate of NMOS (PG, PD) and PMOS (PU) devices are electrically connected by the common P-well.

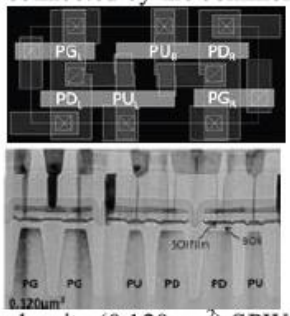
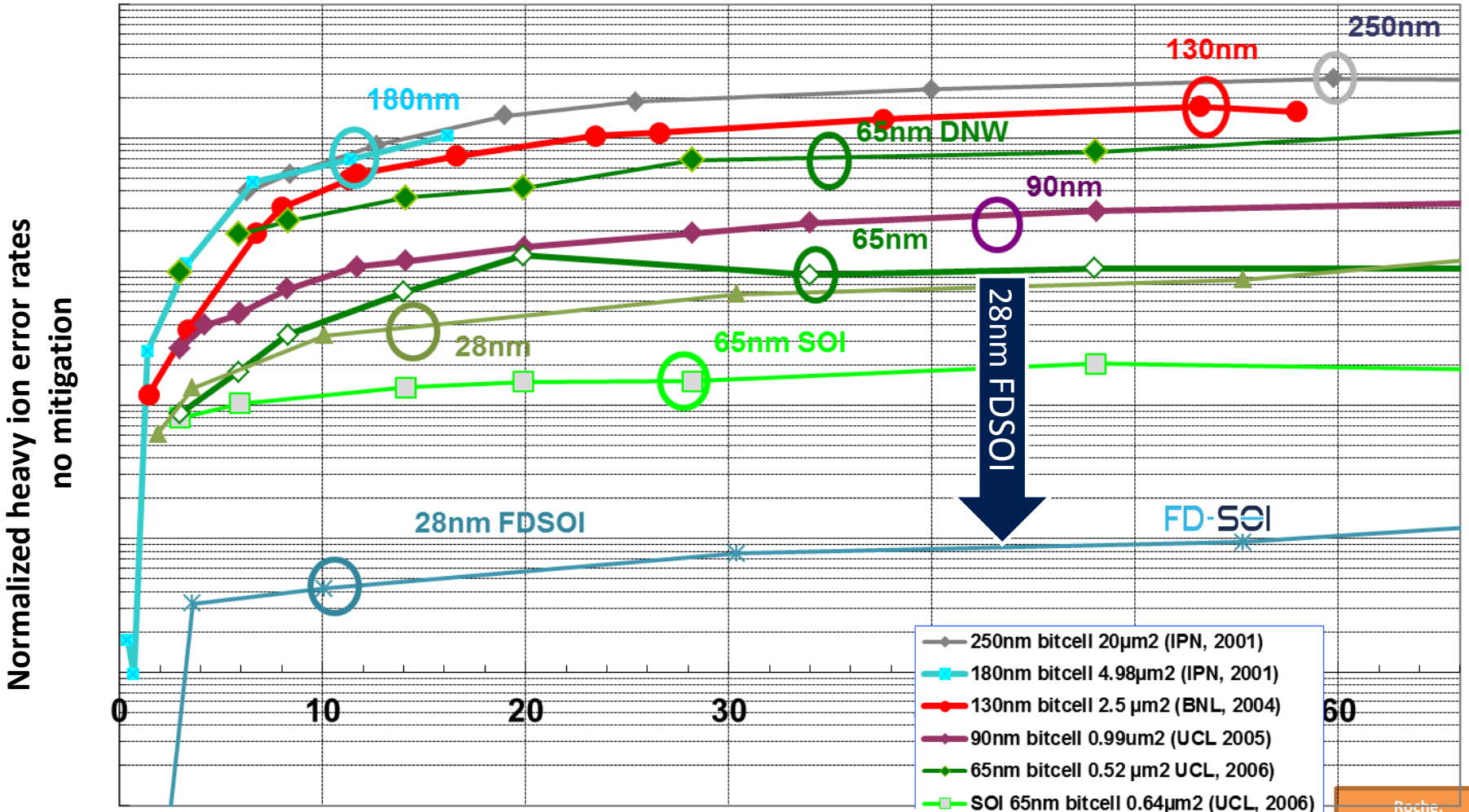


Fig.6: High density (0.120µm^2) SPW bitcell layout and TEM cross section [8]. 28nm High-k metal-gate technology implementing 7nm Si-film relying on 25nm BOX thickness [9].

Soft Error Rate in SRAMs on 28nm FDSOI

- **Lowest (best) error rates against space ions in 28nm UTBB FDSOI**
  - 3 and 2 decades lower respectively than CMOS 65nmn and 28nm (no SEGR/SEL)



Courtesy of P. Roche, STMicroelectronics

Roche, ESA QCA Days 07'09'11' NSREC'14

Advanced pixel stacking Imager

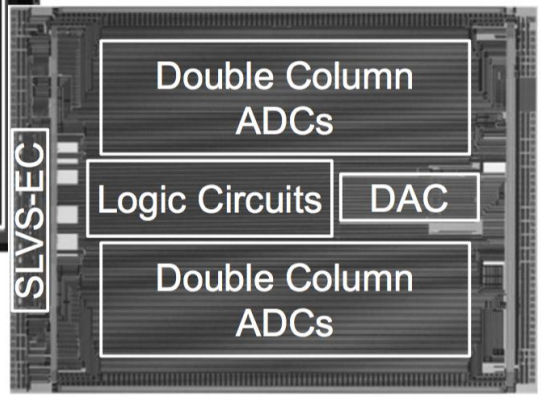
6.1 A 1/1.7-inch 20Mpixel Back-Illuminated Stacked CMOS Image Sensor for New Imaging Applications

Atsushi Suzuki[1], Nobutaka Shimamura[1], Toshiki Kainuma[1], Naoki Kawazu[1], Chihiro Okada[1], Takumi Oka[1], Kensuke Koiso[2], Atsushi Masagaki[1], Yoichi Yagasaki[3], Shigeru Gonoi[4], Tatsuya Ichikawa[1], Masatoshi Mizuno[5], Tatsuya Sugioka[1], Takafumi Morikawa[1], Yoshiaki Inada[1], Hayato Wakabayashi[1]

[1]Sony, Atsugi, Japan,
[2]Sony Semiconductor, Kikuyou, Japan,
[3]Sony, Shinagawa, Japan,
[4]Sony LSI Design, Fukuoka, Japan

90nm 1P4M MOS

65nm 1P7M Logic

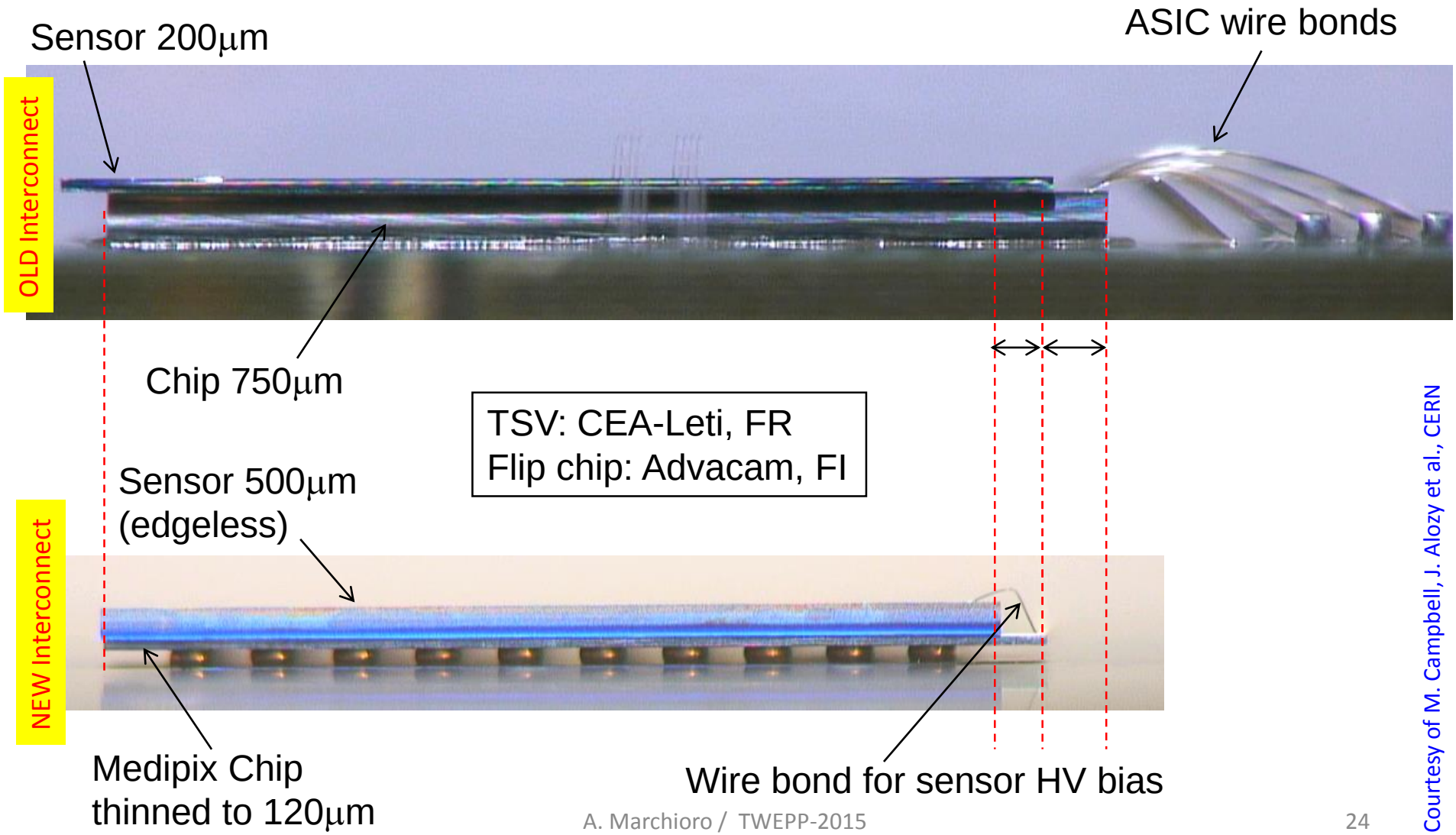


Bottom part

Pixel size		1.43μm (H) x 1.43μm (V)
Frame rate	Still	30fps at 20Mp 12b w/ multiple sampling 90fps at 20Mp 10b w/ data compression
	Movie	120fps at 16Mp 10b w/ data compression 240fps at 4Mp 10b
	Two streams	60fps at 4Mp 12b and 16Mp 10b
Saturation signal		9700e^- at 60ºC
Sensitivity (typical value F5.6)		7922e^-/lx·s (Green pixel)
Conversion gain		76.6μV/e^-
RMS random noise		1.3e^- @20Mp 30fps w/ multiple sampling (analog gain : 27dB)
Dynamic range		72dB at 12b

Chips in two different technologies
Wafer-to-wafer bonding

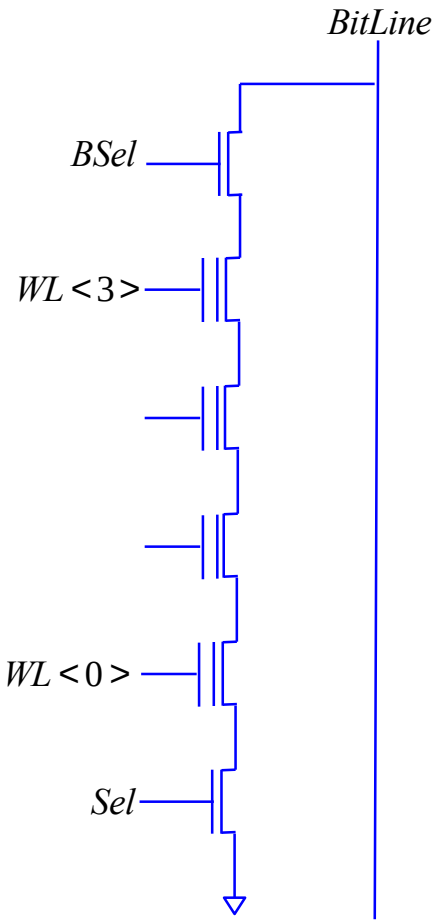
TSVs on Medipix3



Courtesy of M. Campbell, J. Alozy et al., CERN

Monolithic 3D for memories (1)

NAND Flash Architecture

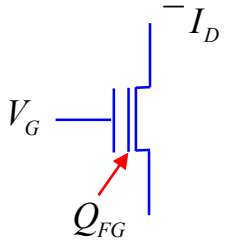


Flash Transistor has two gates, an external and a "Floating" gate.
The Floating gate modifies the V_t of the transistor
(from negative to positive if programmed)

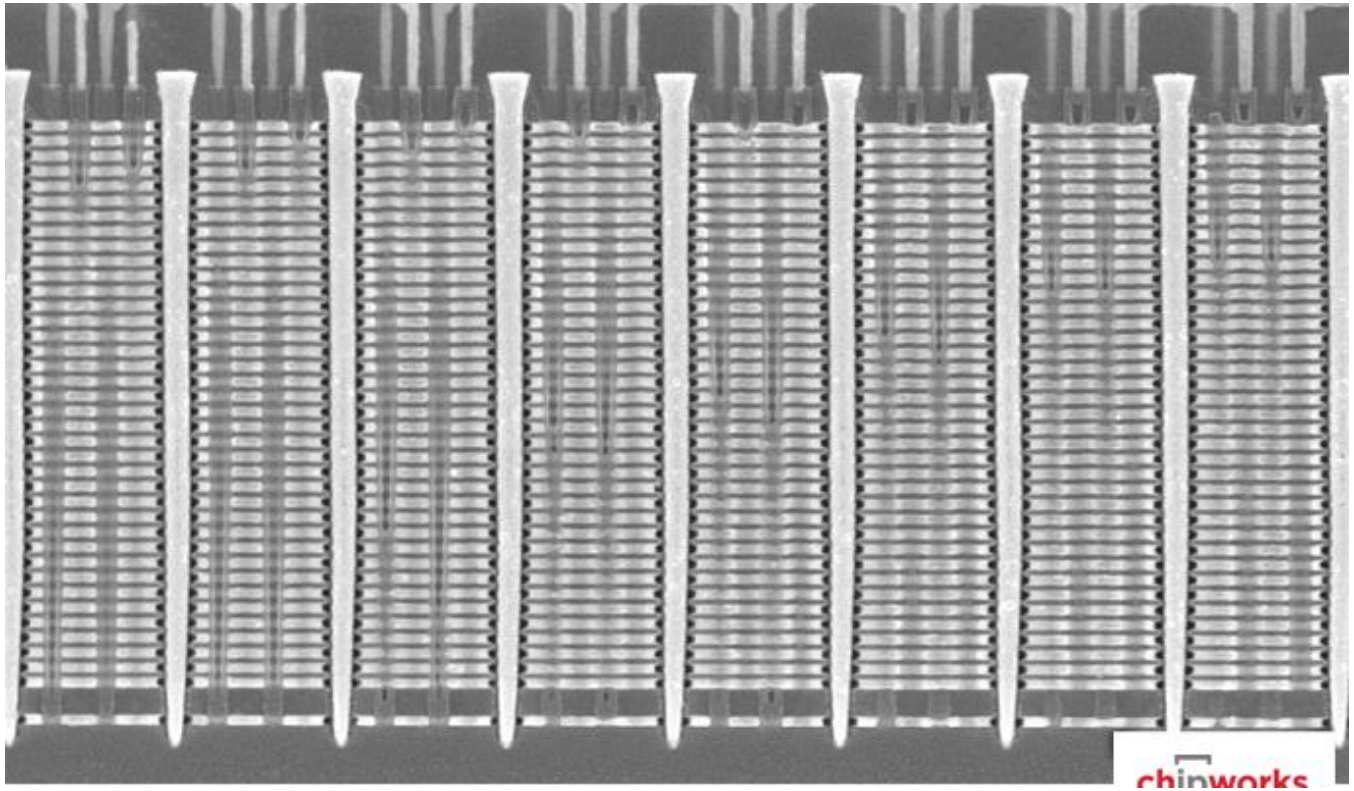
$V_g = 0 \quad Q_{FG} = 0 \quad I_D = 0$

$V_g = 0 \quad Q_{FG} = q_P \quad I_D > 0$

$V_g = V_h \quad Q_{FG} = X \quad I_D > 0$ (transistor is conductive)



Monolithic 3D for memories (2)



Courtesy of *Chipworks*

Note:
Each memory bit is stored as trapped charge on the gate of a transistor.

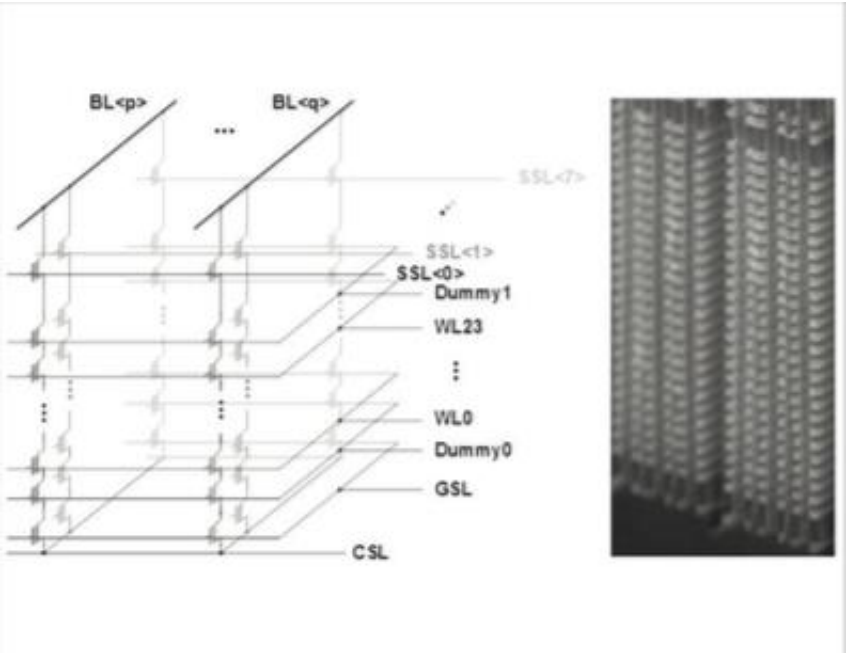
Today a "1" is represented by something like 500-1000 e^- trapped, implying a leakage current of << 1 e^-/month for a 10 years retention.

Monolithic 3D for memories (2')

19.5 Three-Dimensional 128Gb MLC Vertical NAND Flash-Memory with 24-WL Stacked Layers and 50MB/s High-Speed Programming

Ki-Tae Park, Jin-man Han, Daehan Kim, Sangwan Nam, Kihwan Choi, Min-Su Kim, Pansuk Kwak, Doosub Lee, Yoon-He Choi, Kyung-Min Kang, Myung-Hoon Choi, Dong-Hun Kwak, Hyun-wook Park, Sang-won Shim, Hyun-Jun Yoon, Doohyun Kim, Sang-won Park, Kangbin Lee, Kuihan Ko, Dong-Kyo Shim, Yang-Lo Ahn, Jeunghwan Park, Jinho Ryu, Donghyun Kim, Kyungwa Yun, Joonsoo Kwon, Seunghoon Shin, Dongkyu Youn, Won-Tae Kim, Taehyun Kim, Sung-Jun Kim, Sungwhan Seo, Hyung-Gon Kim, Dae-Seok Byeon, Hyang-Ja Yang, Moosung Kim, Myong-Seok Kim, Jinseon Yeon, Jaehoon Jang, Han-Soo Kim, Woonkyung Lee, Duheon Song, Sungsoo Lee, Kye-Hyun Kyung, Jeong-Hyuk Choi

Samsung Semiconductor, Hwasung, Korea

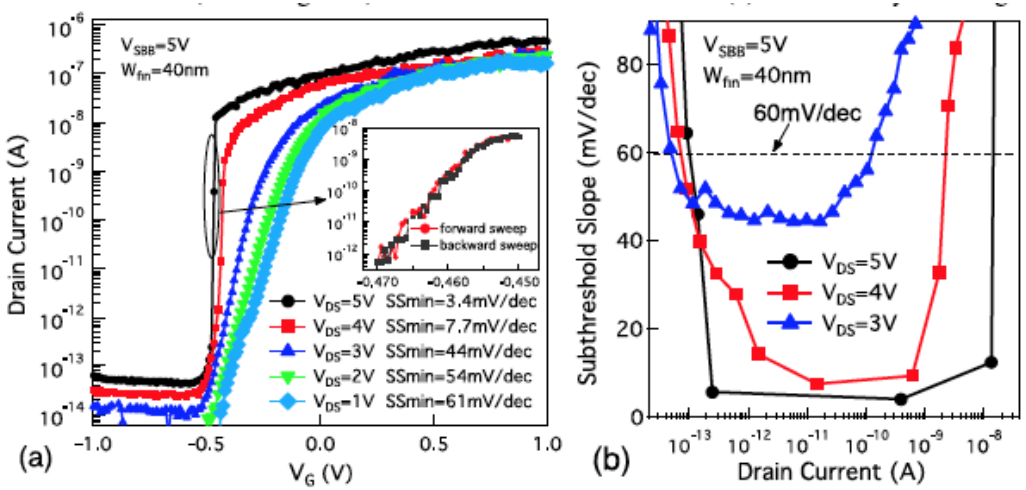


Future Devices: Steep Swing FETs

A Schottky-Barrier Silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 Decades of Current

Jian Zhang, Michele De Marchi, Pierre-Emmanuel Gaillardon, Giovanni De Micheli

Integrated Systems Laboratory, EPFL, Lausanne, Switzerland
Tel: +41 21 6938164, E-mail: jian.zhang@epfl.ch



(Notice that unfortunately the SS is steep only for high V_{DS}!)

Conclusion:
Is scaling really finished in industry?

- If one calls “scaling” only the (2D) miniaturization of transistors, then definitively Dennard’s scaling is closer to saturation than Moore’s.

- If instead one calls scaling the reduction in cost (somehow) of the $/transistor on a chip, then surely several more generations are ahead of us.

The early benefits

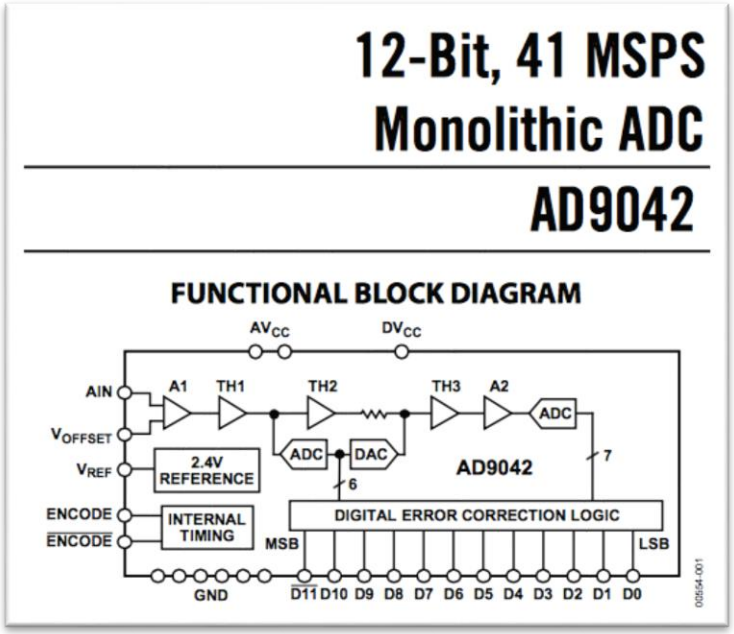
MICROELECTRONICS IN HEP 1.0

Major benefits

- Functionality
  - The ¼ um generation made the integration of 128 FE channels and relative (analog/digital) buffering in a single chip much easier and more economical.
  - Signal processing FE chips with 16+ ADCs, true DSP and buffering have also been realized (e.g. SALTRO for Alice).
- Speed
  - Gbit/sec class links also required a fast and low power technology
- RH
  - Magically (LITERALLY) gate oxides of ~ 5 nm thickness appeared in this generation and this (and another little layout trick) saved the day with respect to Total Dose damaging effects.

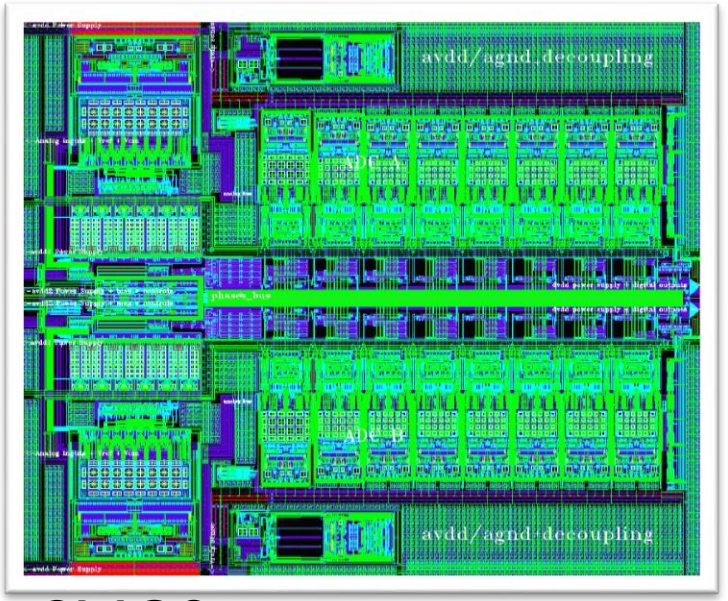
RH ADCs, circa 2002

Commercial



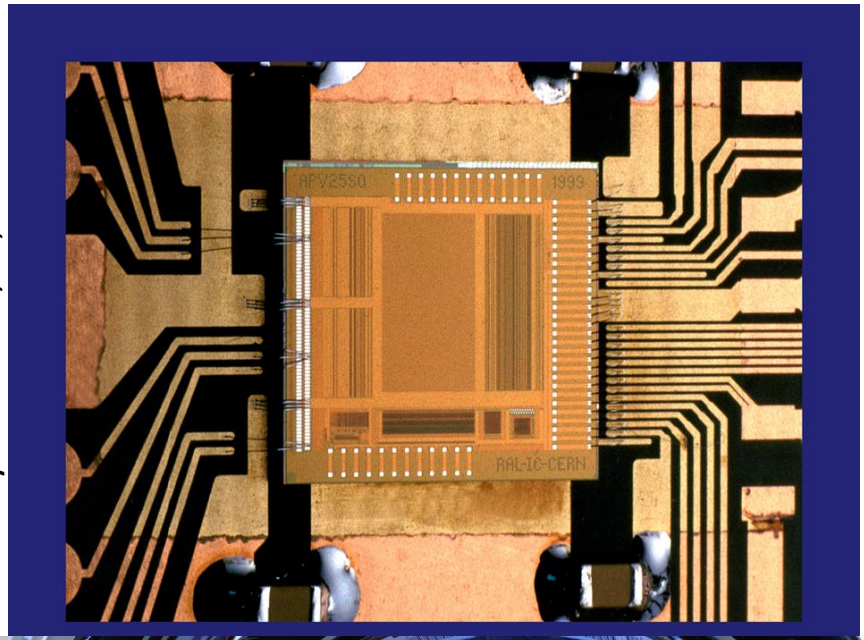
- Bipolar tech
- 595 mW, one channel

Custom

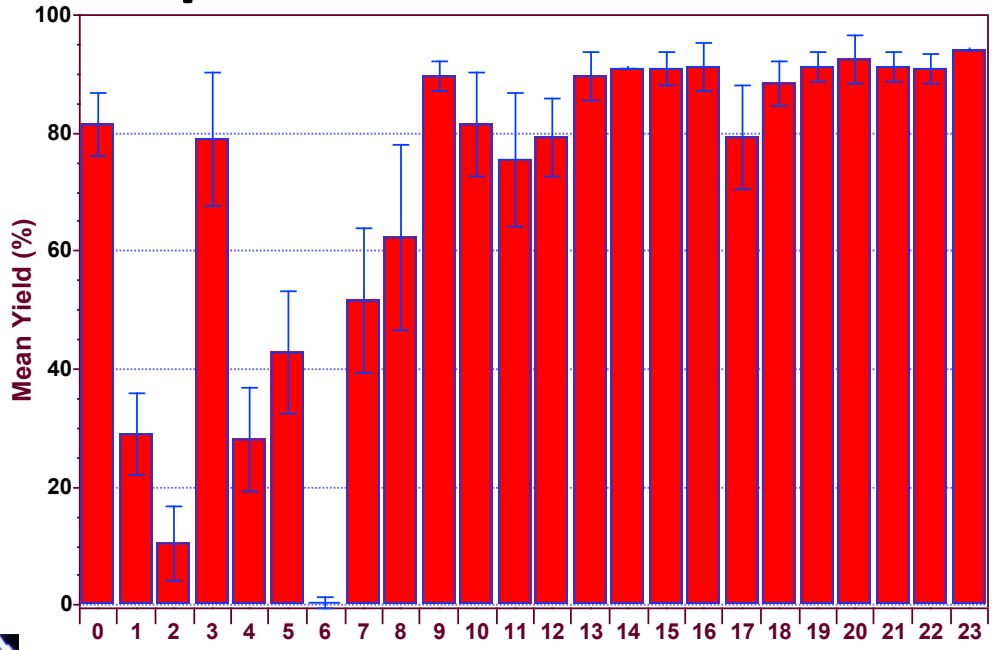


- CMOS
- 120 mW / channel
- No need for input and output adapters

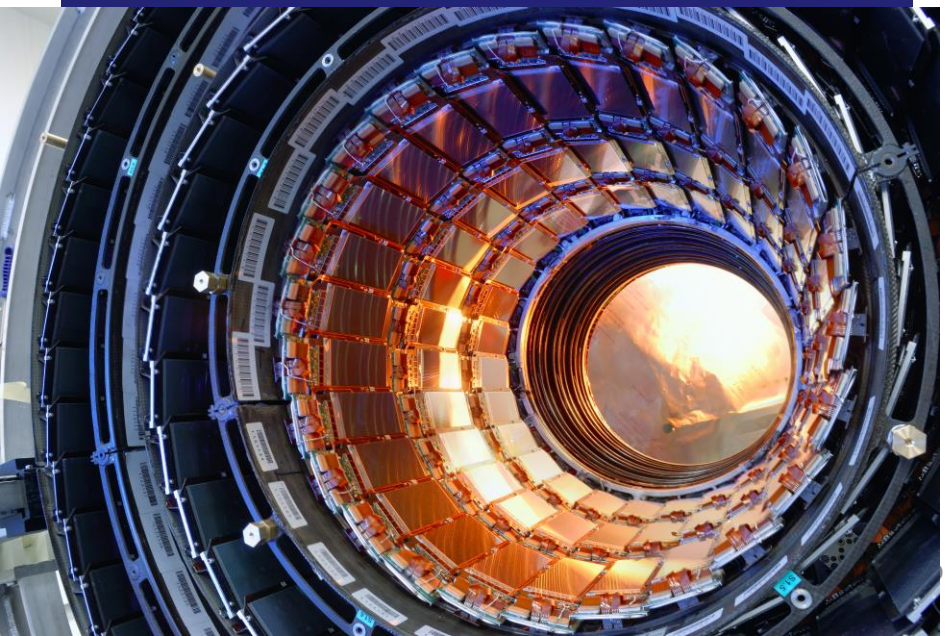
Tracker FE chips: APV



Courtesy of G. Hall, IC, UK



Technology “infancy” problems.

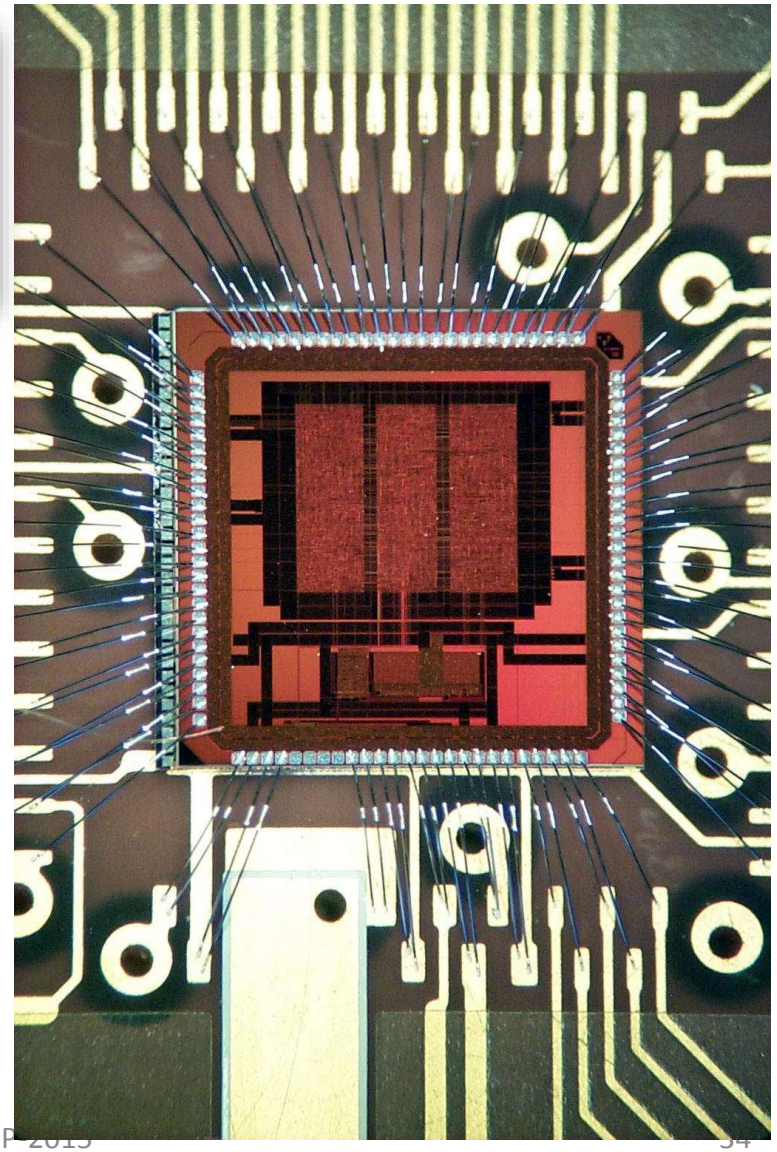


High Speed Links: The GOL {$}

A 1.25Gbit/s Serializer for LHC Data and Trigger Optical Links

P. Moreira[1], J. Christiansen, A. Marchioro,
E. van der Bij, K. Kloukinas, M. Campbell and G. Cervelli

CERN-EP/MIC, Geneva Switzerland

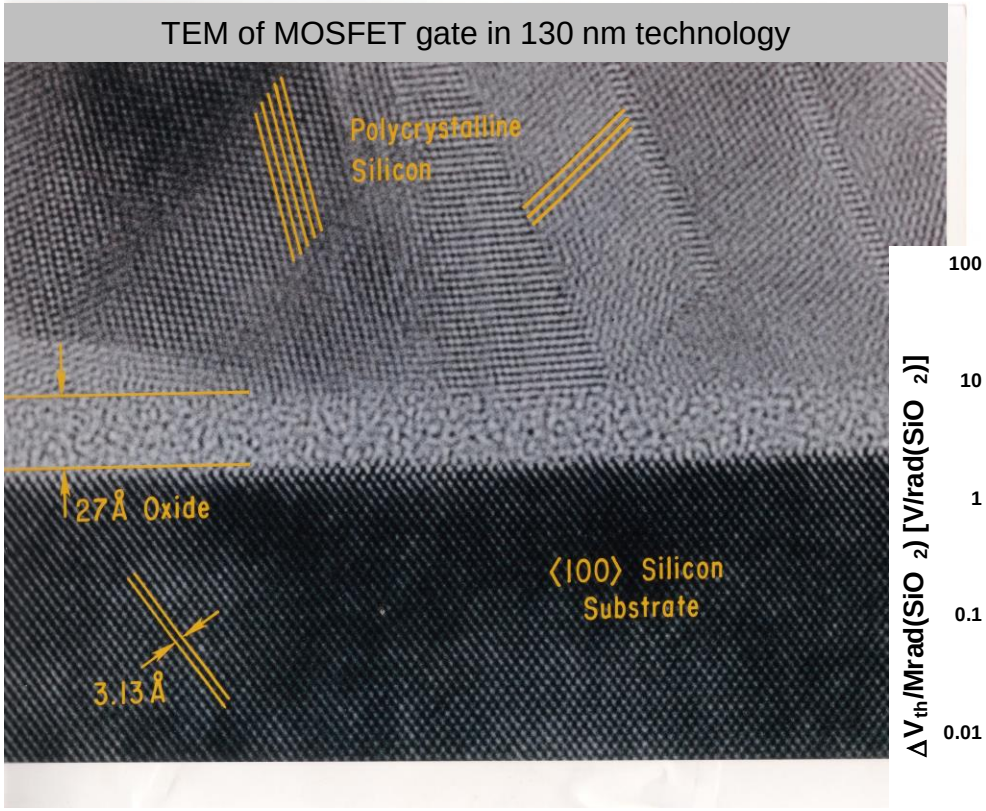


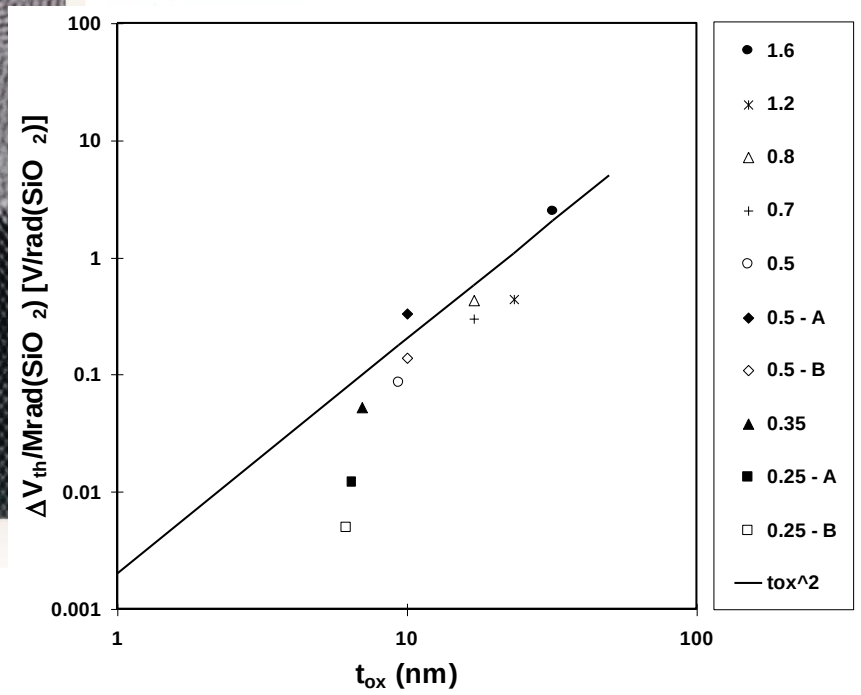
High density, low power CMOS allowed not only to implement a high speed serializer in a chip, but actually three to combat SEU effects

{$} Paper presented at LEB 1999

Radiation Hardness of DSM

TEM of MOSFET gate in 130 nm technology





N.S. Saks et al., IEEE TNS, Dec. 1984 and Dec. 1986

The future

MICROELECTRONICS IN HEP 2.0

3 Questions to draw a roadmap

1. Can functionality be improved (invented?) with new technologies in more integrated chips?

2. Can we substantially reduce the $/channel figure with more advanced chips?

3. Can sub 65nm CMOS take us to the GRad regime?

Can functionality be improved (invented?) with more integrated chips?

QUESTION 1

SRAM Density Comparison

Node	SRAM Cell Area [um2] {$}	KBits/mm2	Relative Density Gain
130nm	1.2	814	1.0
65nm	0.55	1776	2.2
28nm [bulk]	.1	~10K	12
14nm [Finfet]	0.05	~20K	25

{$} From various published sources

FE memory with FinFET

TSMC Finfet Based SRAM @ IEDM 2014

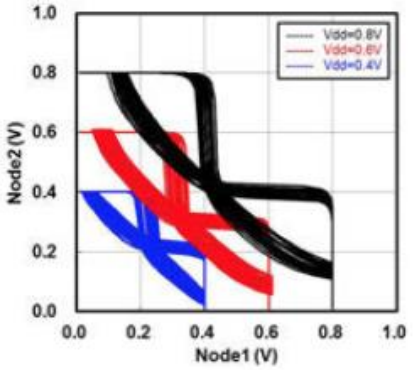


Fig.9 SNM of 0.07um^2 HD SRAM cell is illustrated down to 0.4V.

Cell size: 0.07 um2

Min Operating Voltage: 0.45V

Access time @1V is 0.6ns

Used in FE

Size of a 128Kbit buffer:

$128\ 10^3 * 0.07\ um^2 = 8.9\ 10^3\ um^2$

=> 94x94 um

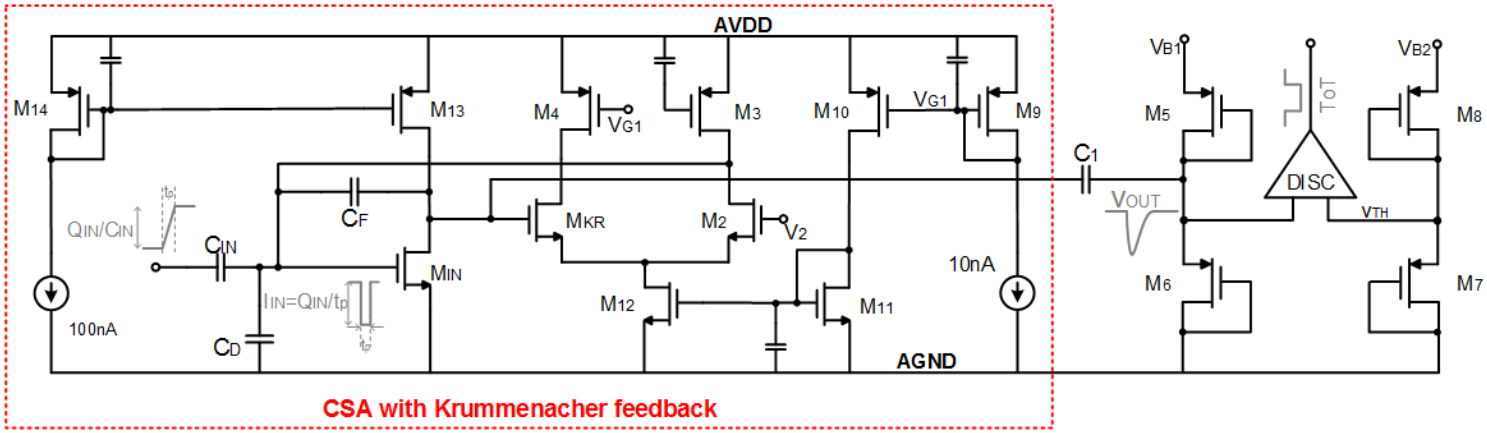
Operation @ 0.5V => ¼ of the power

from Shien-Yang Wu et al: An Enhanced 16nm CMOS Technology Featuring 2nd Generation FinFET Transistors and Advanced Cu/low-k Interconnect for Low Power and High Performance Applications, IEDM 2014

Advanced pixels: 28nm

IC-PIX28: a 28nm read-out channel for pixel detector
F. Resta, G. Rota, A. Pezzotta, A. Pipino, A. Baschirotto
Physics Department University of Milano-Bicocca, Italy

To be presented at ICECS2015

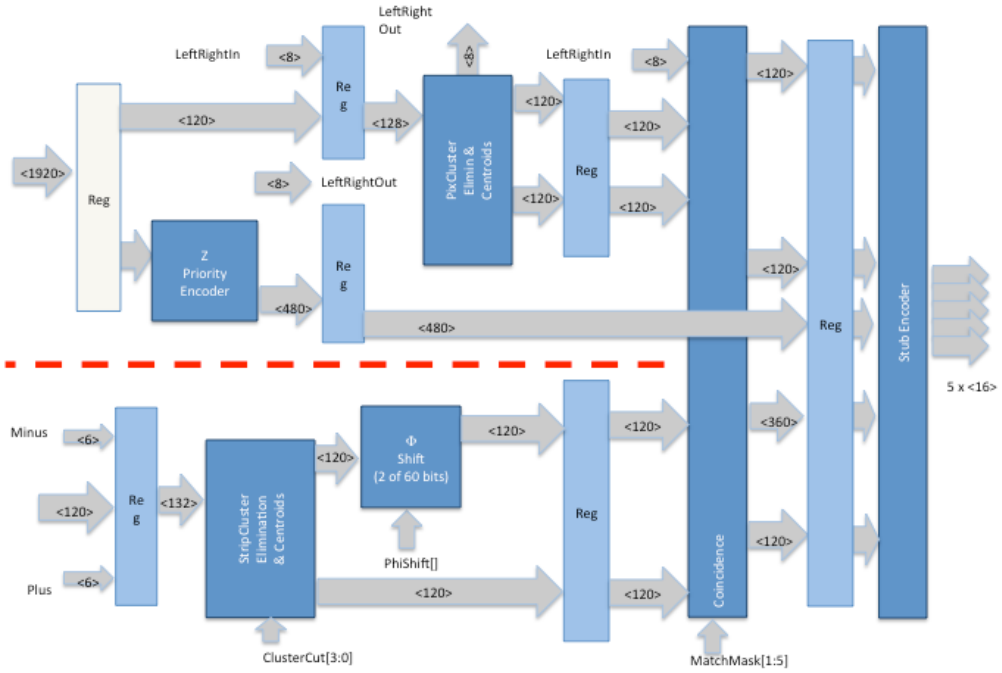


Parameter	Value
Tech	Hi-K metal Gate
Power	4.2 uW
Input signal	< 30 ke$^-$
Detector capacitance	100 fF
Min detectable signal	1 ke$^-$
Peaking time	11 ns
Noise level	200 e$^-$

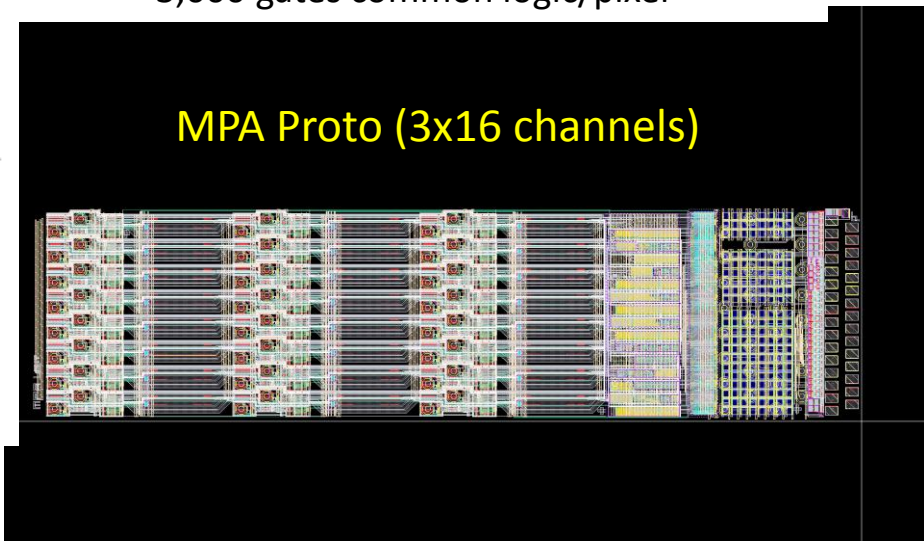
Courtesy of A. Baschirotto, Università Bicocca MI, IT

High complexity FE: the MPA

- Functionality
  - two layers sensor to find promptly “stiff” tracks through prompt combinations of hits in FE chips



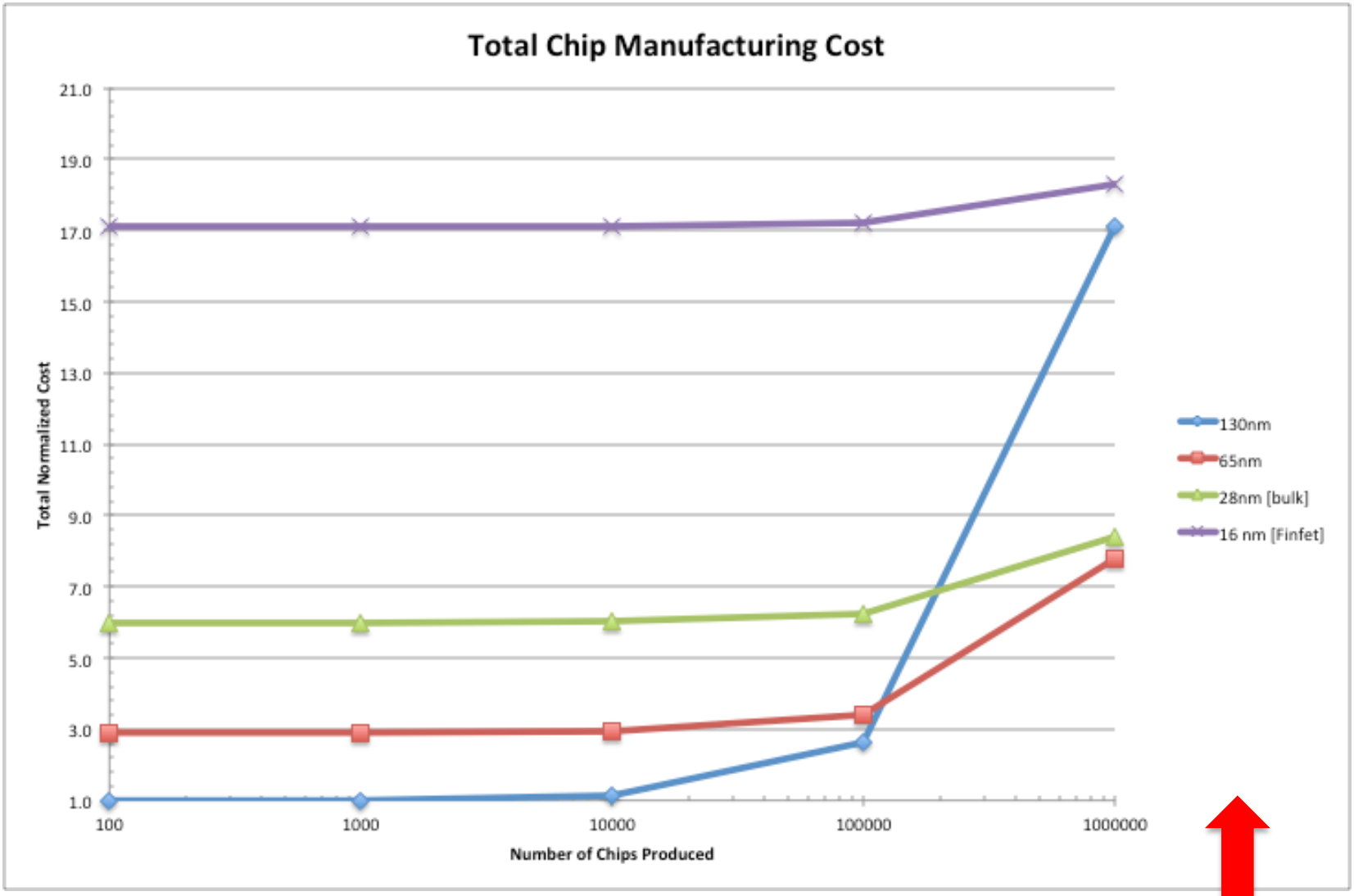
- One macro pixel (1500x100 um) contains:
  - normal analog FE for amp/shaping/discriminating
  - clustering logic
  - re-alignment logic
  - pixel-strip trigger logic
  - storage for L1 2,000 logic gates + 512 bit SRAM/pixel
  - 3,000 gates common logic/pixel



For details see talk 57 by D. Ceresa on Wednesday

Can we reduce substantially the $/channel figure with more advanced chips?

QUESTION 2



A 500m^2 calorimeter
"could" have 5 10^6 chips

Cost reduction hints

- Do not reinvent the hot water over and over
  - Use qualified IPs
    - Reward those in the community that make them
    - Buy from industry (it is cheaper!)
- Complexity is in the systems
  - Design your system top-down, not the other way around
- Strengthen design groups
  - More training and education
    - Today's tools are much more capable and still largely underused
    - Look at what others are doing!
  - Create the conditions to retain and motivate experienced designers
- Create a reward mechanism for good engineering (and not just "academic inventing")

Can sub 65nm CMOS take us to the GRad regime?

QUESTION 3

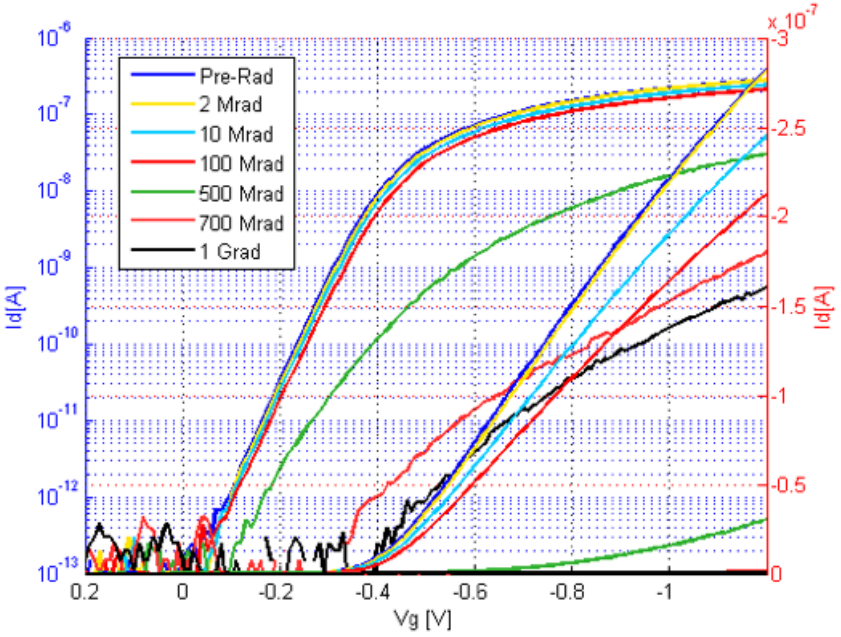
TID @ 1 GRad

- Thin gate oxides and enclosed transistor have solved the problems of charge trapping in gate oxides and in shallow trench borders.
- Complex problems remain with:
  - Trapping in sidewalls, spacers, shallow tranches
  - Transport mechanism of traps in different materials
  - Interfaces Si-SiXX
  - Holes mobility degradation
  - Non SiO_2 materials
  - Difficulty in accessing detailed process information from “huge” foundries

Can 65nm survive 1 GRad

- Issue is much more complex than RH of ¼ um in 1996
- Discordant effects related to:
  - N/P
  - Total dose
  - Dose rate
  - Size of devices
  - Temperature
  - Biasing conditions
  - Interplay of items above
- RH > Grad is unlikely to be relevant outside HEP
- R&D Investment (manpower) required >> than what was done previously.

- See talk of Federico @ MUG



65nm PMOS
W=120nm, L=1um
T = 25C
|Vgs|=|Vds|=1.2V

Conclusions

- Innovation is not constrained by availability of technologies!
- Their higher complexities require much stronger collaboration and coordination between players in our small community.
  - Only workable model:
    - Ride commercial mainstream technologies
    - Single supplier
    - Common qualified library of high level, well constructed, truly portable IPs
    - Strictly controlled and documented design flow
- Design costs are rising (but not cost/function !), but possibilities are unbounded.
- Perhaps TID robustness > 1 Grad is “beyond physics”, therefore we might want to consider making “disposable modular detectors”.
  - Already done in some detectors: can wee extend the idea?

THANK YOU