

High-Performance Analog-to-Digital Converters: Evolution and Trends

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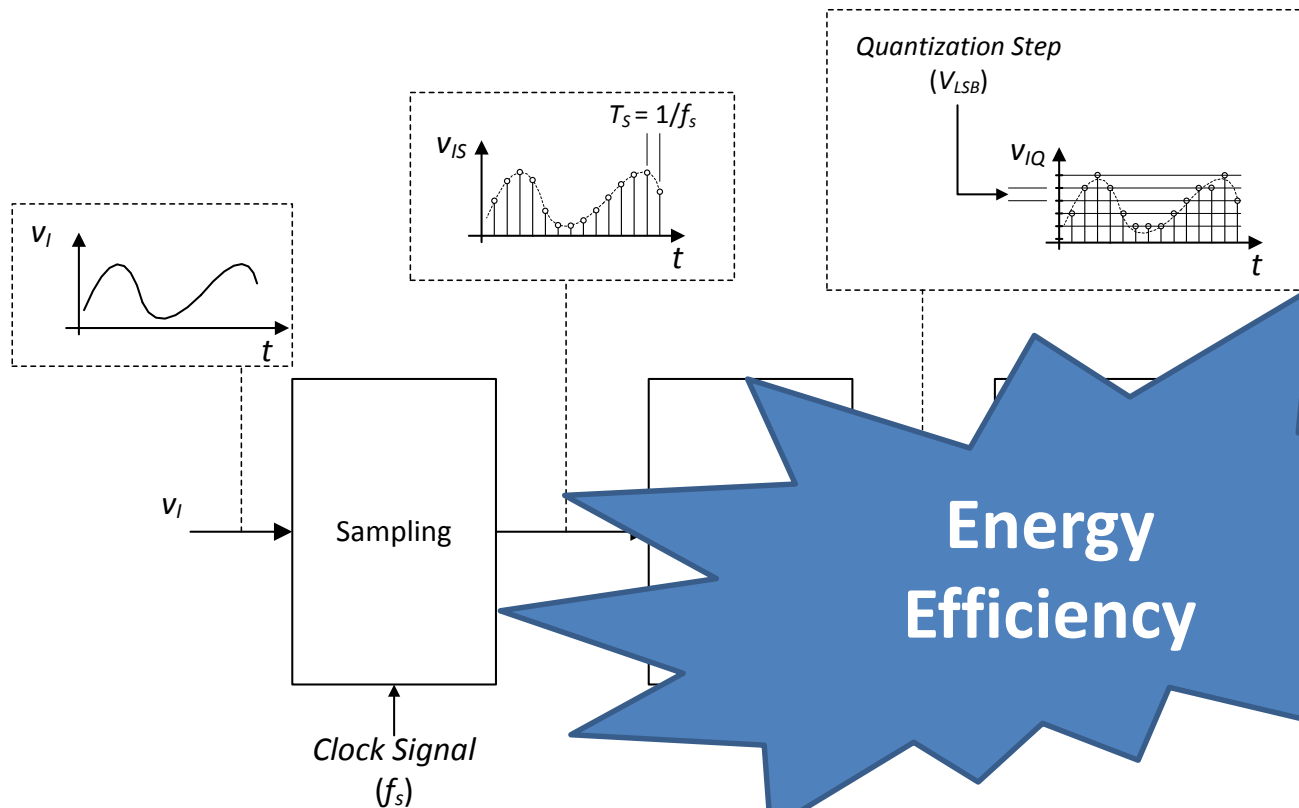
28th September 2015

Outline

- ADC performance: Evolution
- ADC architectures: Relationships, Speed, Performance
- Technology Scaling: Difficulties and Opportunities
- Synopsys digitally calibrated Pipeline and SAR ADCs

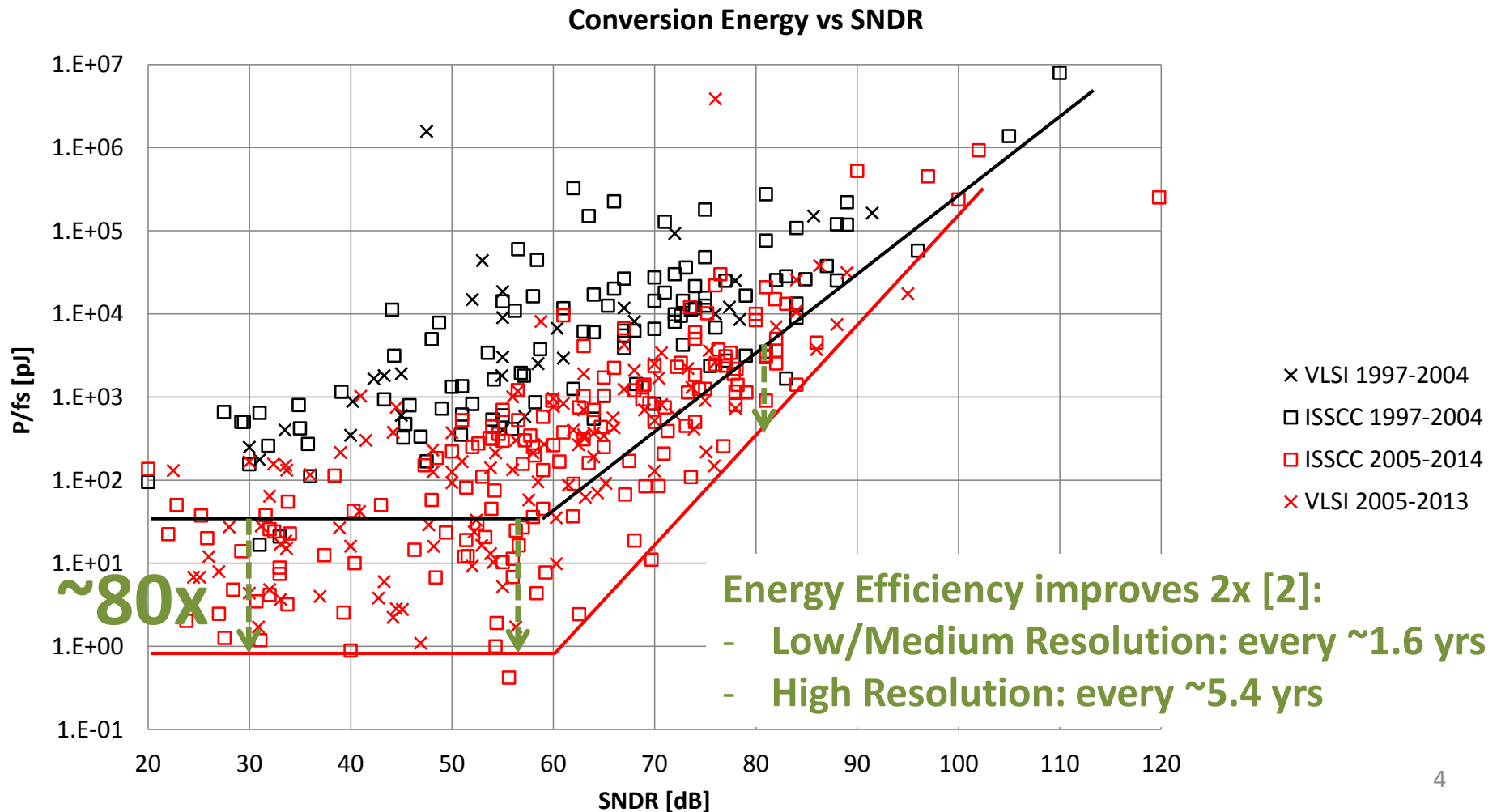
The Analog-to-Digital Converter

- Translates an **analog input signal** into its **binary coded representation (N bit)**, at a certain **rate (f_s)**



Evolution of ADC performance

- Data from Prof. Murmann's Survey [1]



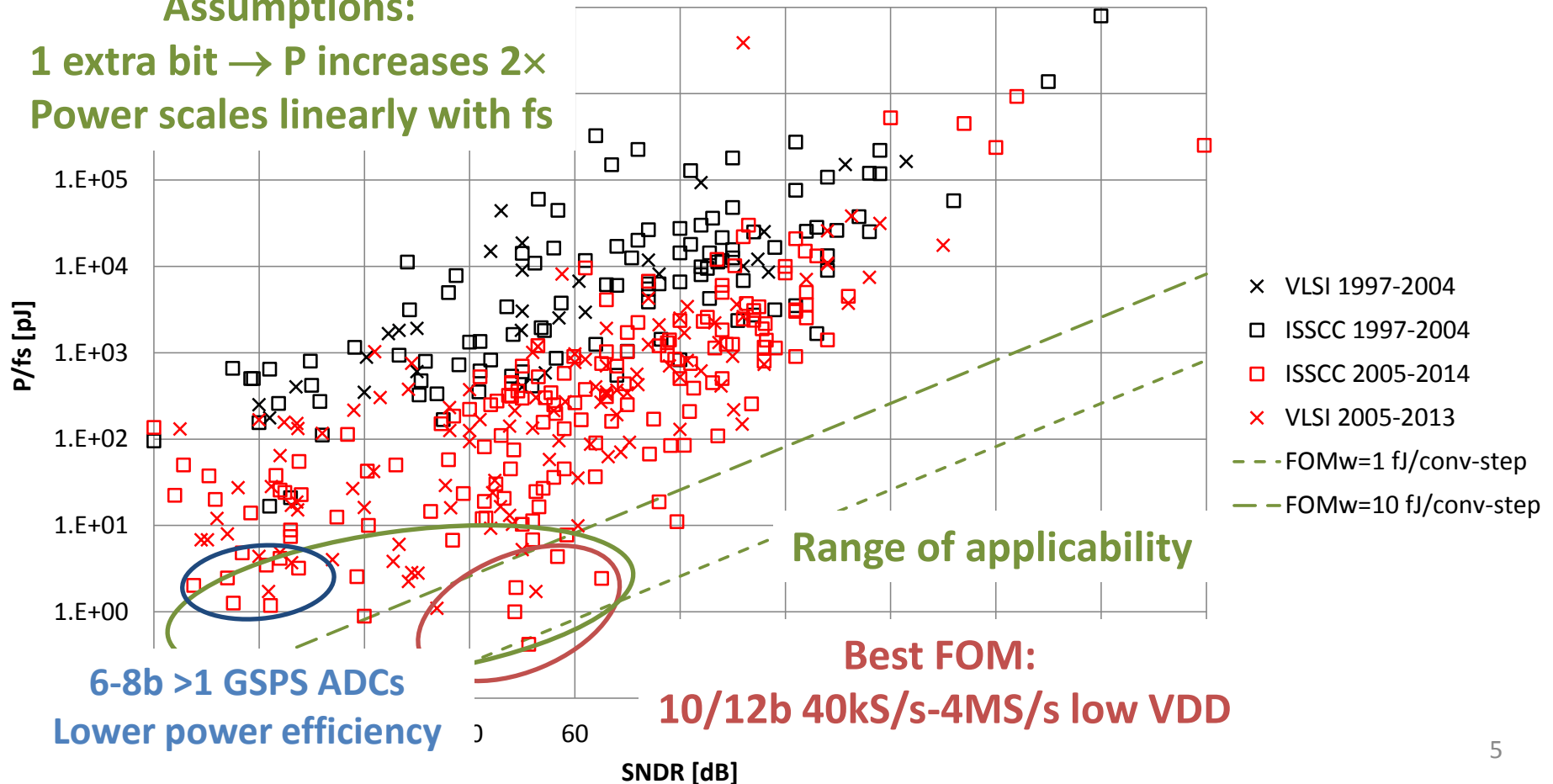
Evolution of ADC performance

- Walden's FOM = $P / (2^{\text{ENOB}} \cdot f_s)$

Assumptions:

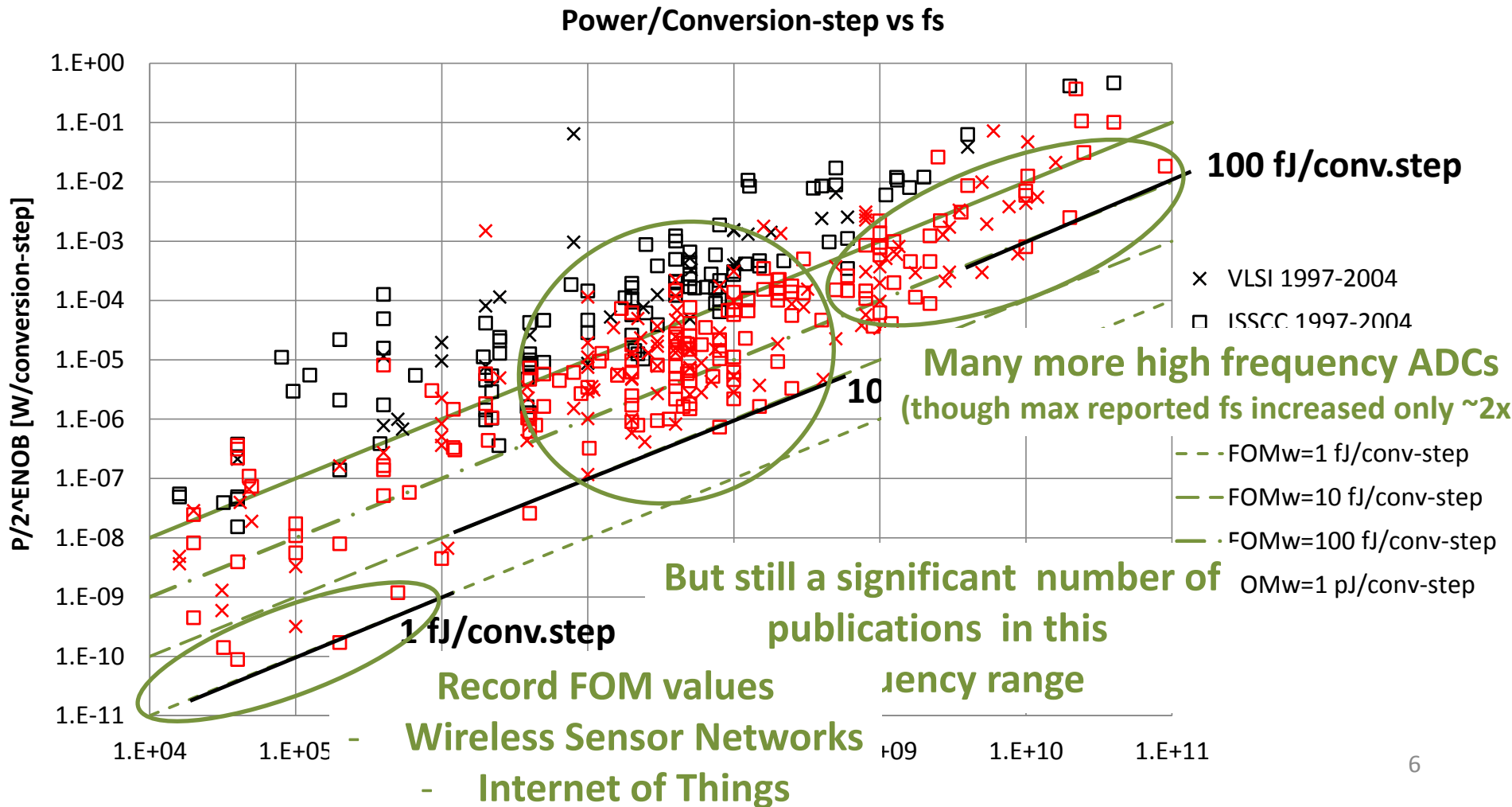
- 1 extra bit \rightarrow P increases 2 \times
- Power scales linearly with f_s

Conversion Energy vs SNDR



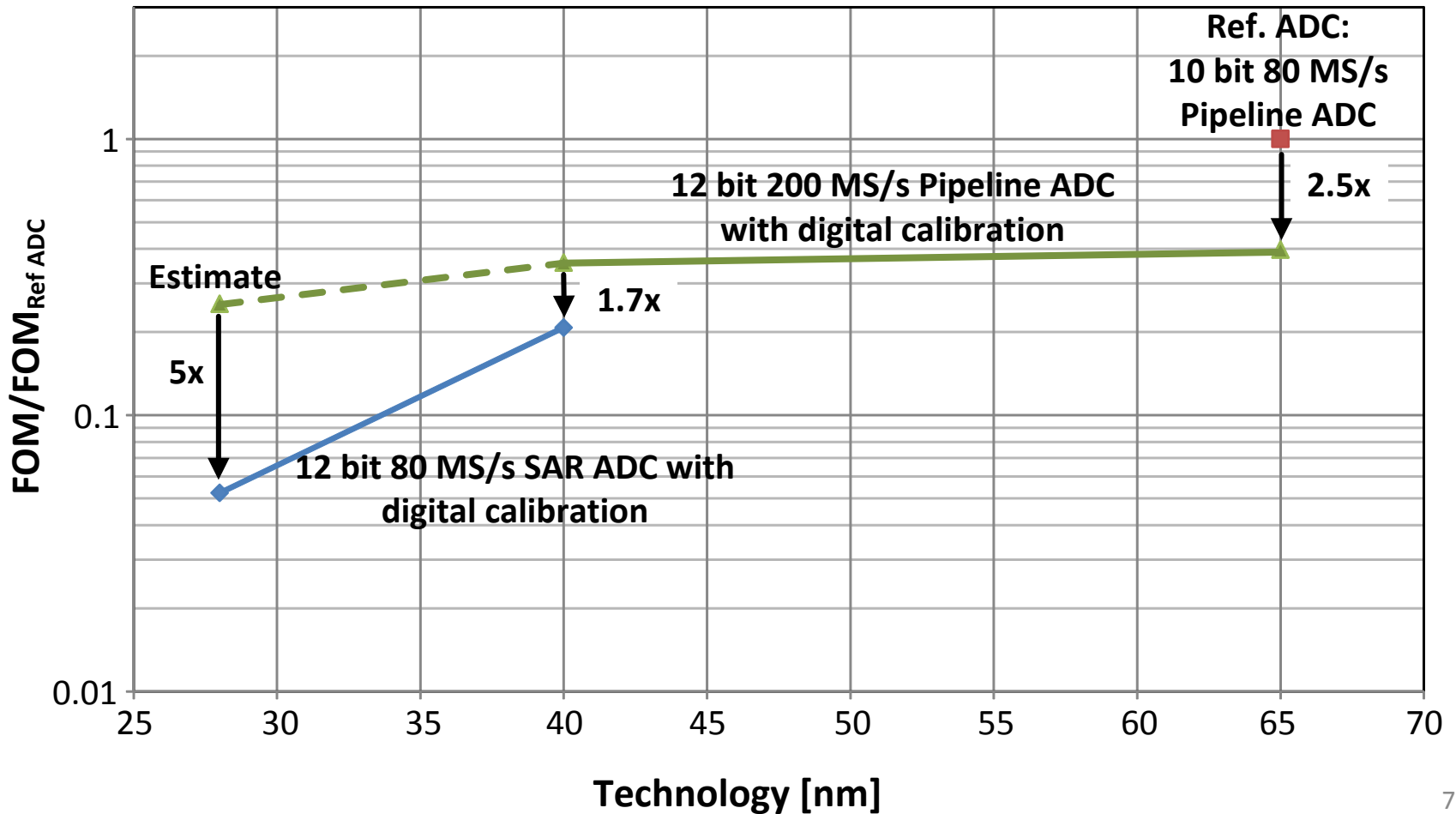
Evolution of ADC performance

- Power per conversion-step as a function of f_s



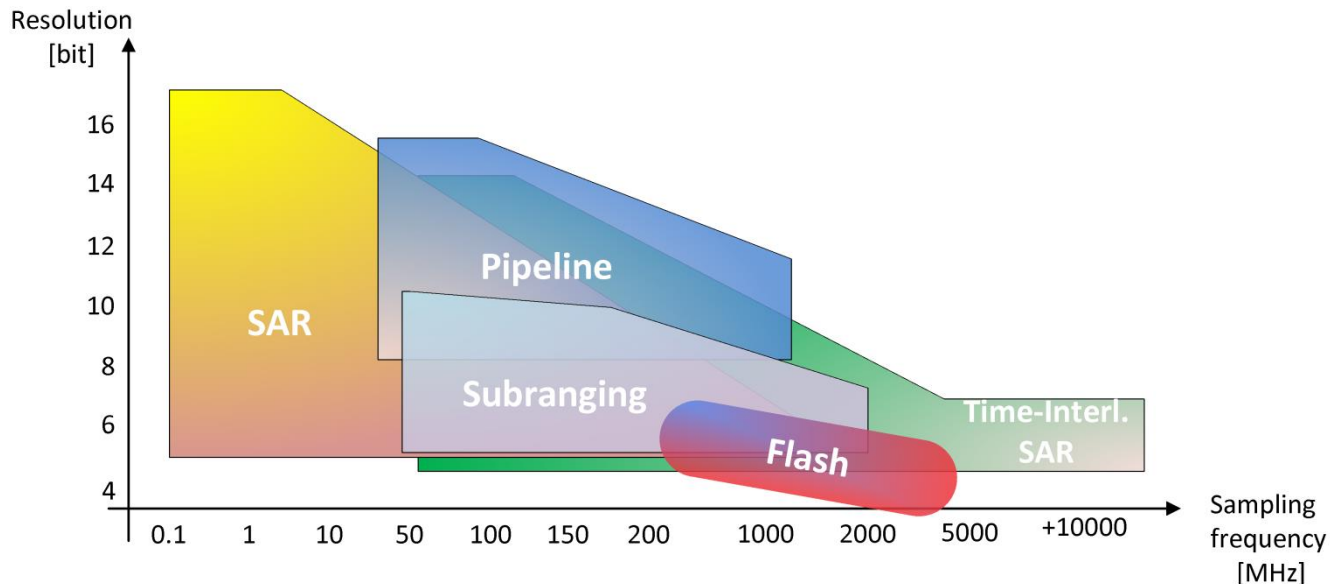
Evolution of ADC performance

- Some of Synopsys ADC implementations



ADC architectures

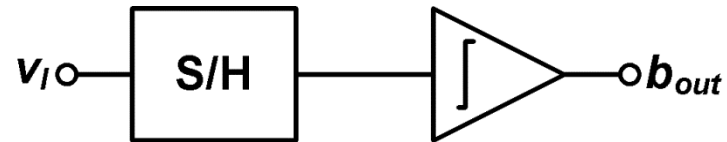
- ADC architectures typically presented as different and (somewhat) unrelated alternative solutions...
 - ... each with its own pros and cons ...
 - ... each best suited to certain resolution and f_s
- Here we will focus on **fundamental operations** and how they are **related** [3]



Single and Multi-bit ADCs

- ADC fundamental operations: **sampling** and **quantization**

- Single bit ADC:

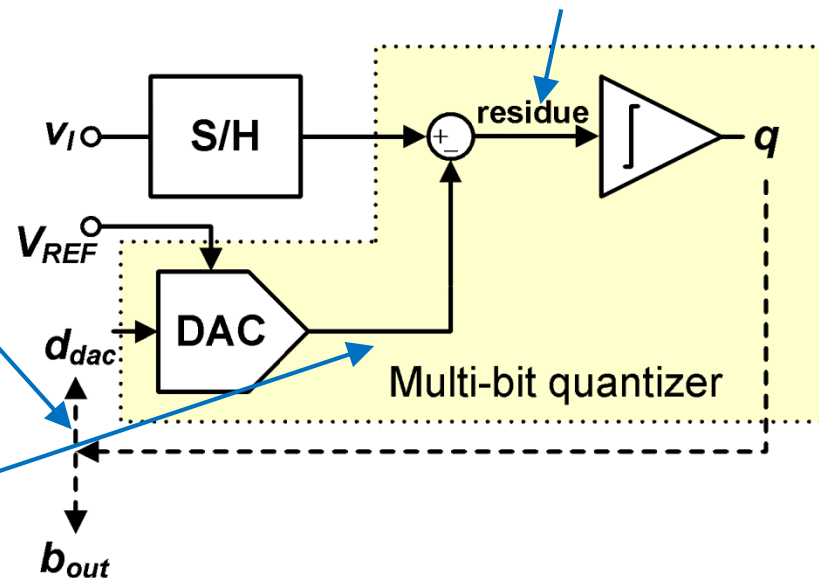


... i.e. minimize the residue ...

- Multi-bit ADC:

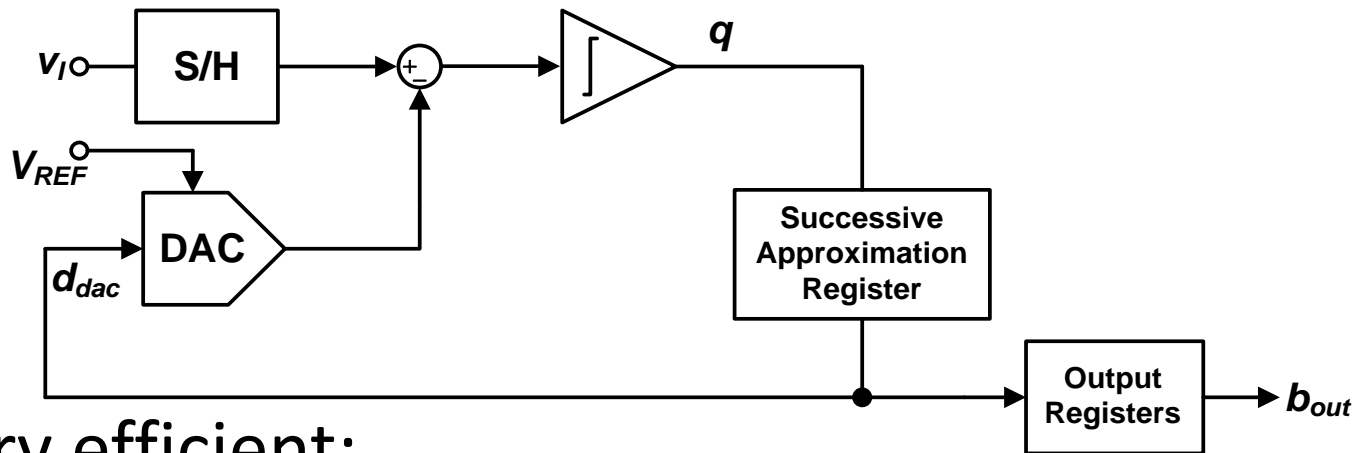
... and then use $b_{out} = d_{dac}$

Conversion Process:
Search the DAC output that
best approaches the
sampled input...



SAR ADC

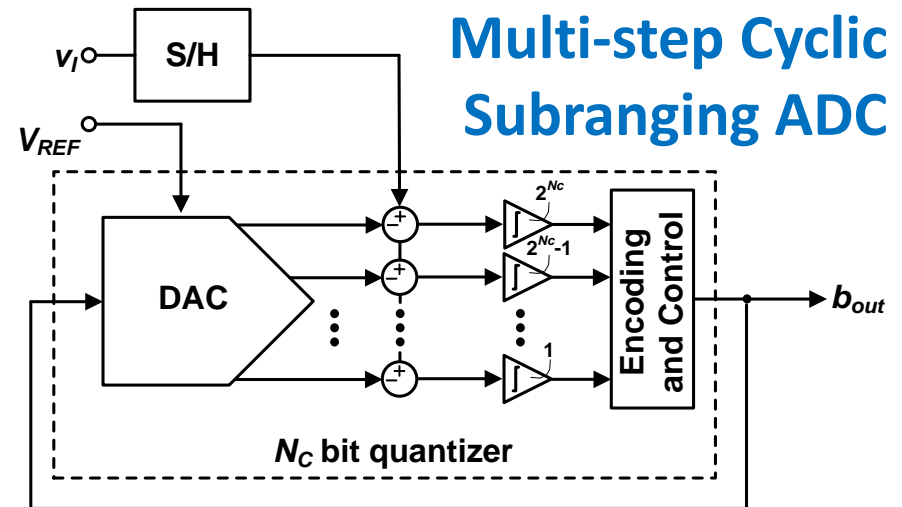
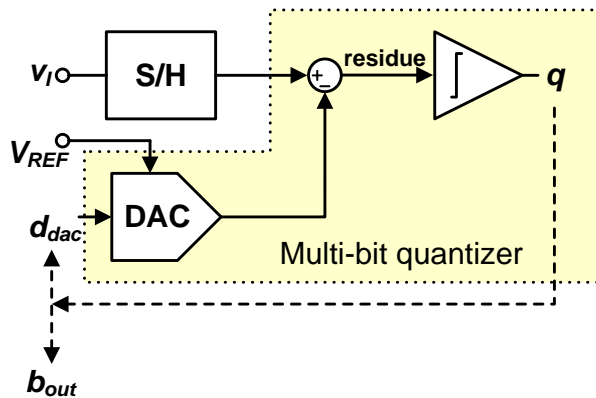
- **SAR ADC** is the direct implementation of the elementary multi-bit architecture



- **Very efficient:**
 - Re-uses same hardware in each cycle
 - Necessary number of cycles grows linearly with resolution: N cycles for N bits
 - **Performance limited by DAC nonlinearity**

Speed Increase: Parallelization in the code-search process

- If DAC provides several outputs simultaneously: possible to search several codes in parallel

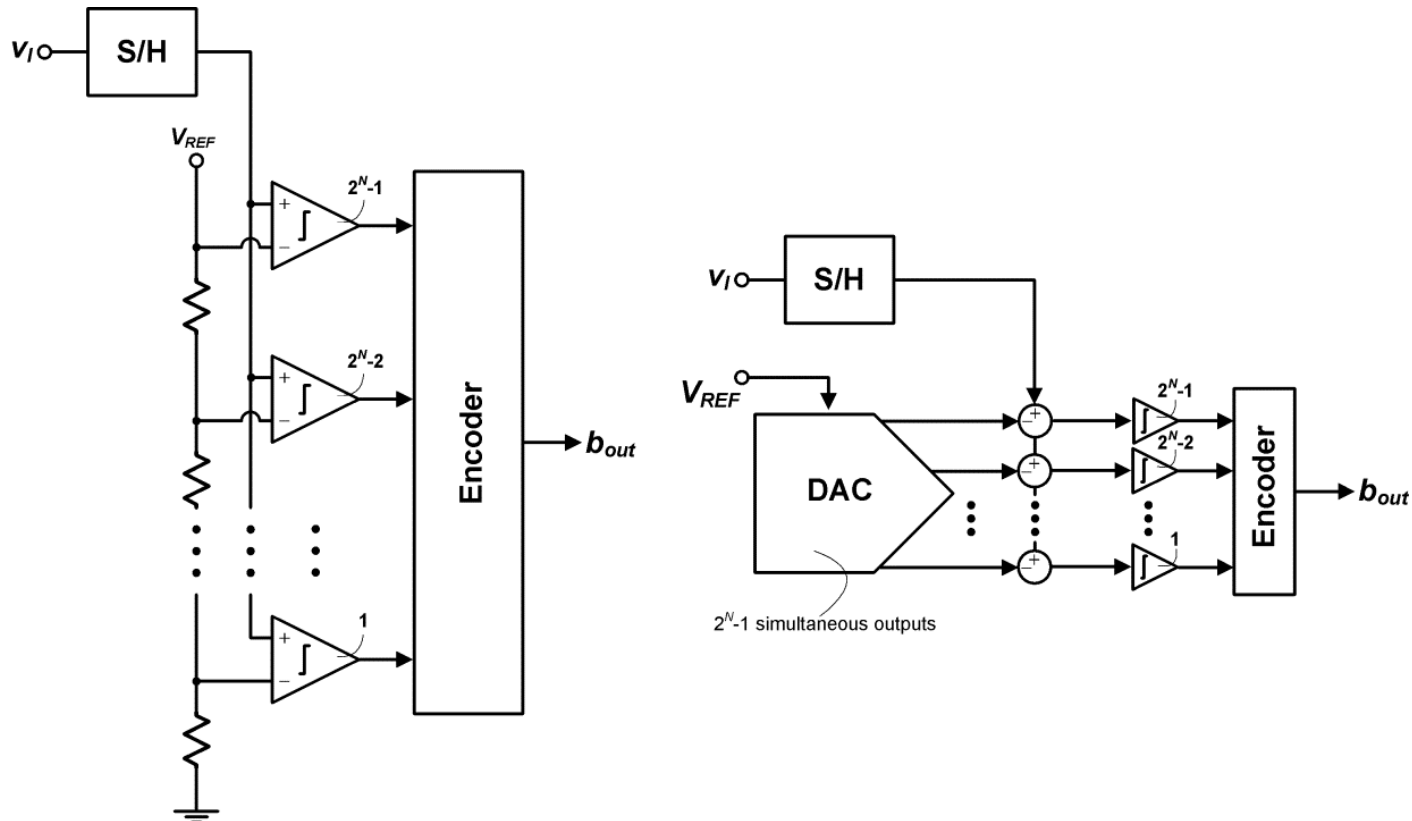


- Different codes are searched by different paths
- **Faster:** N/N_C cycles to complete a conversion
- **Number of parallel paths: 2^{N_C}**
- **Differences between them degrade performance**
- Examples: 2 and 3 bit per cycle SAR ADCs [4,5]

Speed Increase: Parallelization in the code-search process

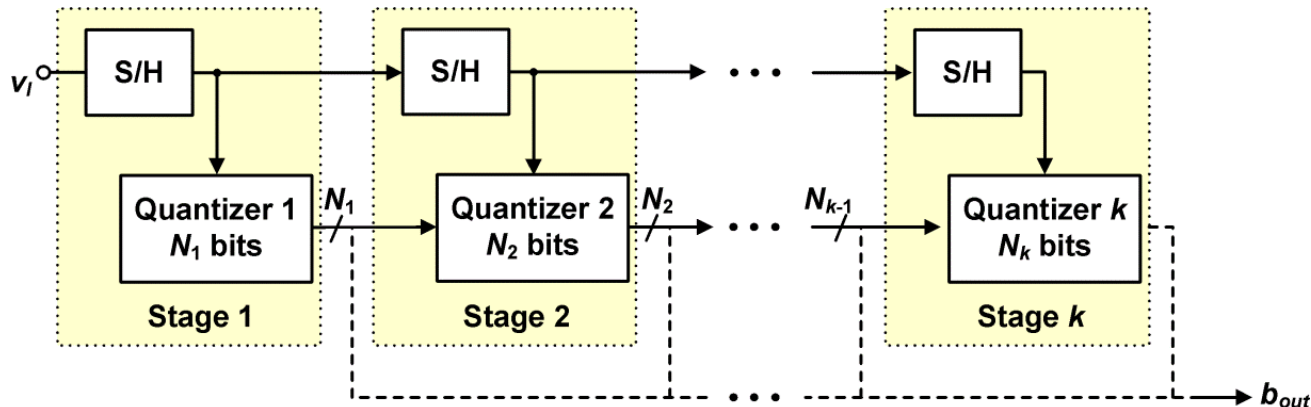
- Taking this parallelization to the limit: $N_C=N$
- All codes are searched simultaneously

Flash ADC



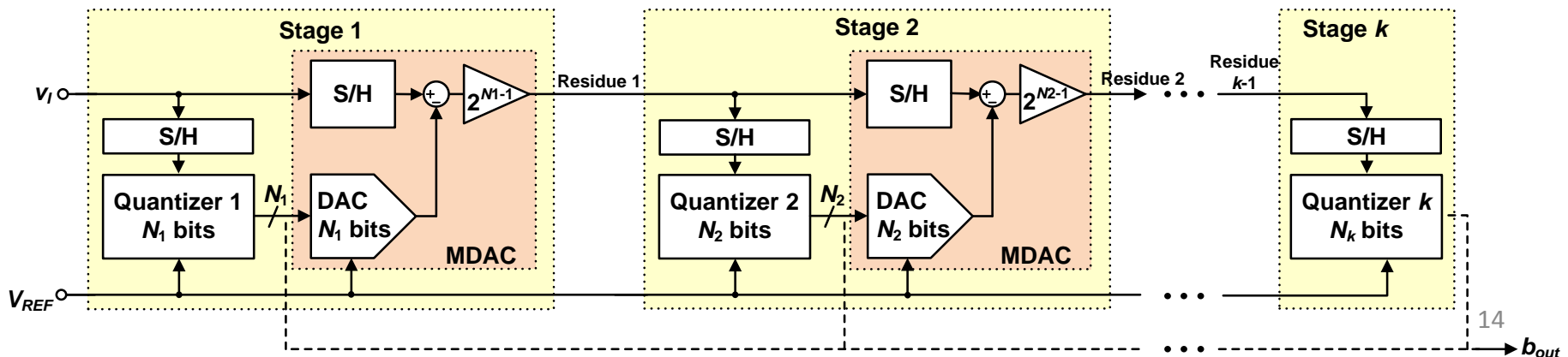
Speed Increase: Pipelining

- Another possibility is **pipelining**:
 - Quantization process is divided in several steps that occur in a pipelined fashion:
 - Typically, quantizers have low resolution → low parallelization in the code search process
 - At a given clock cycle, the ADC is quantizing several different samples



Speed Increase: Pipelining

- **Pipelined ADCs:** Practical considerations lead to the structure shown below.
- Each stage constituted by:
 - Quantizer
 - Residue calculator/amplifier block – MDAC
 - Residue: error signal corresponding to what is left to quantize



Speed Increase: **Pipelining**

- Quantizer specifications are relaxed (low resolution)
- MDAC non-idealities limit performance
 - Gain error of S/H, DAC and residue amplifier limit overall linearity
 - In practice this translates into stringent **gain** specifications of the amplifier implementing the MDAC

Speed Increase Technique \Leftrightarrow Limitations

- **Non-linearity of the DAC(s) limits performance**
- **Additionally:**
 - Use of **Pipelining** \rightarrow Residue Amplification \rightarrow Relaxed Quantizers



Performance limited by amplification blocks

- Use of **Parallelization in the code search process** \rightarrow Quantizer only ADCs \rightarrow Many parallel paths



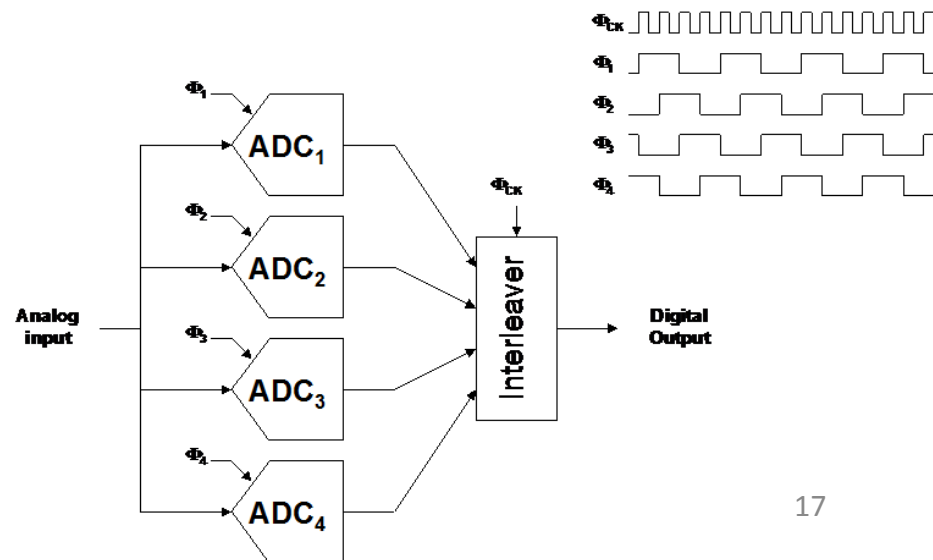
Performance limited by differences between parallel paths (offsets)

- SAR ADCs use none of the above: **limited only by DAC non-linearity**

Parallelization: in time domain

- Another **parallelization** possibility is **time-interleaving**
- Different samples processed by independent paths
 - Differences of **offset**, **gain**, **sampling instants** degrade performance
- Unit ADCs use the parallelization/pipelining techniques previously discussed
- N_{ch} ADCs \rightarrow fs increases N_{ch} times

Example: 6b 90GS/s ADC with 64 unit SAR ADCs [6]



ADC implementations in advanced technologies

- Technology Scaling – **the bad**
 - Reduction of g_m/g_{ds}
 - Headroom limitations caused by VDD reduction
 - Bad CMOS switches
 - Higher variability
 - Transistor properties and matching more and more dependent on surroundings
 - Higher interconnect delays

- ... and **the good**

- Faster devices
- Digital processing is in power - available to over sub-blocks of ADCs

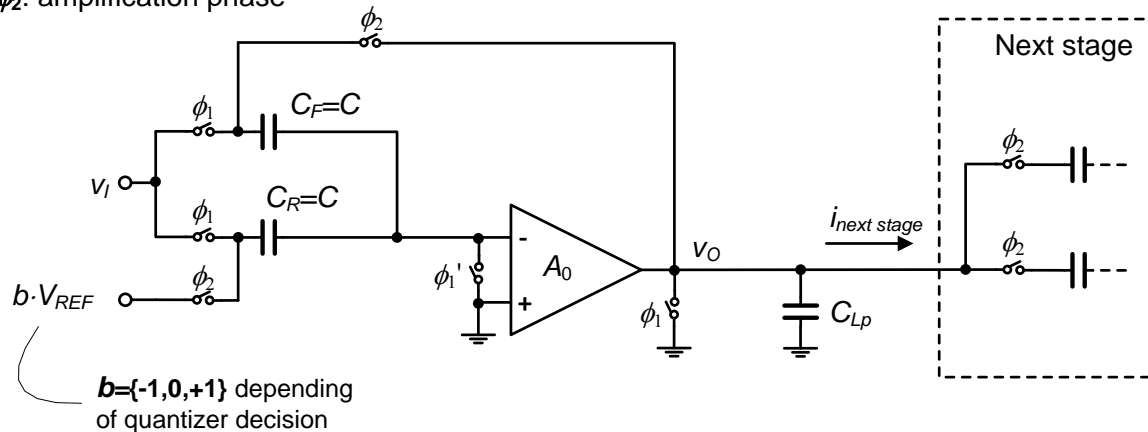


ADCs with residue calculation/amplification

■ Typical 1.5b MDAC circuit

- ϕ_1 : Sampling ϕ_2 : Residue Amplification

ϕ_1 : sampling phase
 ϕ_2 : amplification phase



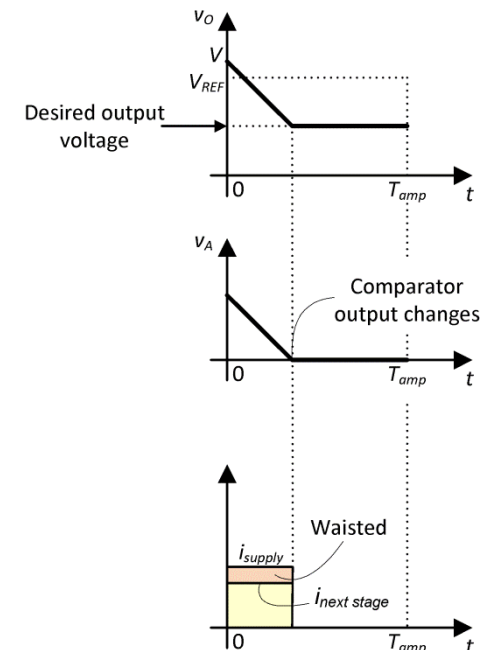
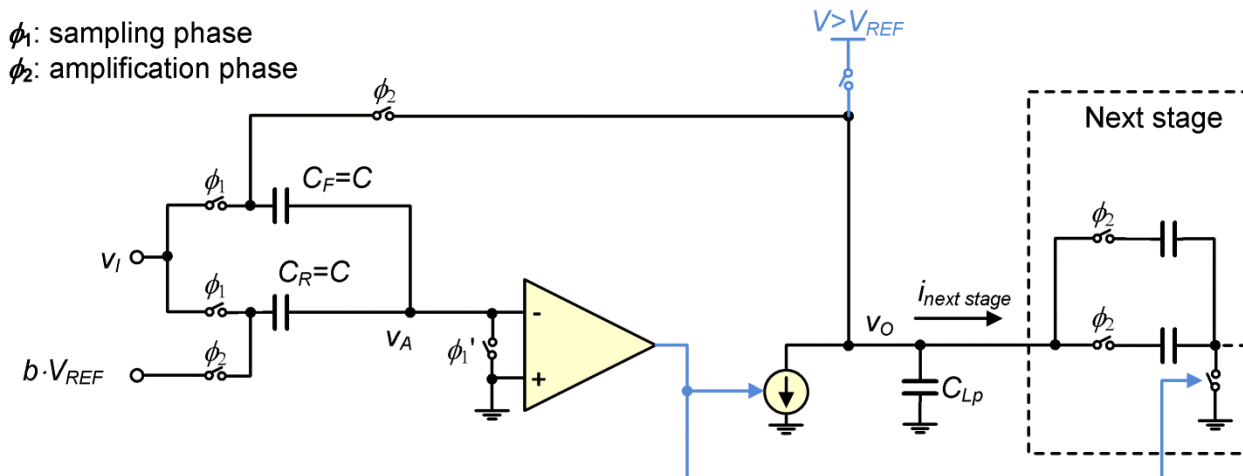
- Negative feedback around a high-gain amplifier sets residue amplification gain very accurately
- Increasingly difficult to attain high gain in nanoscale technologies
- Class A amplifiers not power efficient

ADCs with residue calculation/amplification

- Techniques to improve power efficiency:
 - **Opamp switching** reduces power consumption during reset phase, but introduces speed or headroom limitations [7-9]
 - **Opamps** can be **shared** between stages in order to ensure they are being used at all times [10-13]
 - **Class AB amplifiers** [14] may be used, but are more complex and have limited effectiveness

ADCs with residue calculation/amplification

- Techniques to improve power efficiency:
 - Use of **low gain amplifiers** and **digital calibration**
 - Opamp substituted by **comparator + current source** [15,16].
 - No stability and gain-bandwidth product limitations
 - Stops consuming when the desired voltage is reached

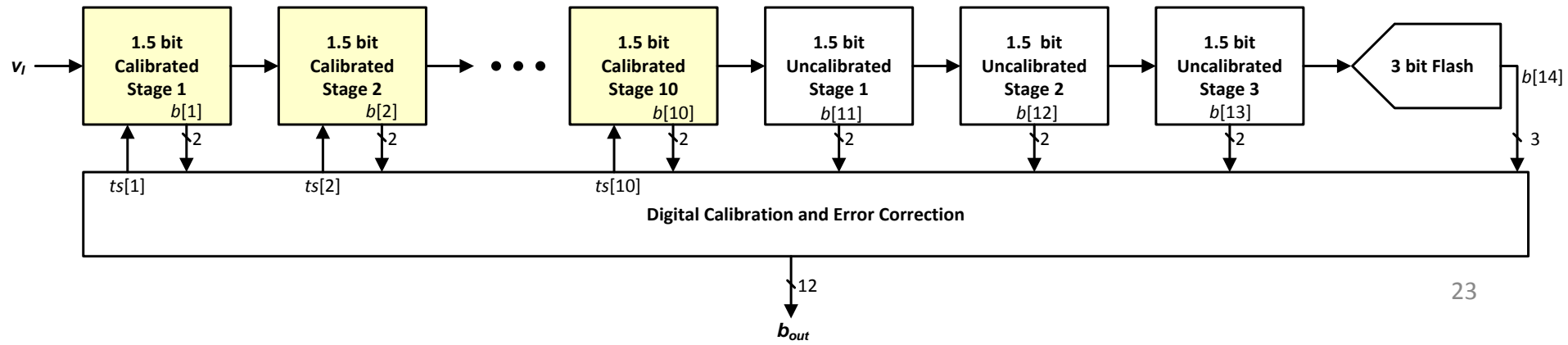


ADCs with residue calculation/amplification

- Techniques to improve power efficiency:
 - **Open loop amplifiers based on transconductances** [17,18]:
 - Gain is parasitic and PVT dependent, and non-linearity is non-negligible. Complex digital calibration required
 - **Open loop amplifiers that are not based on transconductances:**
 - Parametric amplification [19,20]
 - Bucket brigade circuits [21,22]
 - Even larger non-linearity and dependence of parasitics/PVT
 - Digital calibration complexity is further increased

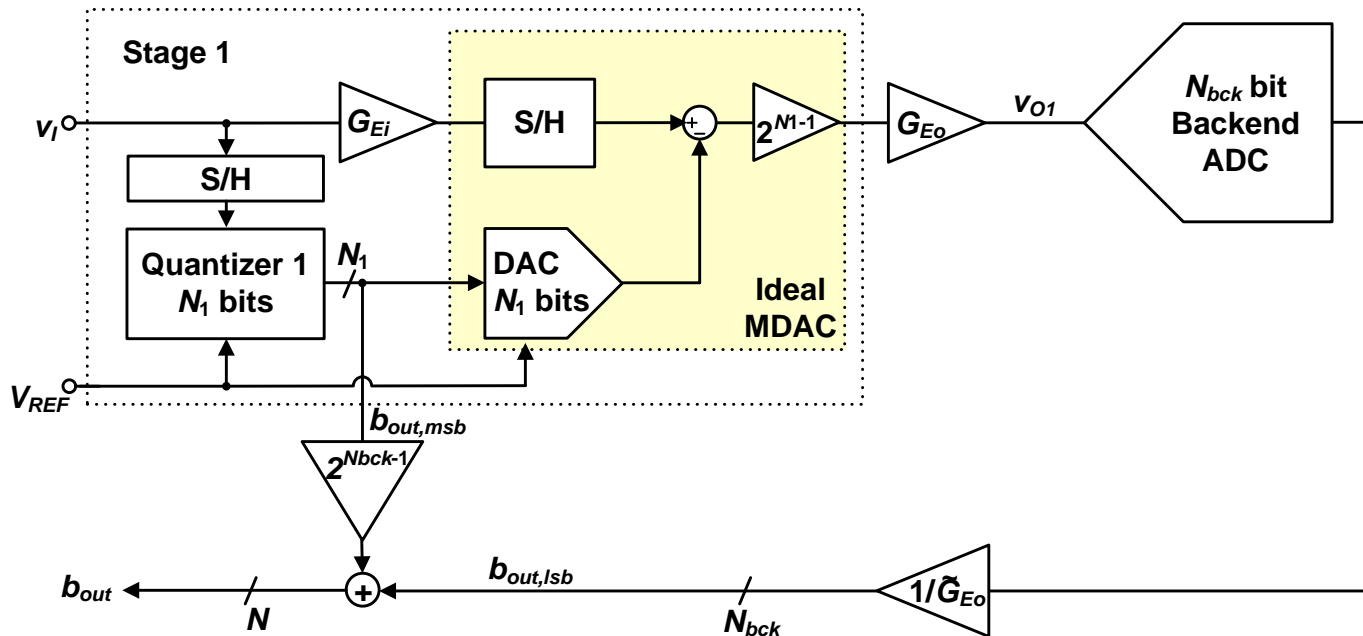
12b 200MS/s digitally calibrated pipeline ADC

- Calibration of amplifier finite gain and capacitor mismatches
 - Fast startup time and robustness against VDD/Temp variations
- Stages with reduced output swing
- Opamp switching technique with no speed or signal swing limitations



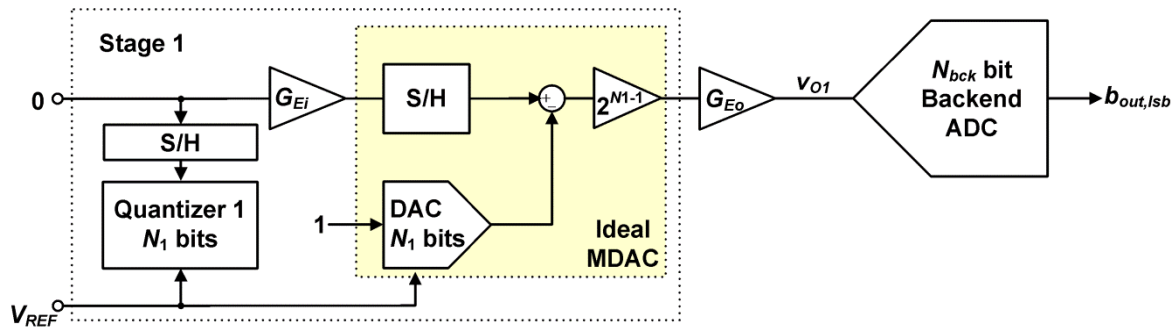
12b 200MS/s digitally calibrated pipeline ADC

- Gain error of S/H, and residue amplifier, and mismatches of the DAC cause G_{Ei} and $G_{Eo} \neq 1$
- Digital gain calibration:** Multiply by $1/G_{Eo}$

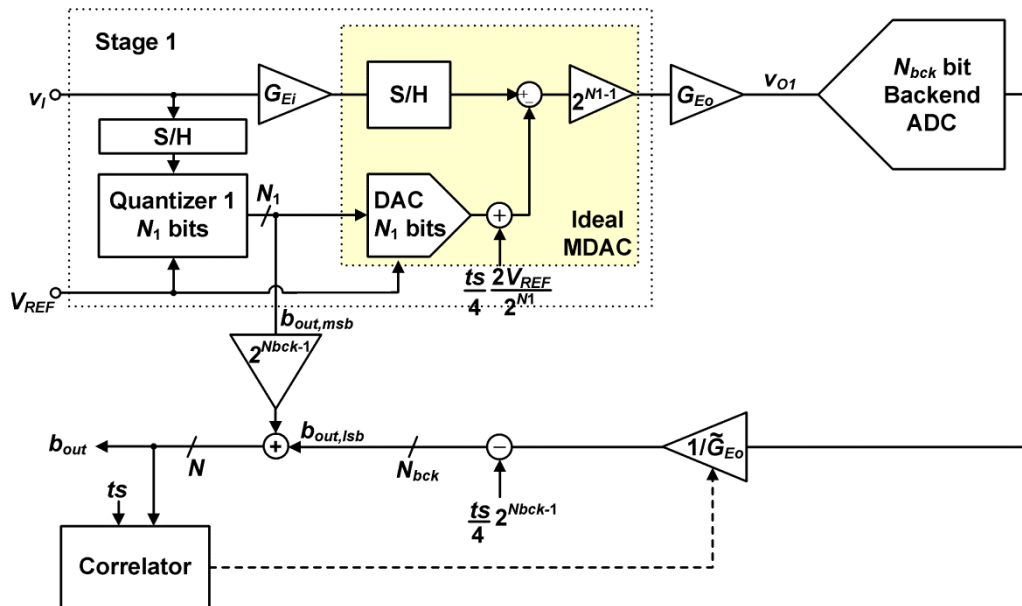


12b 200MS/s digitally calibrated pipeline ADC

■ Determination of digital coefficients



Foreground
(Fast Startup)



U.S. Patent
8 742 961

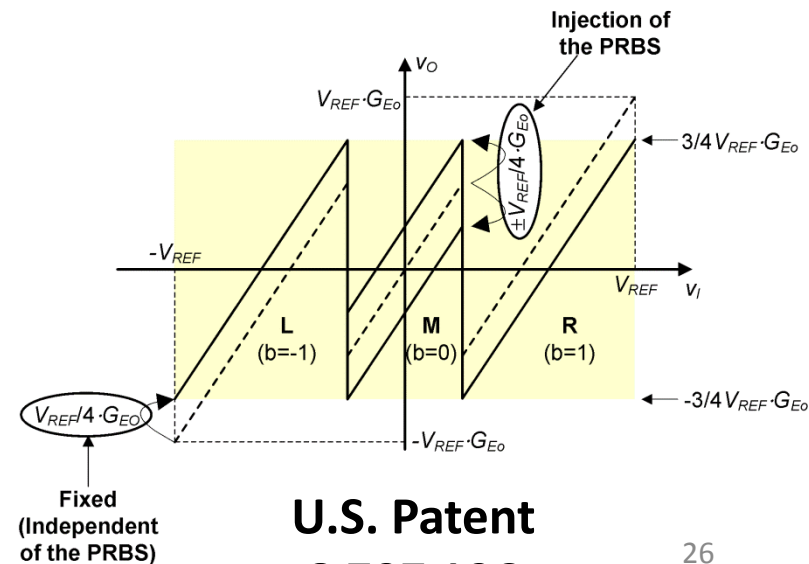
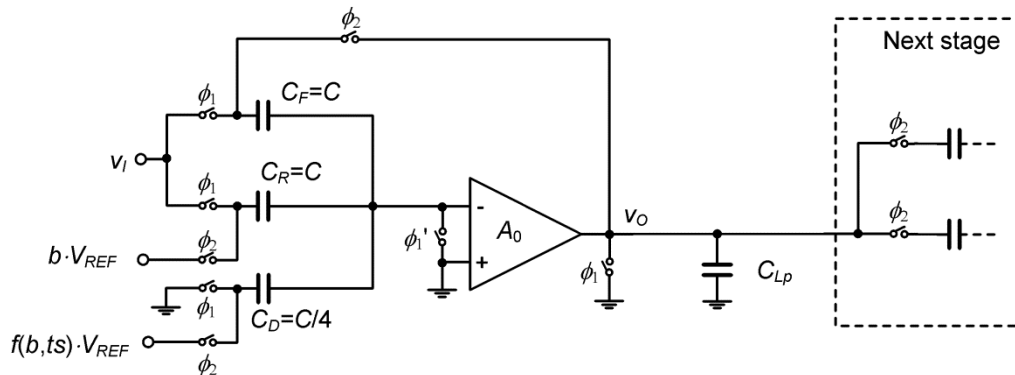
Background
(Adapt coef. as
VDD/Temp varies)

12b 200MS/s digitally calibrated pipeline ADC

■ Capacitor C_D :

- Injects the Pseudo-Random Binary Sequence on the central segment
- Shifts L/R segments in order to reduce signal swing
 - Lower amplifier non-linearity
 - Relaxed settling specifications

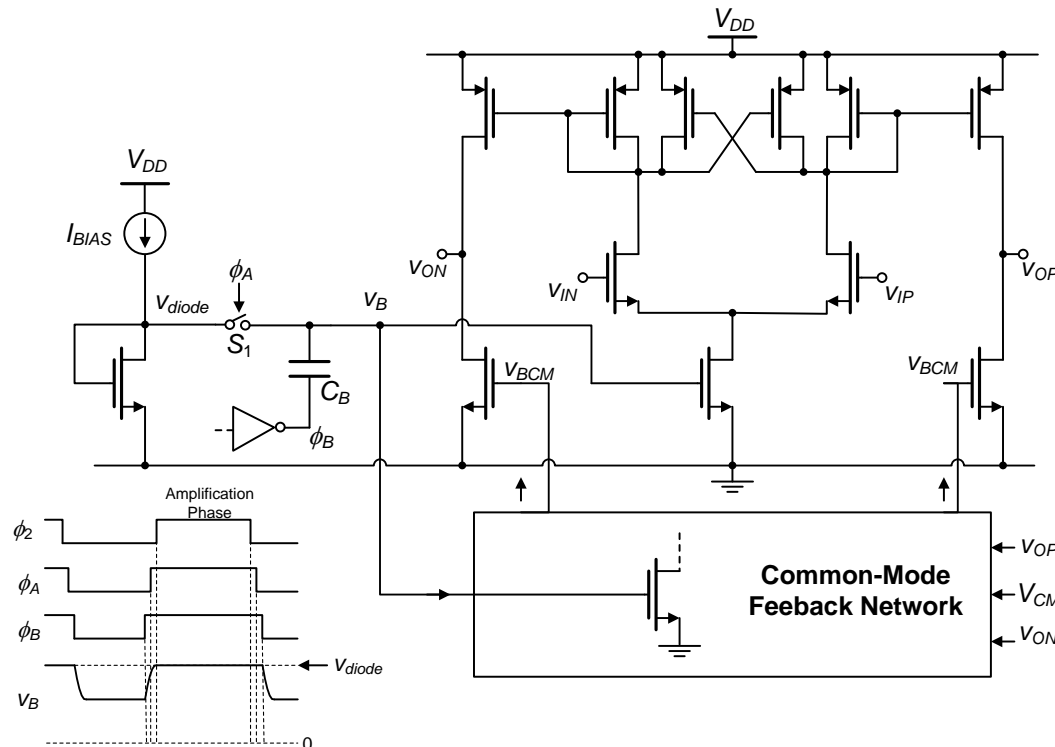
ϕ_1 : sampling phase
 ϕ_2 : amplification phase



12b 200MS/s digitally calibrated pipeline ADC

■ Amplifier:

- Single stage, high-swing $\rightarrow A_0\beta \approx 16\text{dB}$ only
- Switching of C_B reduces power consumption in ϕ_1
 - No speed or signal swing limitations

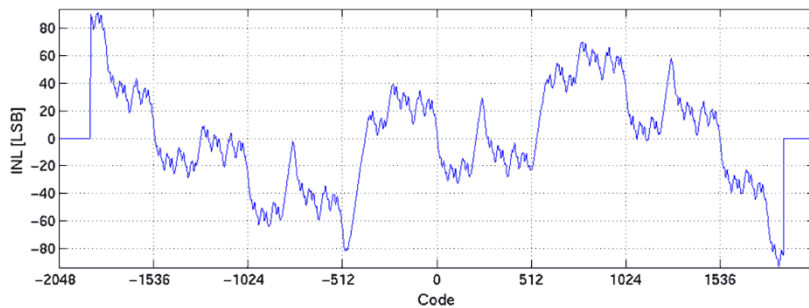
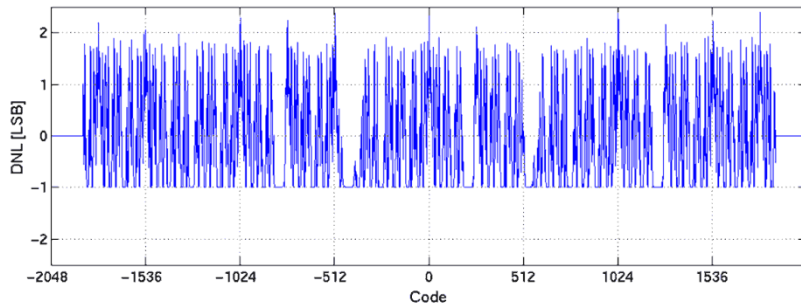


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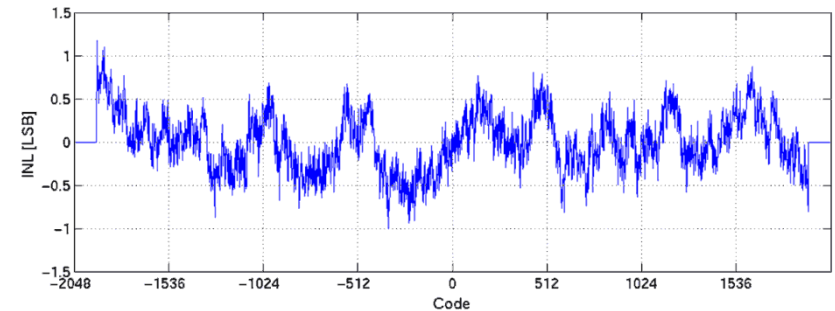
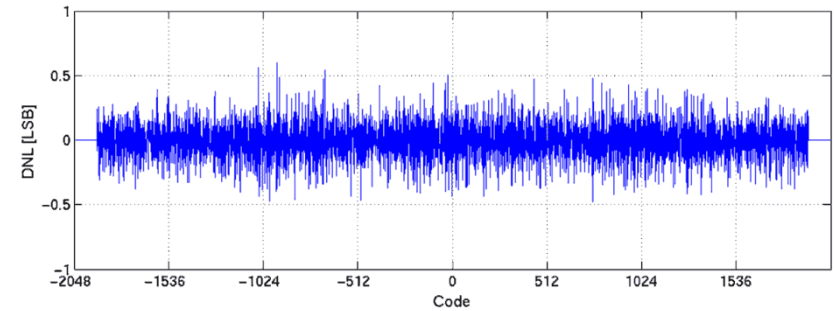
12b 200MS/s digitally calibrated pipeline ADC

- Measurement results:

Calibration off



Calibration on

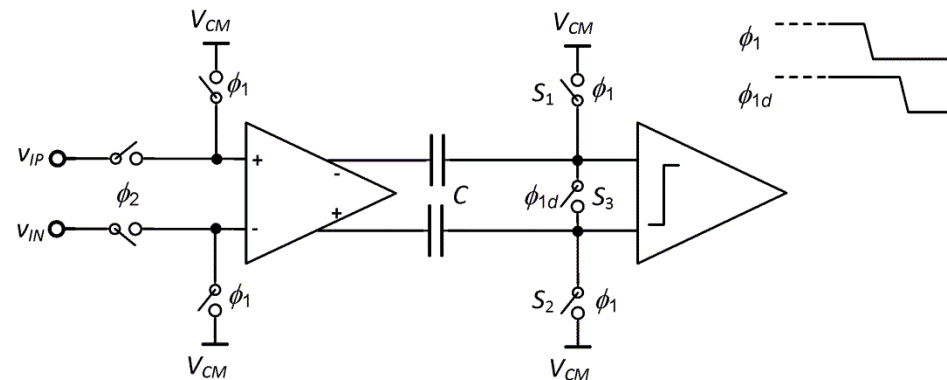
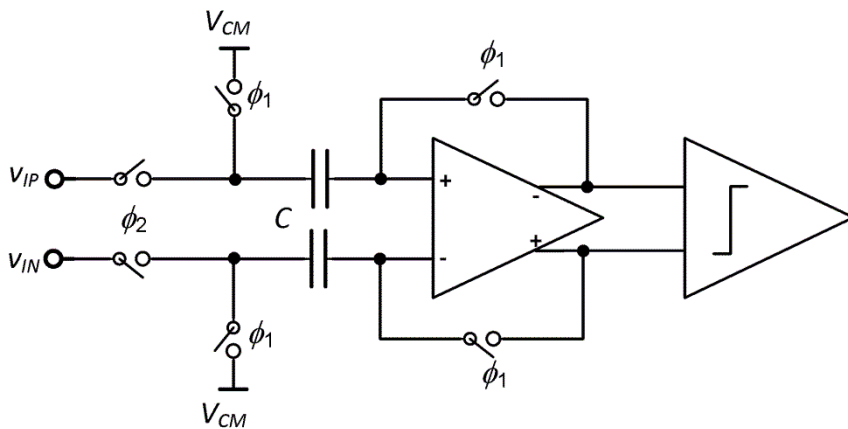


Quantizer-only ADCs

- No need for highly linear or gain accurate blocks
→ better adapted to nanometer technologies
- Non-linearity of the DACs inside the quantizers:
 - Caused by random deviations on its constitutive elements
 - Matching improved by using devices with larger area
 - **Resistive ladder DACs**: increased parasitics
 - **Switched capacitor DACs**: sets a minimum limit for the value of the capacitors (as does noise)
 - May also be addressed by digital calibration

Quantizer-only ADCs

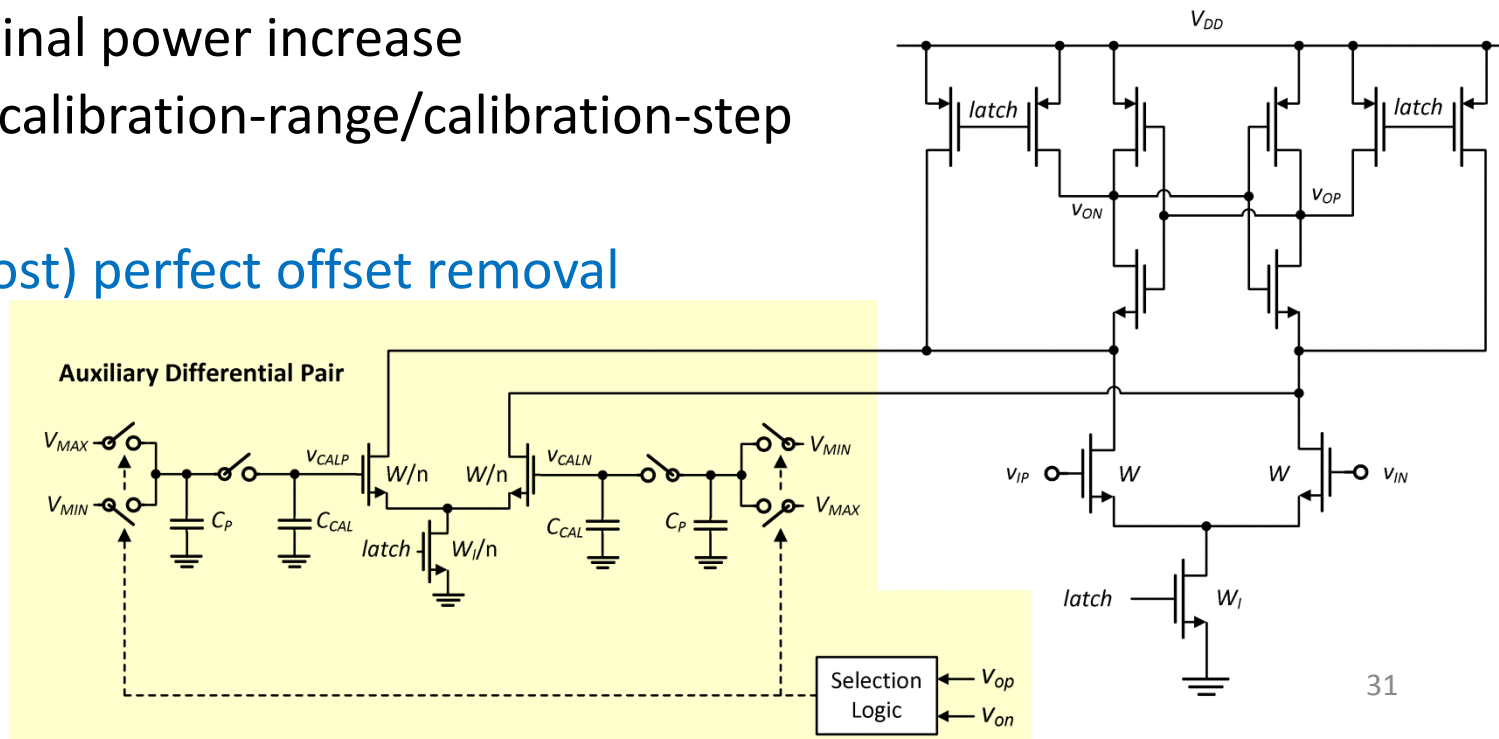
- Performance of flash/subranging/time-interleaved SAR ADCs limited by comparator offsets
- Add pre-amplifier with offset sampling
 - Static consumption
 - Non-negligible residual offset [23]



Quantizer-only ADCs

■ Offset calibration:

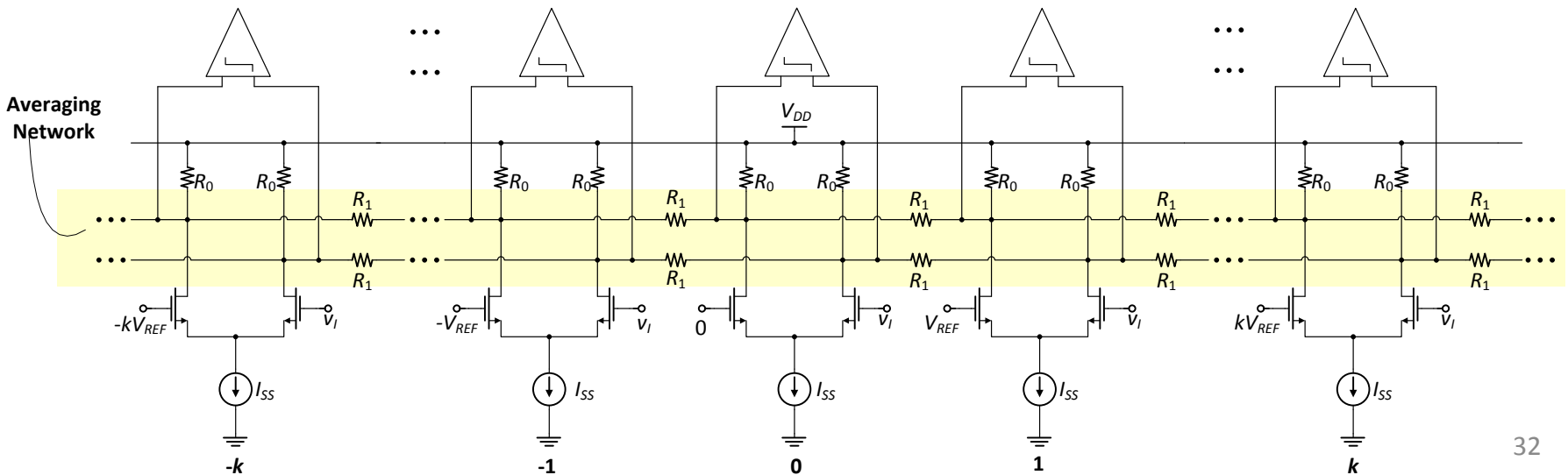
- Programmable capacitor or current source arrays in dynamic comparator [24,25]
- Auxiliary diff pair and switched capacitor integrator [23,26]
 - No speed reduction
 - Marginal power increase
 - High calibration-range/calibration-step ratio
 - (Almost) perfect offset removal



Quantizer-only ADCs

■ Averaging [23,27,28]

- Offset of comparators is a weighted sum of several amplifiers
- Offsets become correlated
- Lower area devices may be used

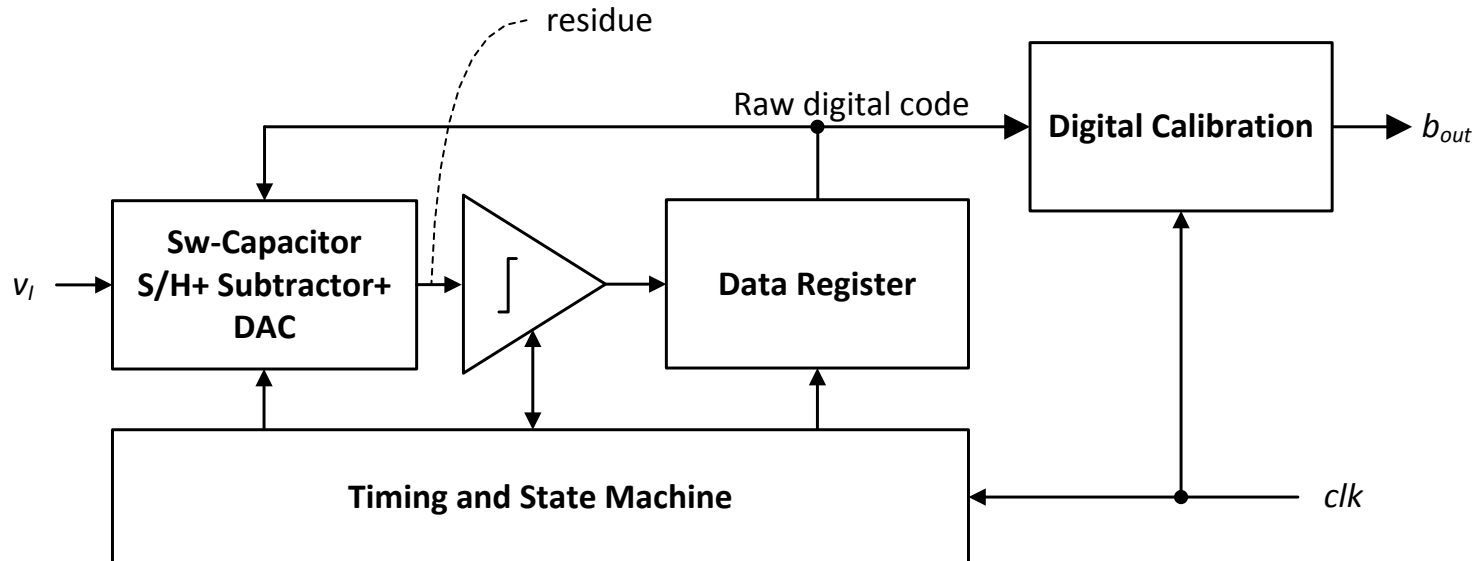


Quantizer-only ADCs

- **Stochastic flash ADCs [29,30]:**
 - **Fully synthesized in a digital flow**
 - $\gg 2^N$ minimum size comparators with the same V_{REF}
 - Output code obtained by counting the number of '1'
 - Nonlinear transfer function: Gaussian cumulative distribution \rightarrow Linearization through digital calibration

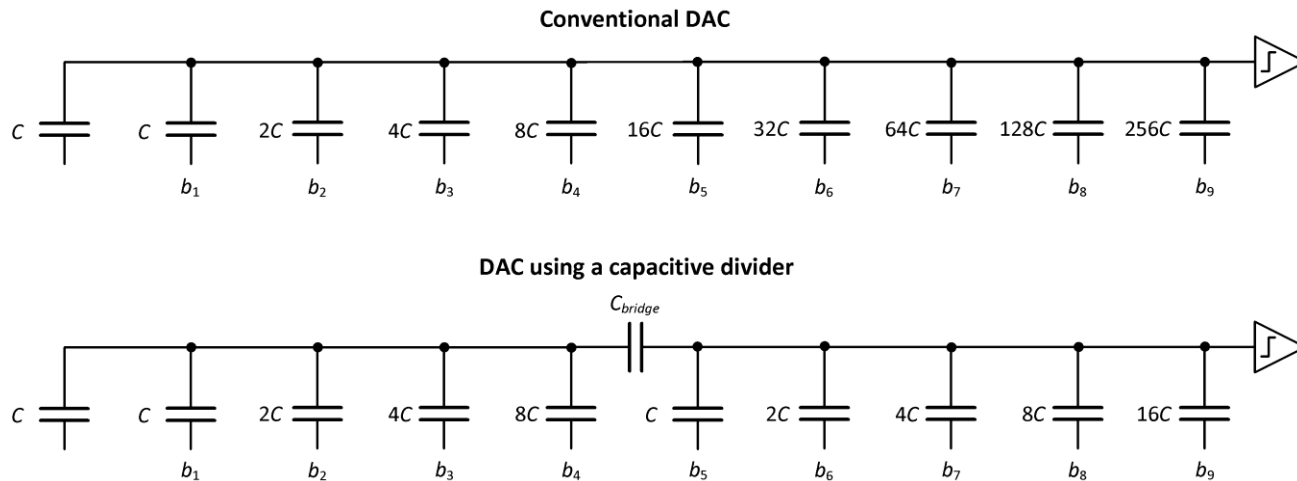
12b 80MS/s digitally calibrated SAR ADC

- Asynchronous architecture.
- Operation independent of clk duty cycle
- Low noise fully dynamic comparator
- Use of time-interleaving: 12b 160MS/s and 320MS/s ADCs



12b 80MS/s digitally calibrated SAR ADC

- DAC with capacitive dividers avoids the exponential increase on the number of (small) unit capacitors

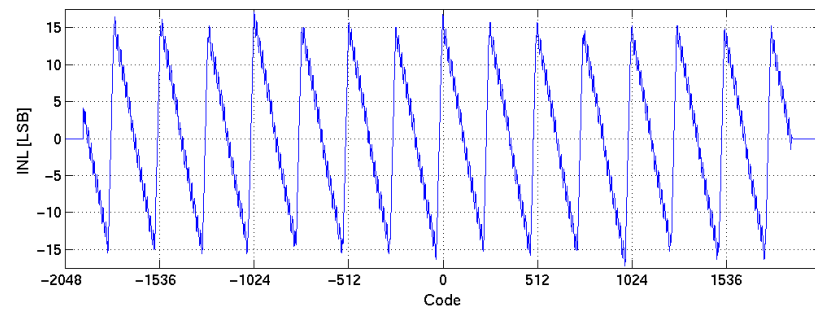
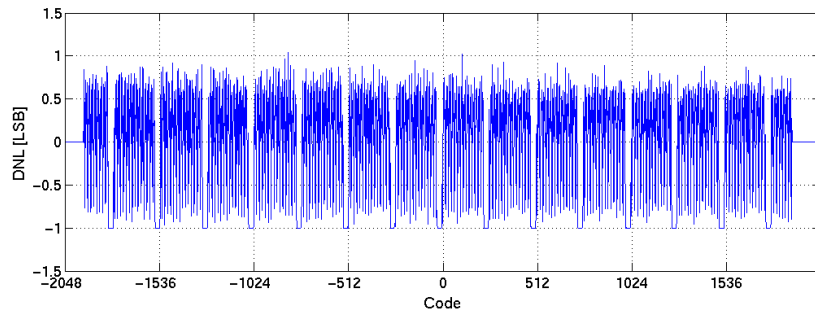


- **Digital calibration:** addresses random capacitor mismatches and sensitivity to parasitics in the capacitive divider nodes.
 - Measures capacitor ratios at startup
 - Corrects the raw code provided by the SAR

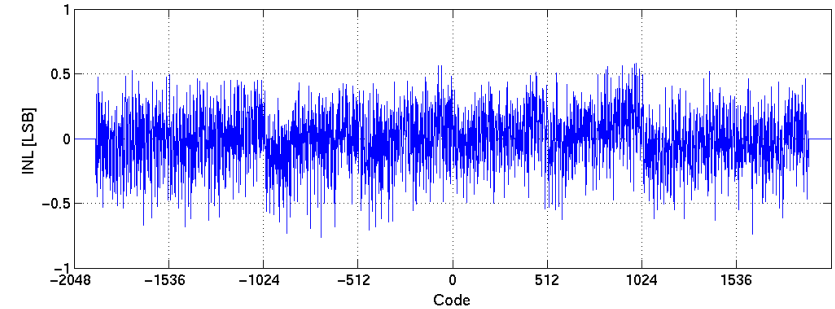
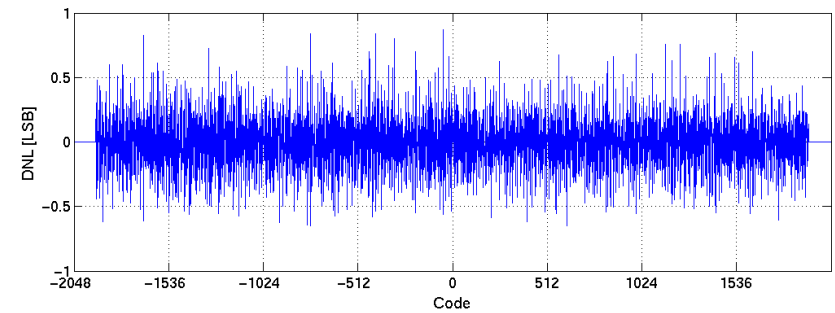
12b 80MS/s digitally calibrated SAR ADC

- Measurement results:

Calibration bypassed



Calibration on



Conclusions

- Reviewed ADC performance evolution in the last 10 years
- **Main trend: energy efficiency improvement**

Conclusions

- ADC architectures
 - SAR ADC is the direct implementation of the elementary multi-bit ADC architecture
 - Speed increase: use **parallelization in the code-search process** or **pipelining**
 - This yields ADCs based only on quantizers, and those based on residue amplification for further quantization
 - ...which have significantly different trade-offs
 - Speed also increases by **parallelizing in time-domain: time-interleaving**

Conclusions

- Reviewed challenges/benefits introduced by technology scaling
- **Digitally Assisted Analog** trend:
 - Relaxed analog circuits' complexity...
 - ...traded favorably by extra digital complexity
- Disclosed a few details about Synopsys 12b digitally calibrated pipeline and SAR ADCs
 - Illustrated how the use of digital calibration can dramatically improve performance

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obrigado

Dank U

Merci

mahalo

Köszí

спасибо

Grazie

Thank
you

mauruuru

Takk

Gracias

Dziękuję

Děkuju

danke

Kiitos

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