GBLD10+: A Compact Low-Power 10 Gb/s VCSEL Driver

Tao Zhang[1], Szymon Kulis[3], Ping Gui[1]
Filip Tavernier[2] and Paulo Moreira[3]
[1]SMU, Dallas, Texas, USA
[2]KU Leuven, Leuven, Belgium
[3]CERN, Geneva, Switzerland

Sept. 28 - Oct. 03, 2015 TWEPP 2015

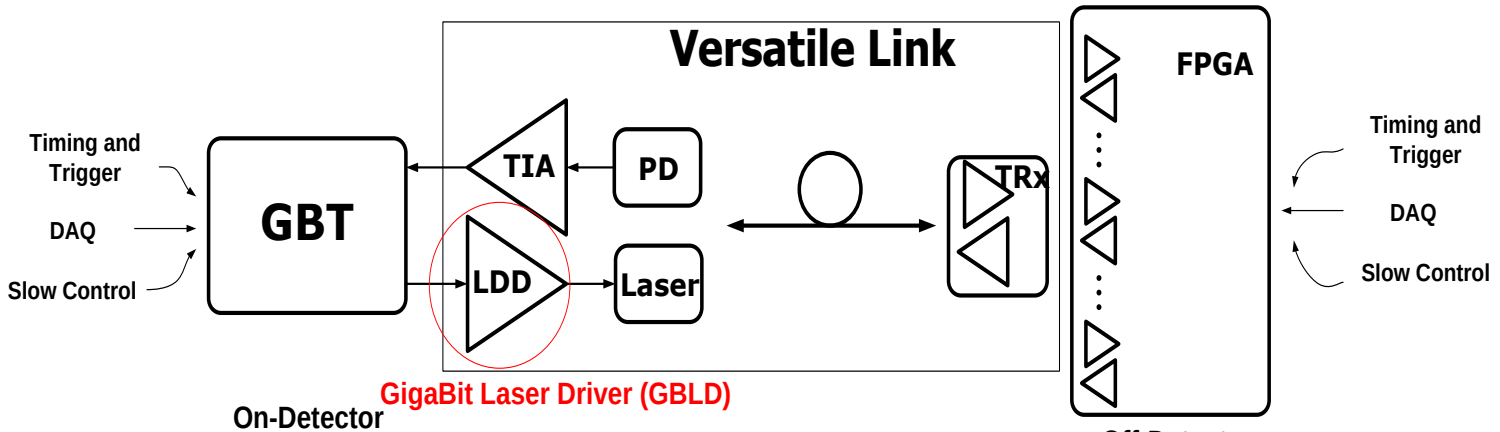
taoz@smu.edu

Outline

- **Background**
- **GBLD10+ Design Requirements and Challenges**
  - Area / Speed / Power
- **GBLD10+ Design**
  - Architecture
  - Circuit Design and Implementation
- **GBLD10+ Measurement Results**
- **Summary**

taoz@smu.edu

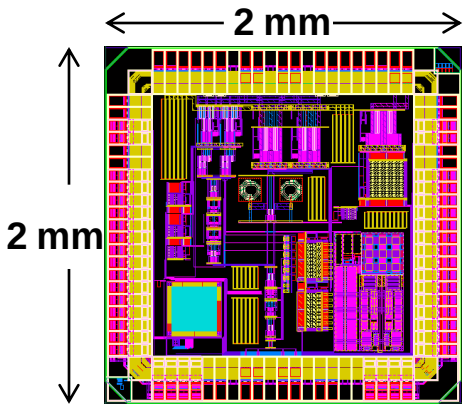
Background



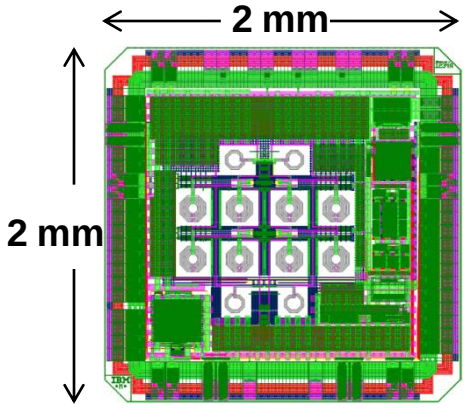
GigaBit Laser Driver (GBLD)

On-Detector
Custom Electronics & Packaging
Radiation Hard

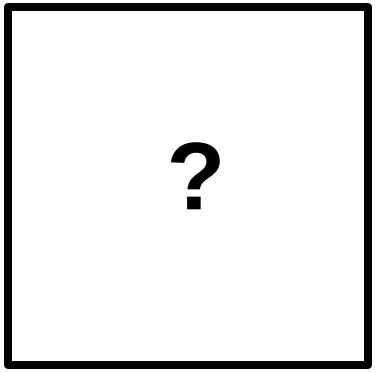
Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol



- **GBLD**
  - 5 Gb/s
  - 130 nm CMOS
  - ~300 mW
  - TOSA

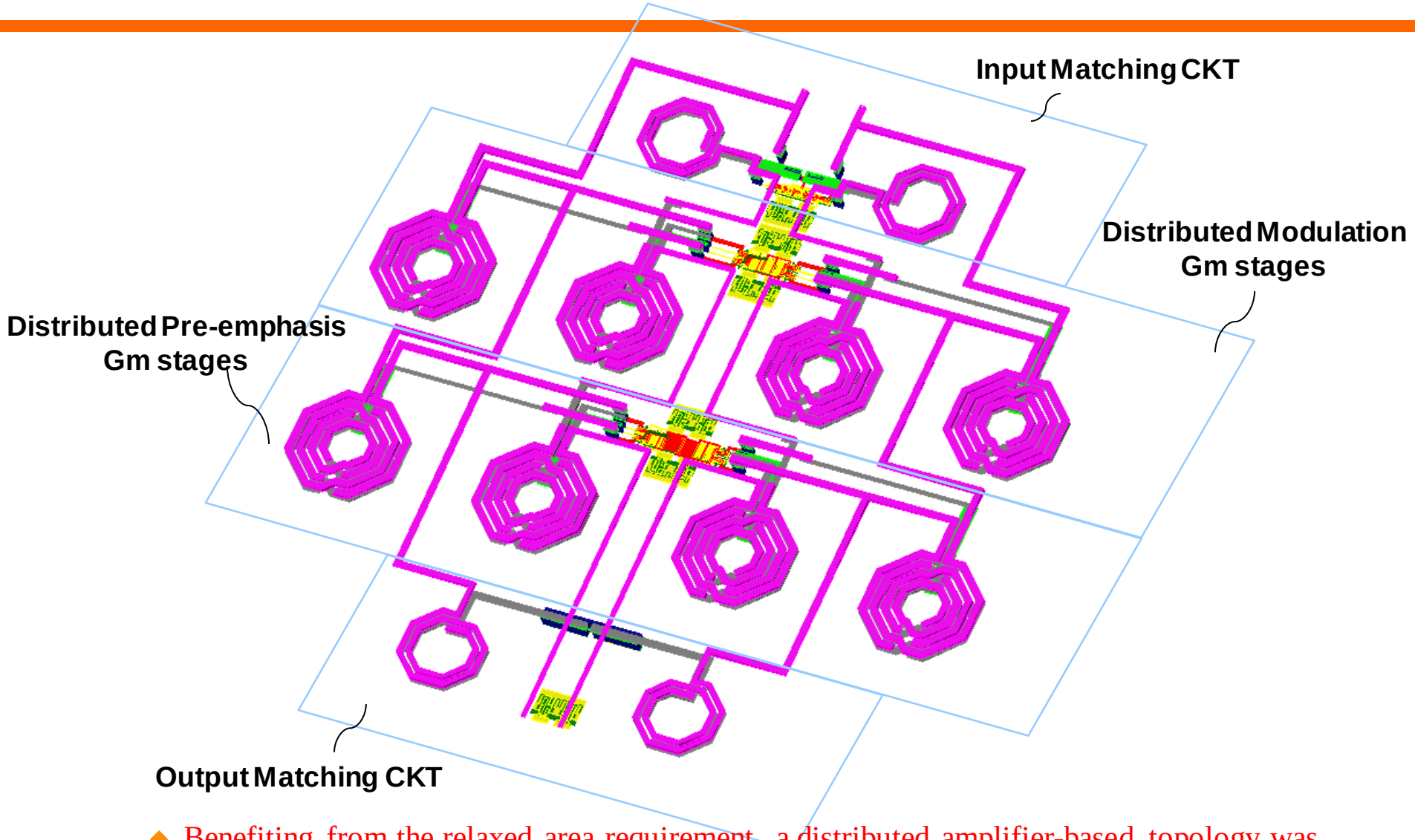


- **GBLD10**
  - 10 Gb/s
  - 130 nm CMOS
  - 85 mW
  - TOSA



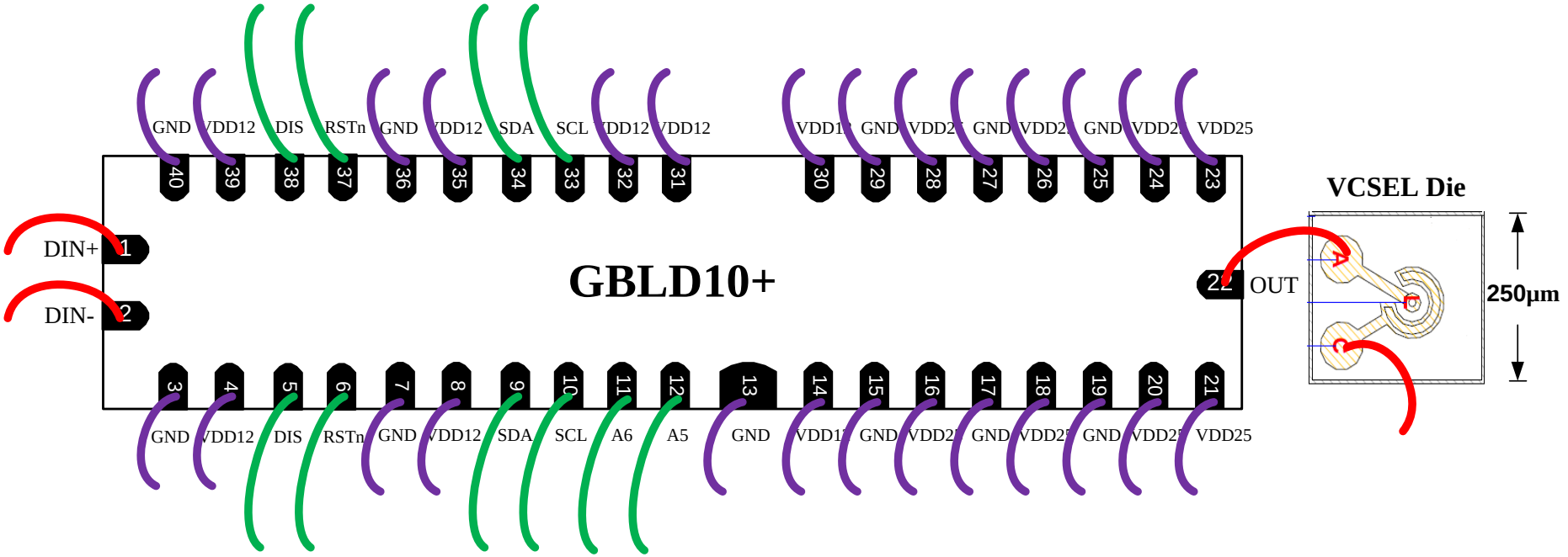
- **GBLD10+**
  - 10 Gb/s
  - 65 nm CMOS
  - VCSEL die

Speed Boosting Approach for TOSA Driver (GBLD10)



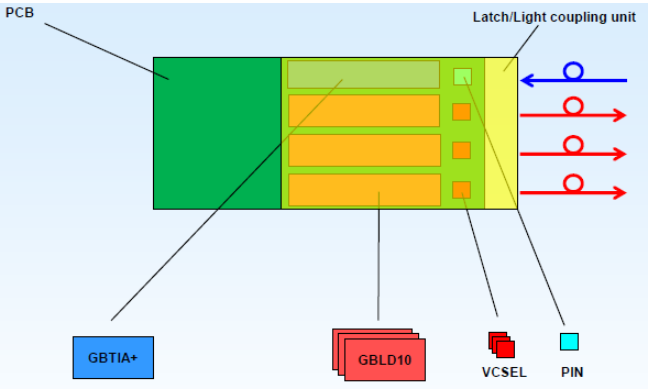
- Benefiting from the relaxed area requirement, a distributed amplifier-based topology was proposed to boost the speed to 10 Gb/s in 130 nm CMOS in GBLD10

Area Requirements from VCSEL

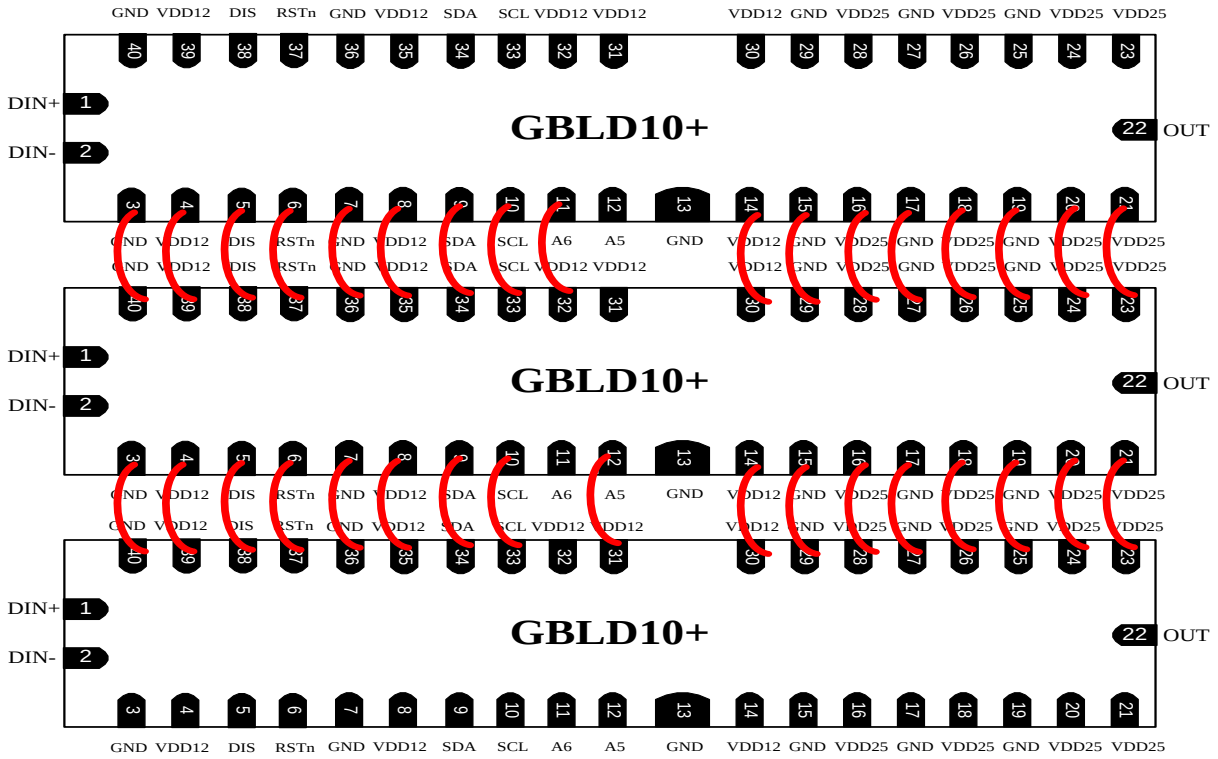


- **GBLD10+ is a laser driver with single-ended output directly bonded to the anode of the VCSEL die**
  - **No need for external components**
  - **Die width compatible with the VCSEL die**

Area Requirement from Pads

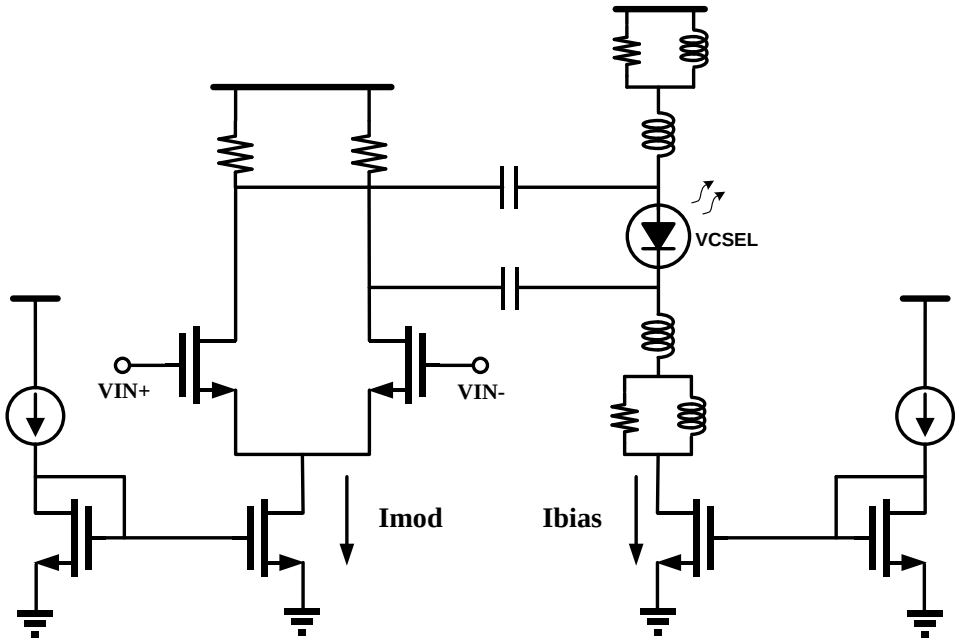


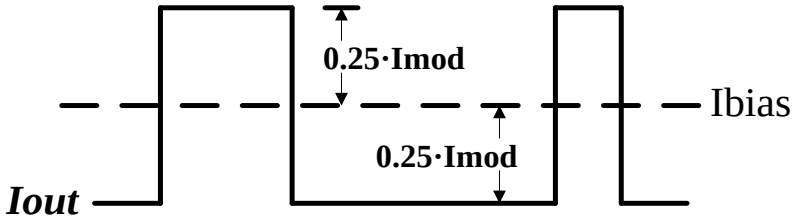
Transceiver with 3Tx and 1Rx



- Pad count is 40
  - Versatile layout for channel number customization → Digital I/O pads are duplicated
  - Small equivalent inductance to minimize ground (and power) bouncing → 3 pairs of supply pads for both the 1.2 V and 2.5 V power domain
- PAD size should be larger than (70 µm × 110 µm) for good assembly yield
- GBLD10+ die size < 1800 µm × 400 µm – Challenging!

Differential Driver Speed Limitation

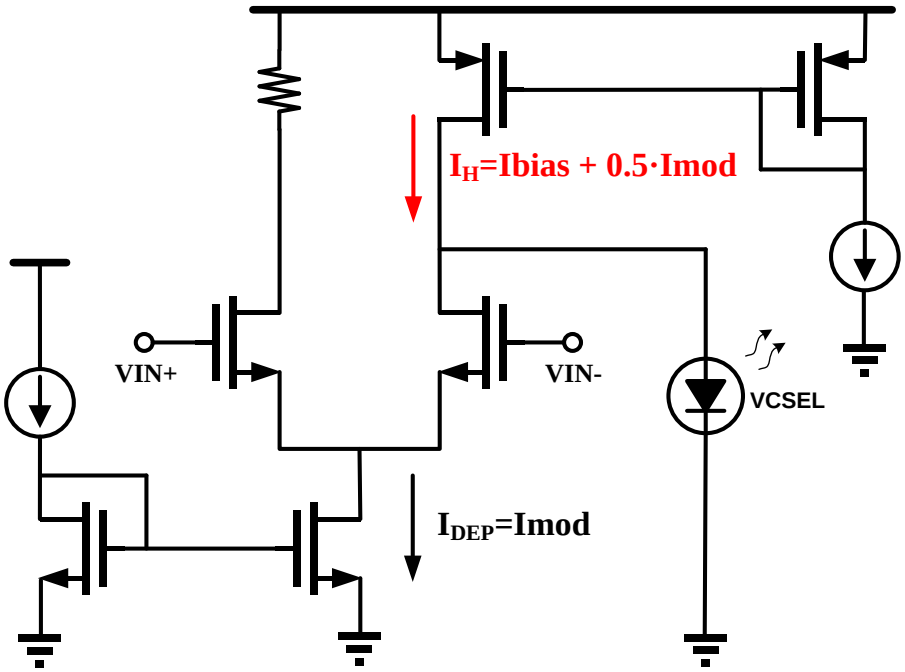


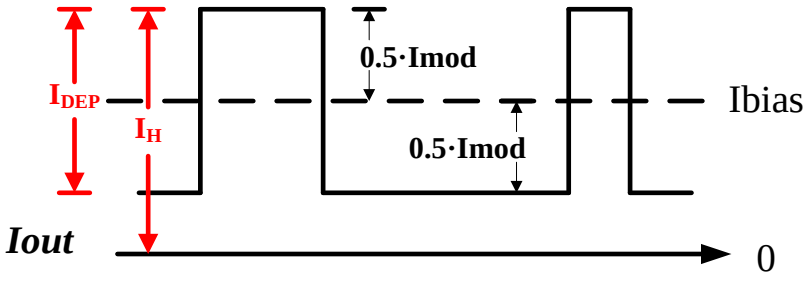


Output driver topology for GBLD/GBLD10

- **Biasing and modulation functions are separated**
- **Main circuit parasitics are due to the NMOS switch which carries 0.5·Imod**
- **Bias parasitic effects can be suppressed**

Single-ended Driver Speed Limitation





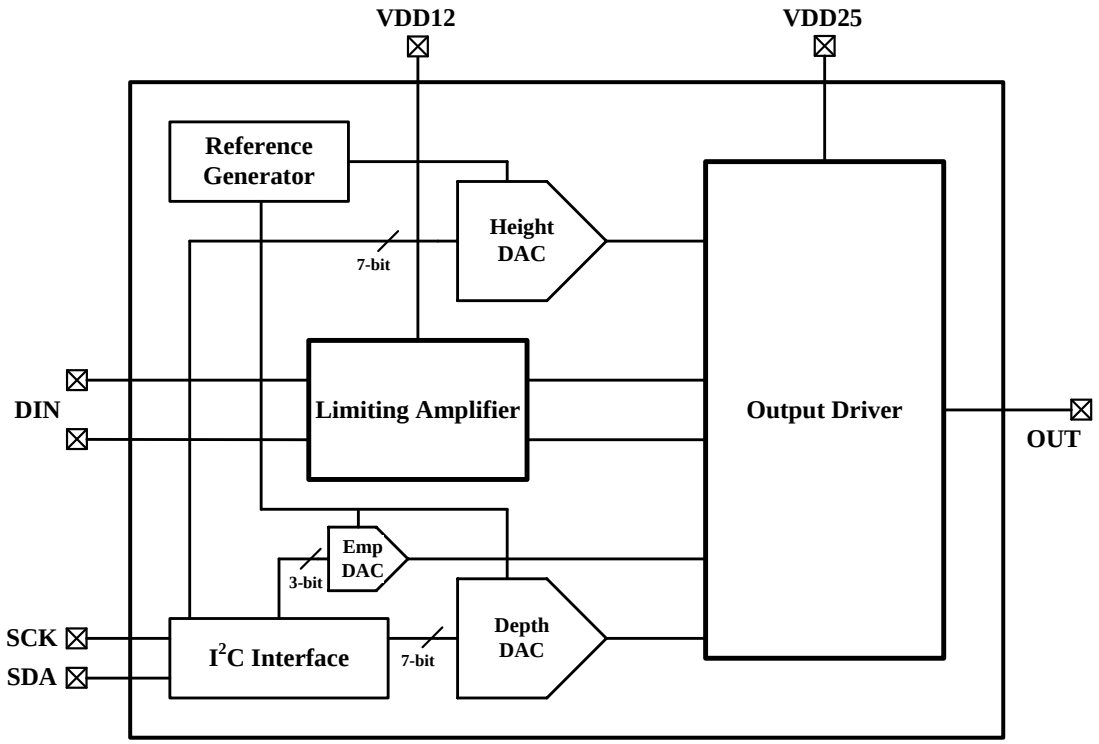
Output driver topology for GBLD10+

- Biasing and modulation functions are combined
- Main circuit parasitics are due to both the NMOS switch which carries 0.5·Imod and the PMOS current source which carries Ibias + 0.5·Imod
- Speed is mainly limited by the parasitics from large PMOS carrying large currents

Design Challenges

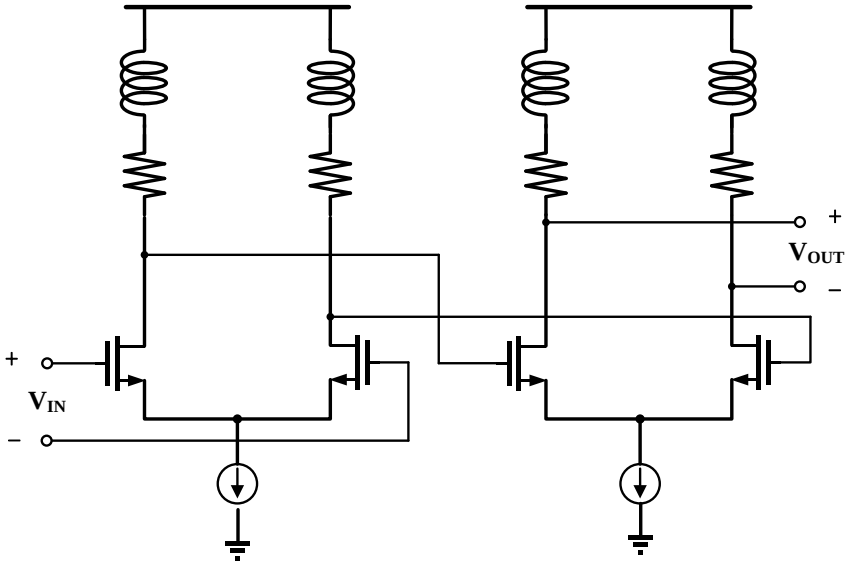
- **Area (< 1800 µm × 400 µm)**
  - **Compact size requirement limits the available approaches to boost the speed**
- **Speed (10 Gb/s)**
  - **Limited by Anode driving topology**
- **Power (< 50 mW)**
  - **Trade-off with the speed**

GBLD10+ Block Diagram

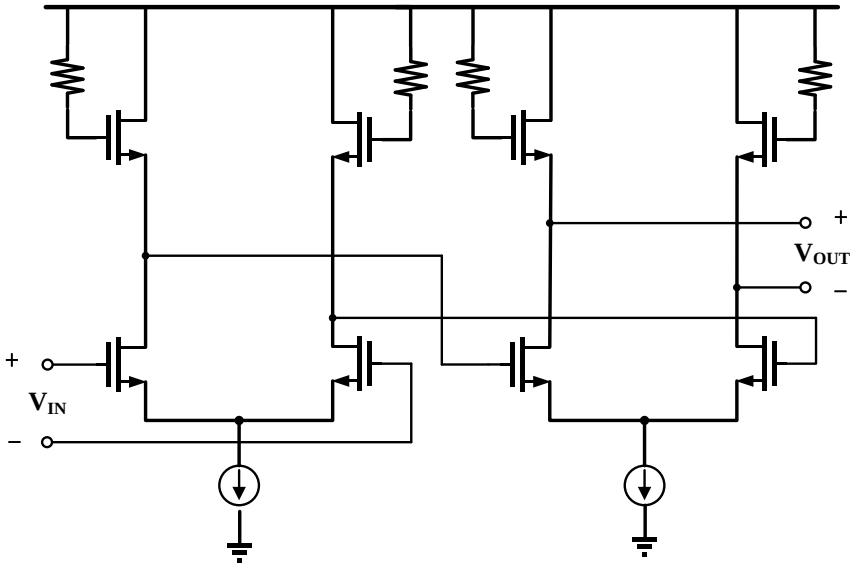


- **Limiting Amplifier**
  - Provides enough gain to guarantee full-swing modulation
  - Gain ≥ 12 dB
  - Bandwidth > 12 GHz
- **Output Driver**
  - Includes the configurable rising/falling edge pre-emphasis
- **Height/Modulation/Emphasis DACs**
  - Biasing current 0-12 mA
  - Modulation current 0-10 mA

Limiting Amplifiers - Traditional Topologies

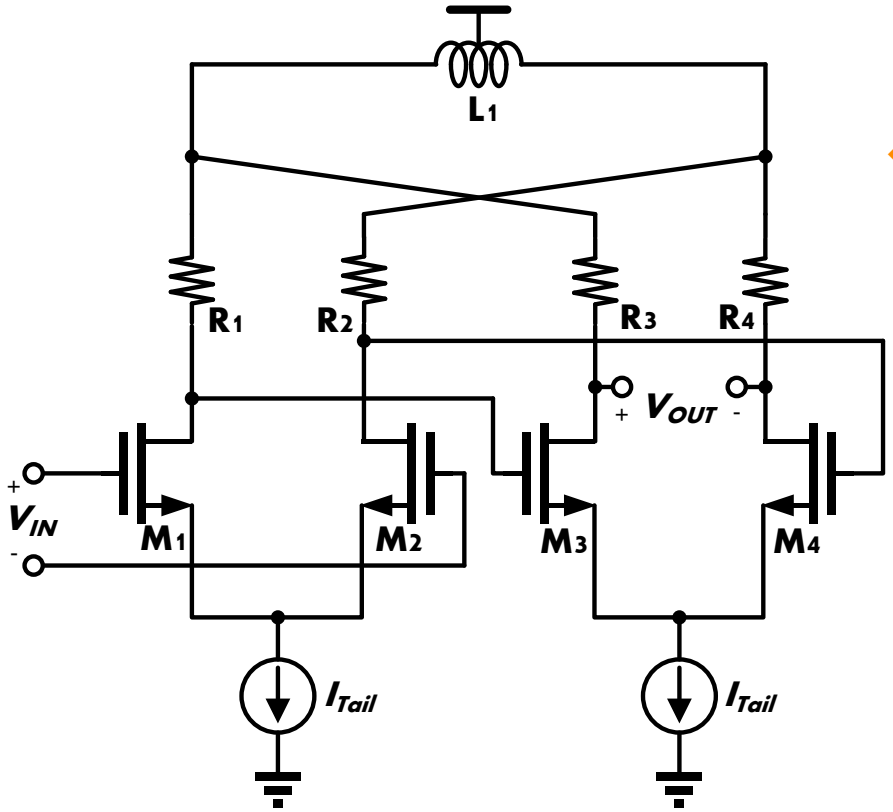


- **Passive Inductor Peaking**
  - **Pros**
    - High speed
    - Well-defined output DC voltage
  - **Cons**
    - Large area occupation



- **Active Inductor Peaking**
  - **Pros**
    - Compact size
  - **Cons**
    - Limited speed
    - Output DC voltage not well defined
    - Output swing limited

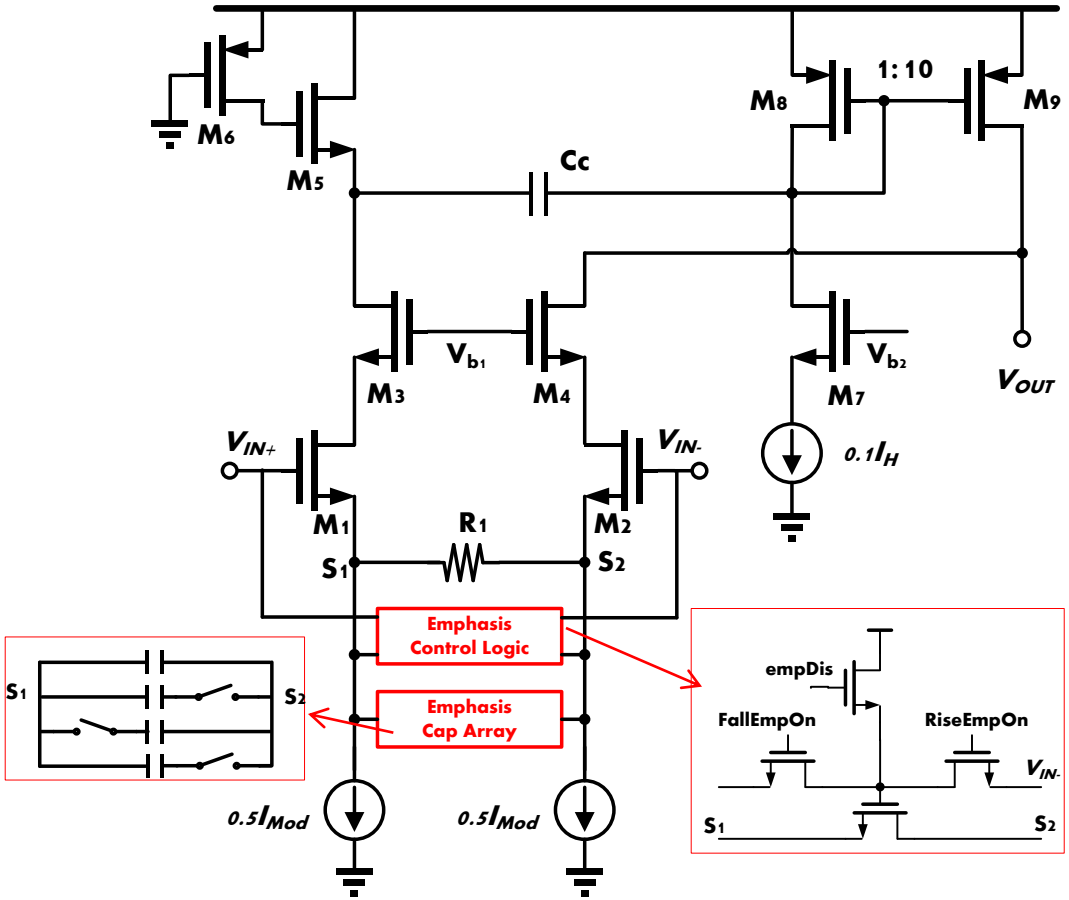
Limiting Amplifier Topology



- **Area-efficient Passive Inductor Peaking**
  - **Pros**
    - High speed
    - Well-defined output DC voltage
    - Small area occupation
  - **Cons**
    - Strict matching required in layout

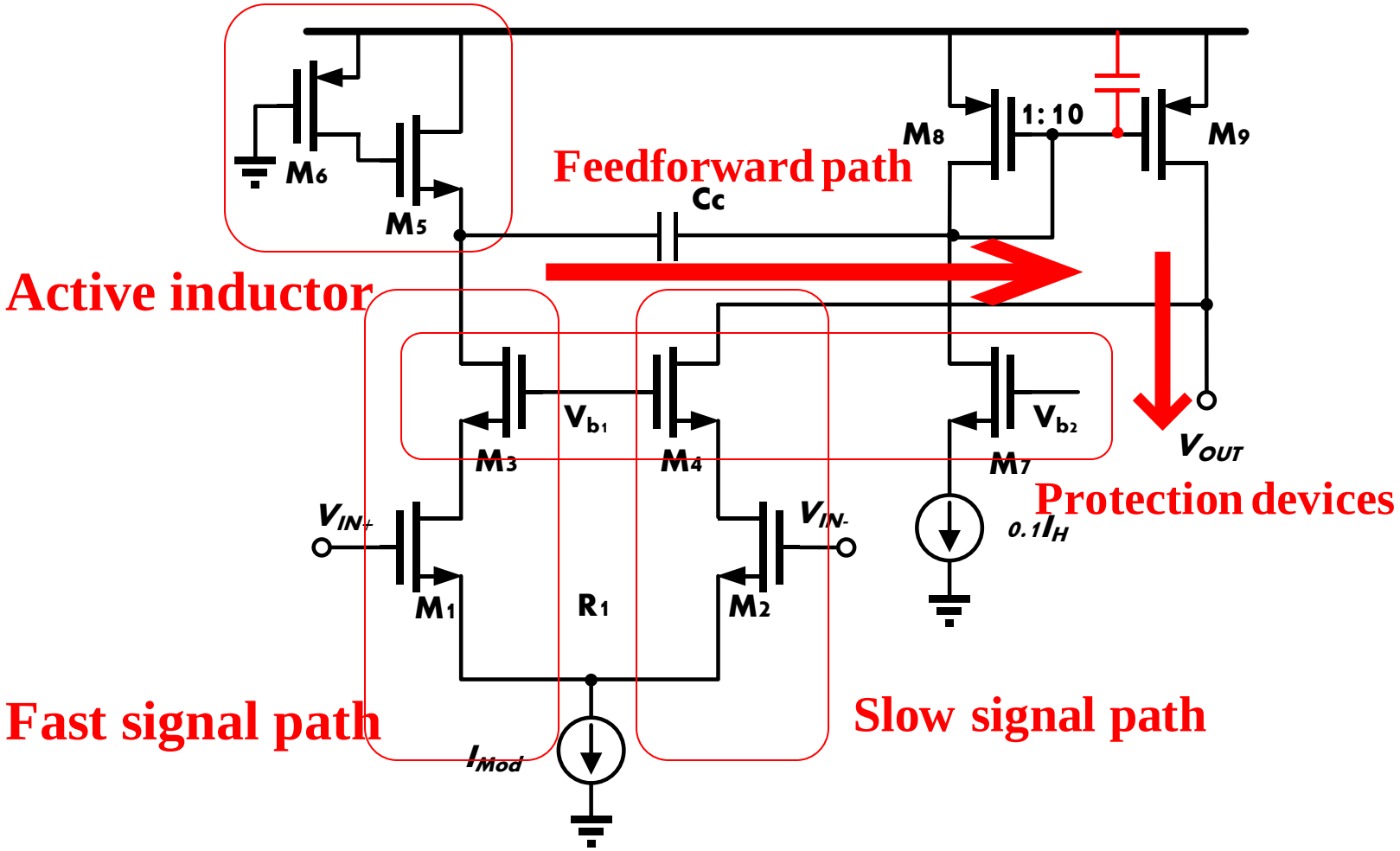
I_{supply} = 8mA
A_0 = 13.3 dB
BW = 14.8 GHz

Output Driver Topology



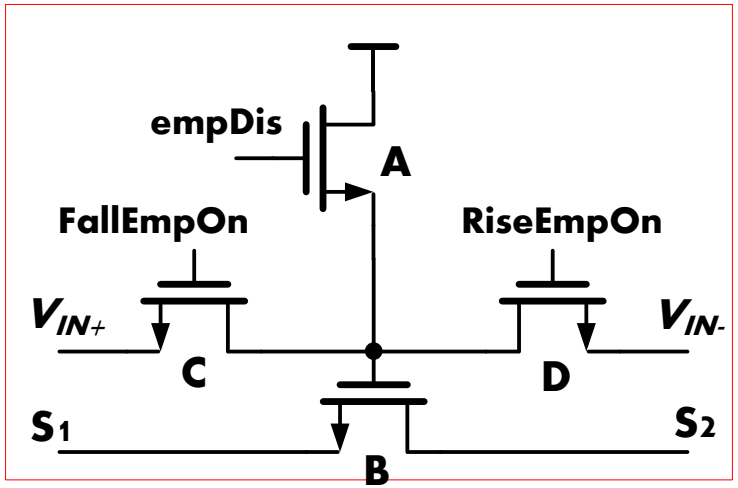
- Area-efficient high-speed output driver with configurable edge pre-emphasis

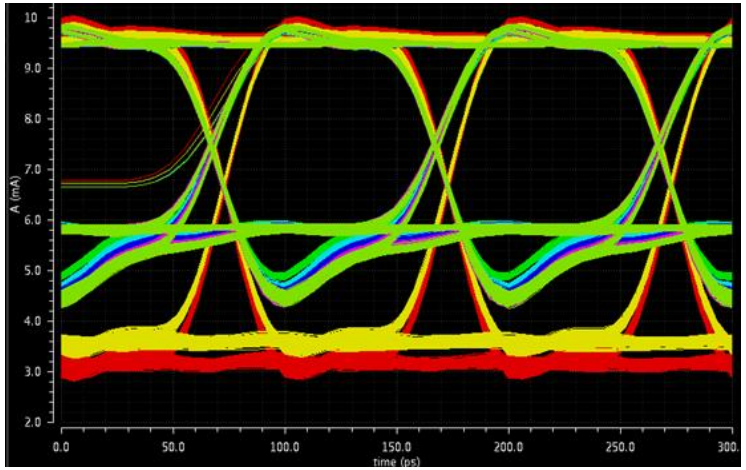
Speed Boosting for Modulation

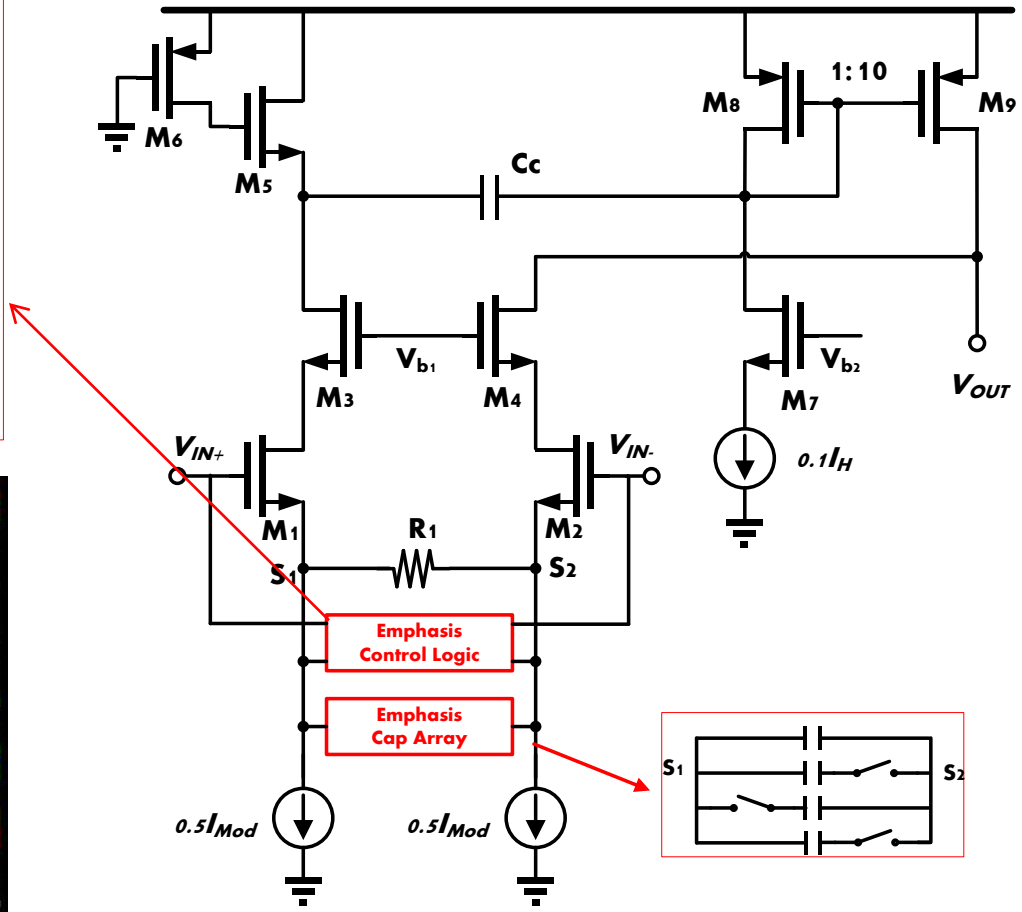


- Feedforward technique with one capacitor instead of inductors to boost the speed

Configurable Rising/Falling Edge Pre-emphasis

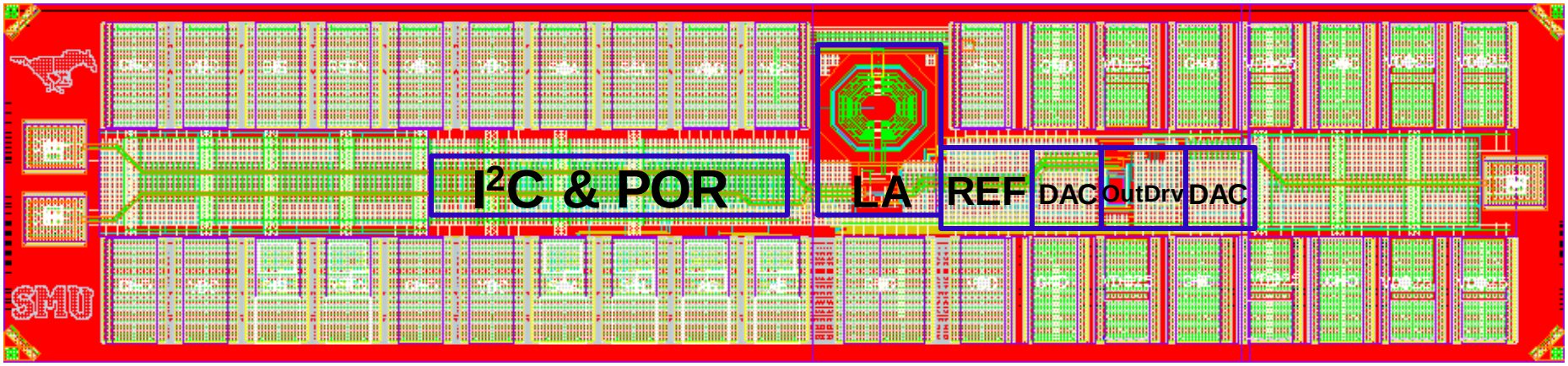


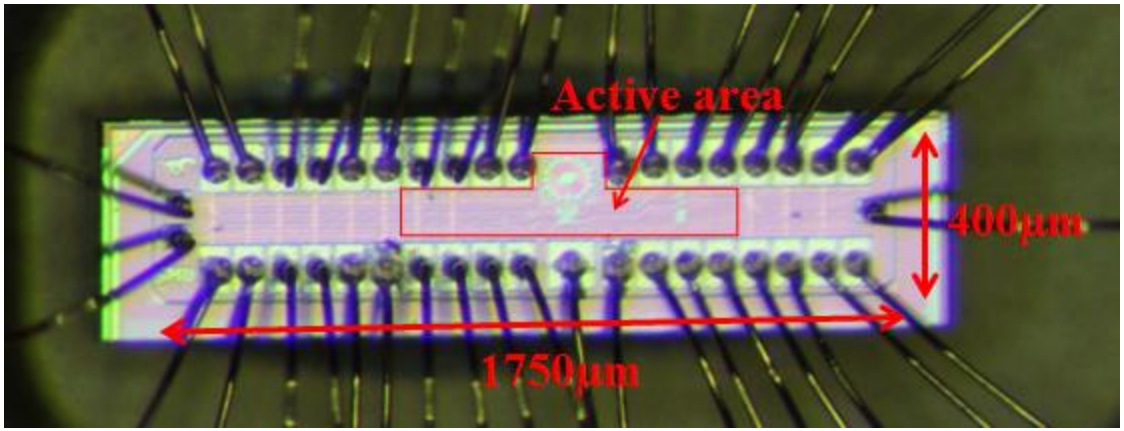




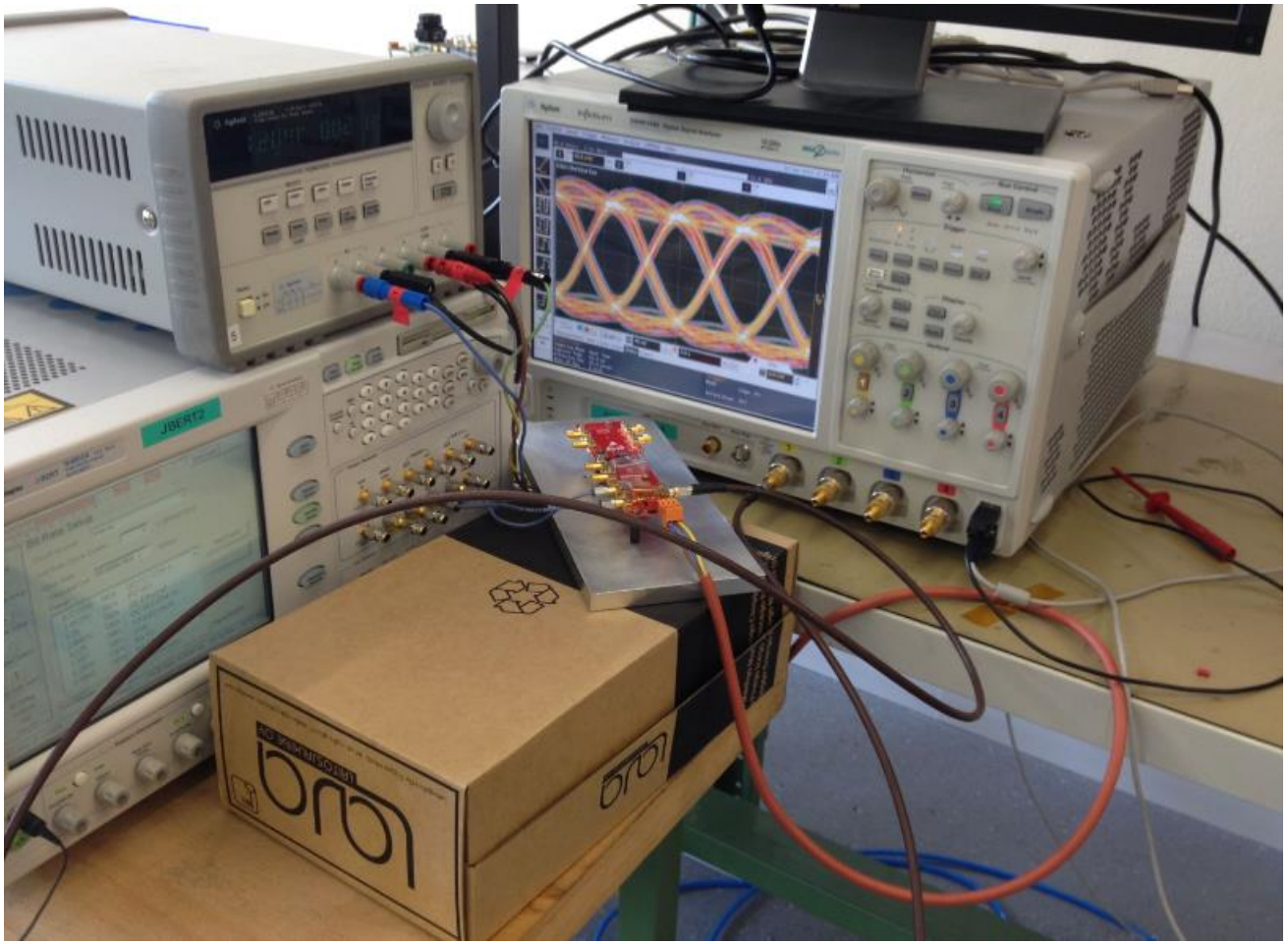
Falling edge pre-emphasis

Layout and Chip Photo

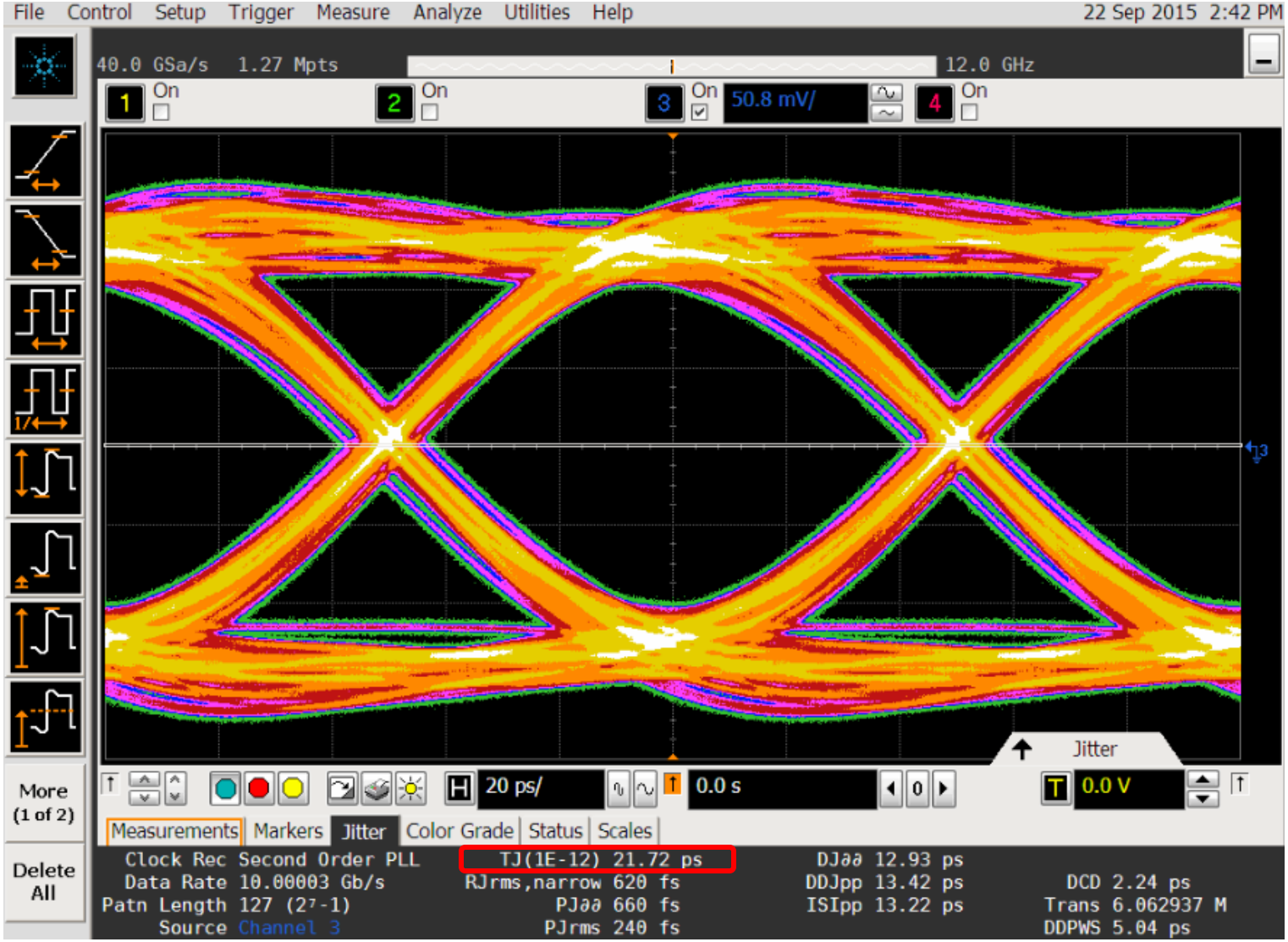




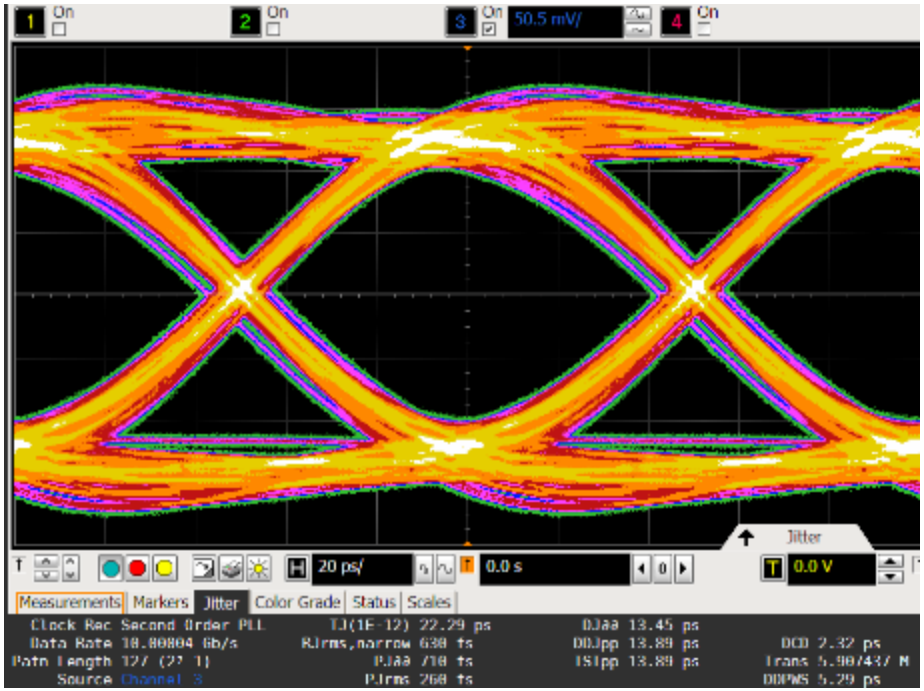
Test Setup for GBLD10+



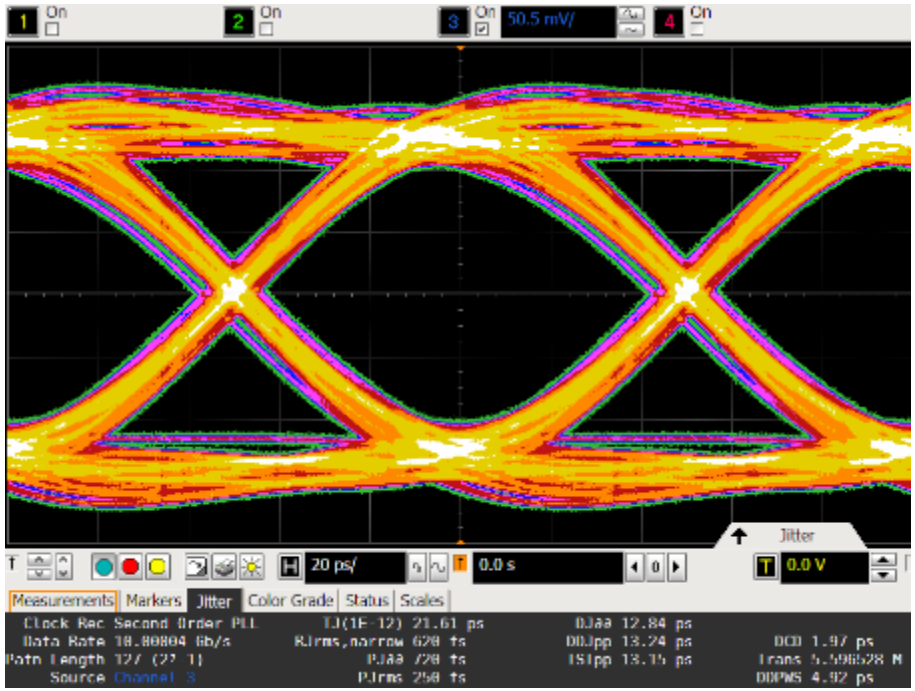
Electrical Eye Diagram @ 10 Gb/s



10 Gb/s Electrical Eye Diagram for Different Input Swings



Differential Input Swing = 200 mV



Differential Input Swing = 1.2 V

Limiting amplifier works as designed

GBLD10+ Power Consumption

Block	Current	Supply	Power
Limiting Amplifier	8 mA	1.2 V	9.6 mW
Output Driver	8 mA	2.5 V	20 mW
DACs/Reference	1mA	1.2 V	1.2 mW
Total	9 mA/1.2 V 8 mA/2.5 V	9 mA/1.2 V 8 mA/2.5 V	31 mW

Measurement is consistent with the expectation

Summary

Parameters	GBLD10	GBLD10+
Technology	130nm CMOS	65nm CMOS
Speed	10 Gb/s	10 Gb/s
Typical Power	85 mW	31 mW
Total Jitter @BER 10^{-12} (Electrical)	14 ps	22 ps
Area	2 mm × 2 mm	1.75 mm × 0.4 mm
Laser Coupling	differential AC with external components	single-ended direct bonding

- A mistake in digital I/O pads prevented full characterization
- More tests expected after Focused Ion Beam (FIB)
  - Emphasis tests
  - S parameter tests
  - Optical tests

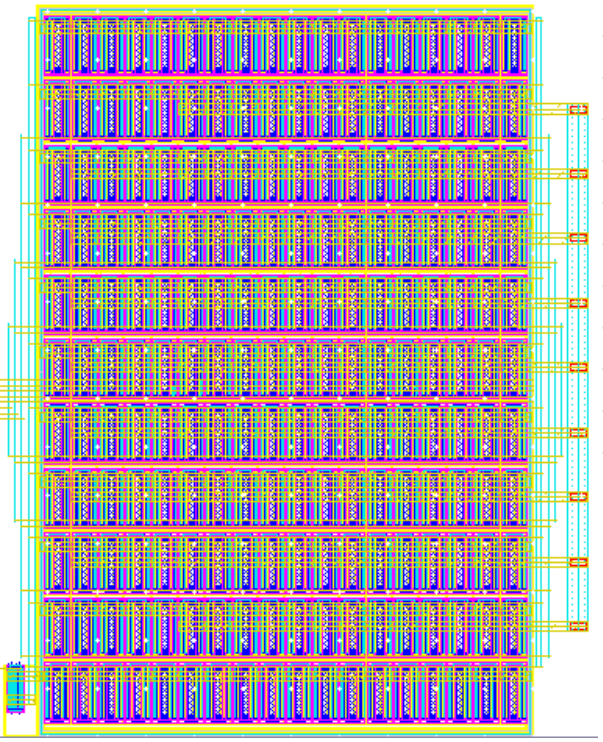
Acknowledgement

- **KU Leuven: Jeffery Prinzie and Paul Leroux for their help during the design, integration and dicing.**
- **CERN: Francois Vasey, Jan Troska, Christophe Sigaud, Giuseppe Pezzullo, Lauri Olanterä and Csaba Soos for their help on electrical and optical test setup.**
- **DoE/Collider Detector Research Program for funding of this project.**

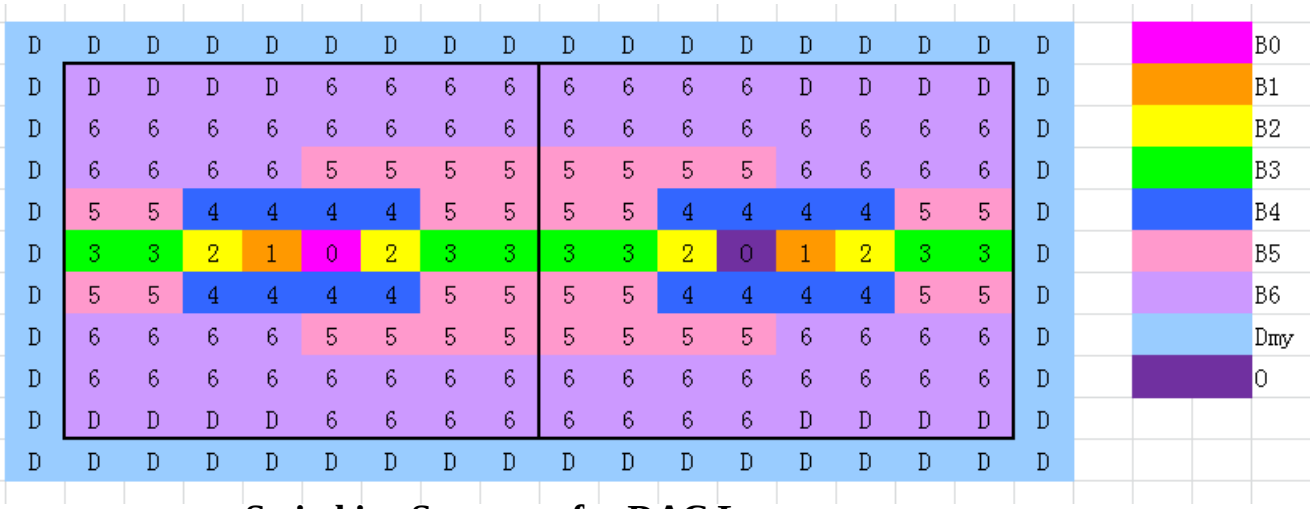
Thank you!

Back-up Slides

7-bit DAC



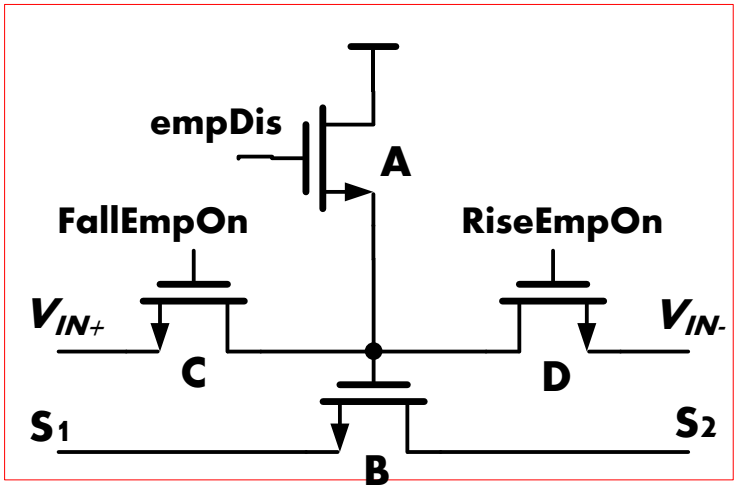
DAC Layout
(input is on left and output is on right)

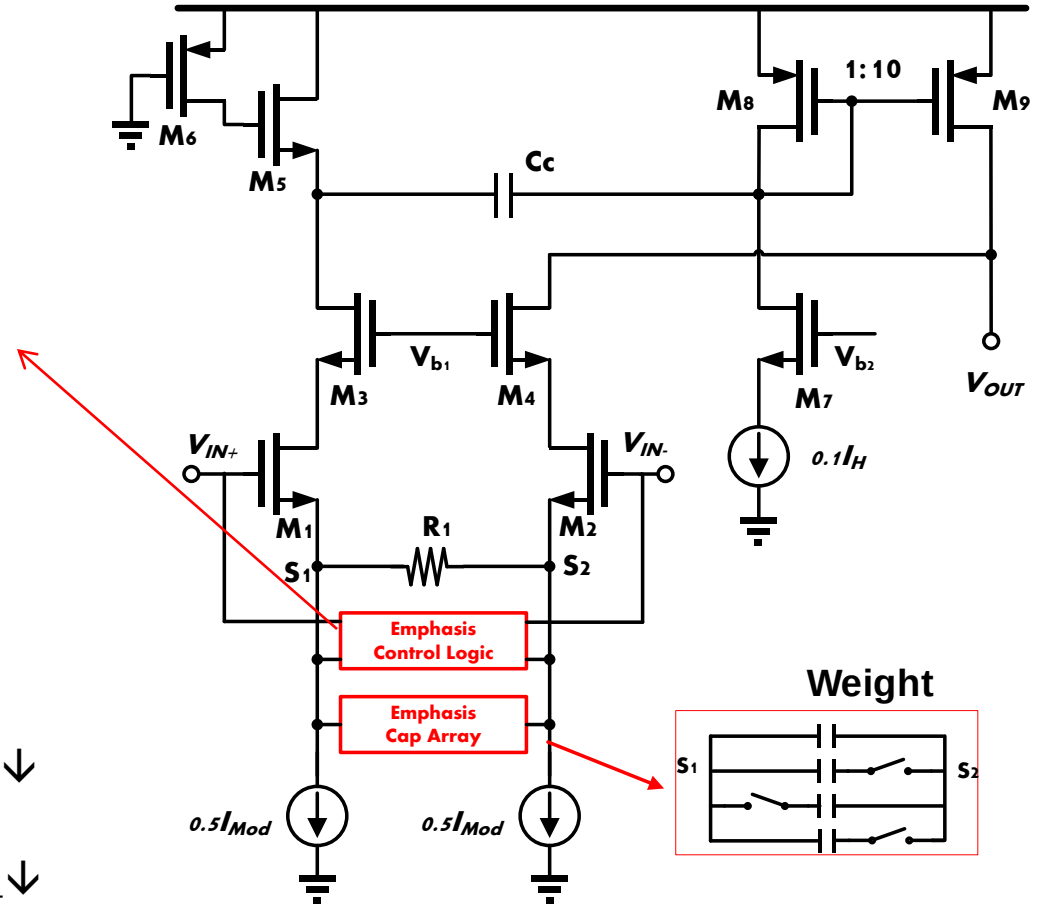


Switching Sequence for DAC Layout

- Layout to suppress gradient effects
  - Both X and Y directions
- Dummy
  - Dummy LSBs are added at the boundary
- Die size is 62 µm × 76 µm
- Top used metal is M2
- 7 complementary input bits
- Typical LSB current is 16 µA

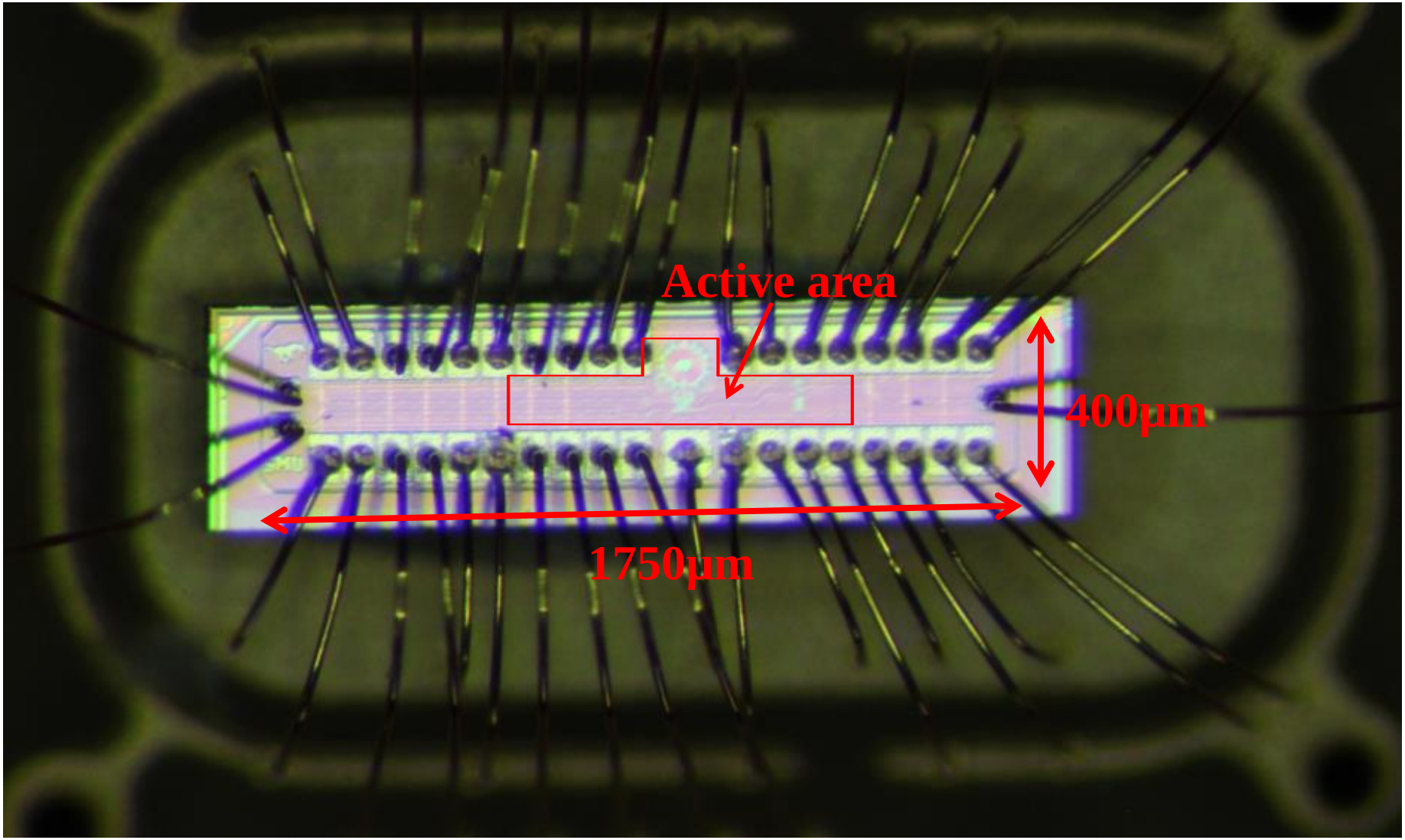
Configurable Rising/Falling Edge Pre-emphasis





- **Emphasis disable (empDis=1):**
  - A&B on and S_1=S_2 @ any time
- **Falling-edge emphasis(FallEmpOn=1):**
  - C&B on and S_1=S_2 only @ V_{IN-}↑ and V_{IN+}↓
- **Rising-edge emphasis(RiseEmpOn=1):**
  - D&B on and S_1=S_2 only @ V_{IN+}↑ and V_{IN-}↓
- **Both-edge emphasis(FallEmpOn=1/RiseEmpOn=1):**
  - D&B/C&B on and S_1=S_2 only @ V_{IN+}↑ ↓ and V_{IN-}↓ ↑

GBLD10+ Die Photo



GBLD10+ with VCSEL