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GBLD10+: A Compact Low-power 10 Gb/s VCSEL Driver IC

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We report the design and implementation of a low-power and radiation-tolerant 10 Gb/s VCSEL Driver (GBLD10+) for High Energy Physics (HEP) applications. With new circuit techniques, the single-channel driver consumes 40 mW and occupies a compact size of 380 µm × 1730 µm including the PADs. These features allow multiple of driver ICs to be assembled side by side in a compact package, with each one directly wire bonded to one diode in a VCSEL array. This makes the GBLD10+ a suitable candidate for the Versatile Link which offers the flexibility in configuring multiple transmitters and receivers.

Summary

Low-power, high-speed and radiation-tolerant Gigabit data links are needed for data transmission in High-Energy Physics (HEP) applications. Last year we reported and demonstrated a 10 Gb/s laser driver IC (GBLD10) implemented in 130 nm standard CMOS technology. It employed a distributed-amplifier (DA) technique to boost the speed and consumes 80 mW and occupies a die size of 2 mm × 2 mm with pads. In this work, we present a new 10 Gb/s VCSEL driver (GBLD10+) with much lower power consumption and more compact dimension, making the circuit suitable to drive a VCSEL array. The GBLD10+ IC consists of a high-speed limiting amplifier (LA) and an output driver with pre-emphasis control. To fit the design in a compact silicon area, the LA employs a new technique, which features a two-stage differential amplifier but with only one compact peaking inductor (130 µm × 130 µm) shared between the two stages, boosting the driver speed without consuming much area as it would require in a conventional inductive-peaking LA. The output driver utilizes a new area-efficient feedforward approach to boost the speed. Moreover, to accommodate different laser load effects, an edge-dependent pre-emphasis approach is proposed and implemented with three configurations –rising-edge pre-emphasis, falling-edge pre-emphasis and both-edge pre-emphasis. Two on-chip 7-bit DACs are used to program the modulation and bias currents with a current resolution of 0.16 mA. A radiation-hard and single-event immune I2C digital circuit is designed to control the IC operation. The single-channel GBLD10+ consumes a power of 40 mW and has a die size of 380 µm × 1730 µm including the PADs. These features allow multiple of such driver ICs to be assembled side by side in a compact package, with each one directly wire bonded to one diode in a VCSEL array. The GBLD10+ prototype chip design has been submitted for fabrication in May, 2015. The chip measurement will be carried out in the summer of 2015 and the measurement results will be presented at the TWEPP conference.

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