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Towards a 65nm Pixel Readout Chip for ATLAS and CMS High Luminosity Upgrades

H. Krüger on behalf of the RD53 collaboration

TWEPP 2015, 28 Sep – 2 Oct, Lisbon

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Outline

- Scope of RD53
- Status of working groups
  - Radiation Tolerance
  - IP Building Blocks
  - Analog Design
  - IO Interface
  - Simulation/Verification
  - Top Level Integration
- Outlook

RD53 in a Nutshell

- R&D program focused on the development of pixel chips for ATLAS/CMS phase 2 upgrades and LCD vertex detector (established in 2013)
- 20 institutes, ~23 FTE (2015)
- Requirements for ATLAS/CMS:
  - Small pixels: 50µm x 50µm
  - Large chips: ~2cm x 2cm (~10^9 transistors)
  - High hit rates: 2-3 GHz/cm^2
  - Radiation dose: 1 Grad, $2 \cdot 10^{16}$ n_{eq}/cm^2
  - Trigger: up to 1MHz, ~12µs latency
  - Low power, low mass
- Technology: 65nm CMOS
- Full scale demonstrator pixel chip by 2016

Working groups

- Radiation Tolerance
- Analog Design
- IP Building Blocks
- Simulation/Verification
- Top Level Integration
- IO Interface

www.cern.ch/RD53/

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RD53 Institutes

- INFN Bari and Politecnico di Bari
- University of Bonn
- CERN
- Aix Marseille Universite, CNRS/IN2P3, CPPM (plus LPCS. LAPP)
- Fermi National Accelerator Laboratory
- Lawrence Berkeley National Laboratory
- Laboratoire de Physique Nucléaire et de Hautes Energies, Paris
- NIKHEF
- University of New Mexico
- INFN Milano and University of Milano
- INFN Padova and University of Padova
- INFN Pavia, University of Pavia and University of Bergamo
- INFN Pisa and University of Pisa
- INFN Perugia and University of Perugia
- Institute of Physicsand Czech Technical University
- Paul Scherrer institute
- Rutherford Appleton Laboratory
- University of California Santa Cruz
- INFN Torino and University of Torino
- University of Sevilla and Instituto de Fisica de Cantabria

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Pixel Chip Generations

Generation	Current FEI3, PSI46	Phase 1 FEI4, PSI46DIG	Phase 2
Pixel size	100x150um^2 (CMS) 50x400um^2 (ATLAS)	100x150um^2 (CMS) 50x250um^2 (ATLAS)	50 x 50 µm^2 (or area equivalent)
Sensor	2D, ~300um	2D+3D (ATLAS) 2D (CMS)	2D, 3D, Diamond, MAPS ?
Chip size	7.5x10.5mm^2 (ATLAS) 8x10mm^2 (CMS)	20x20mm^2 (ATLAS) 8x10mm^2 (CMS)	**> 20 x 20mm^2**
Transistors	1.3M (CMS) 3.5M (ATLAS)	87M (ATLAS)	500M – 1G
Hit rate	**100MHz/cm^2**	**400MHz/cm^2**	**2(3) GHz/cm^2**
Hit memory per chip	0.1Mb	1Mb	~16Mb
Trigger rate	100kHz	100KHz	500kHz – 1MHz
Trigger latency	2.5us (ATLAS) 3.2us (CMS)	2.5us (ATLAS) 3.2us (CMS)	12.5 – 20µs
Readout rate	40Mb/s	320Mb/s	**1-4Gb/s**
Radiation	**100Mrad**	**200Mrad**	**1Grad**
Technology	250nm	130nm (ATLAS) 250 nm (CMS)	**65nm**
Architecture	Digital (ATLAS) Analog (CMS)	Digital (ATLAS) Analog (CMS)	Digital
Buffer location	EOC	Pixel (ATLAS) EOC (CMS)	Pixel
Power	~1/4 W/cm^2	~1/4 W/cm^2	**½ - 1 W/cm^2**

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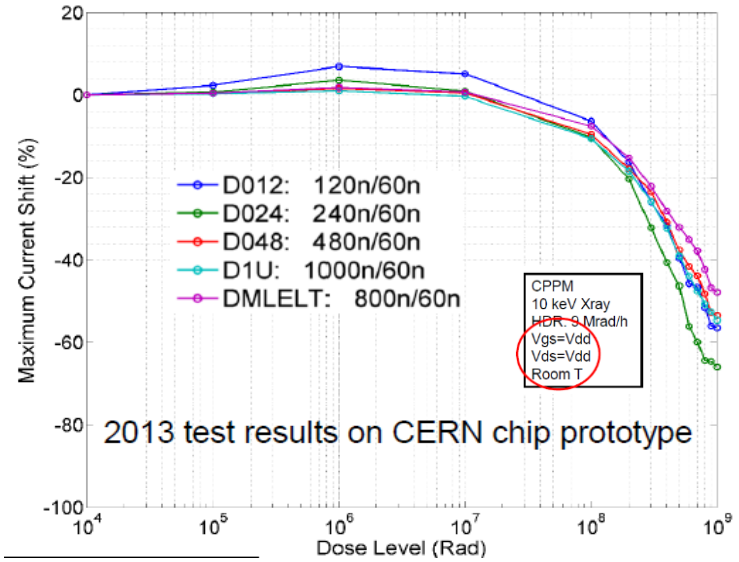
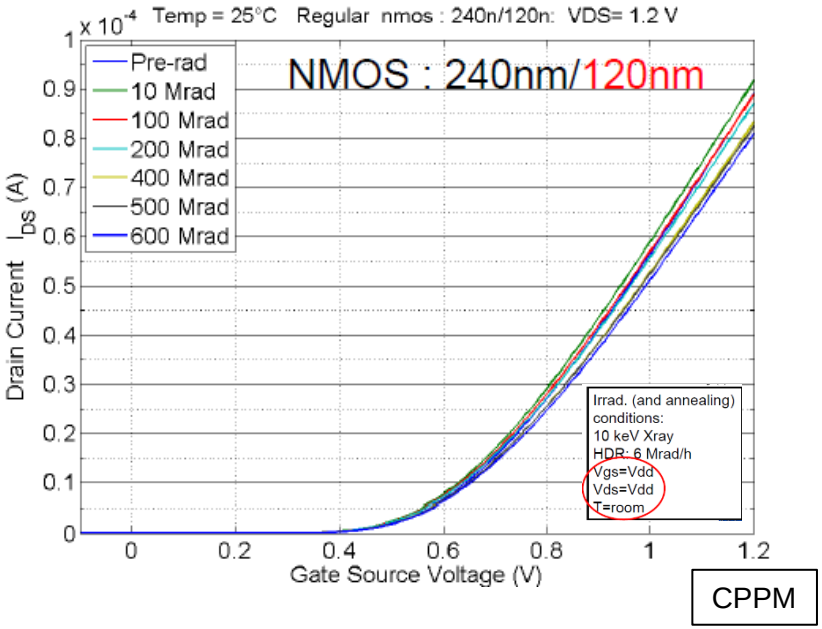
Radiation Tolerance Characterization

Radiation Tolerance of NMOS Transistors

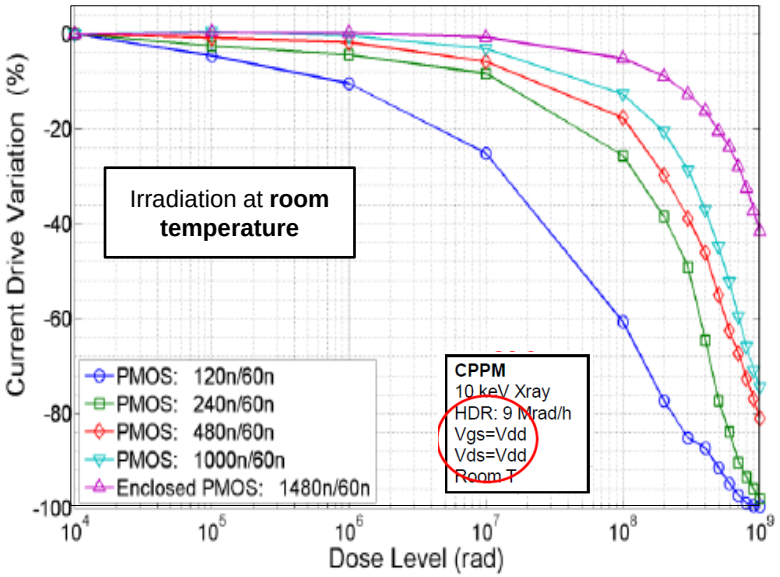


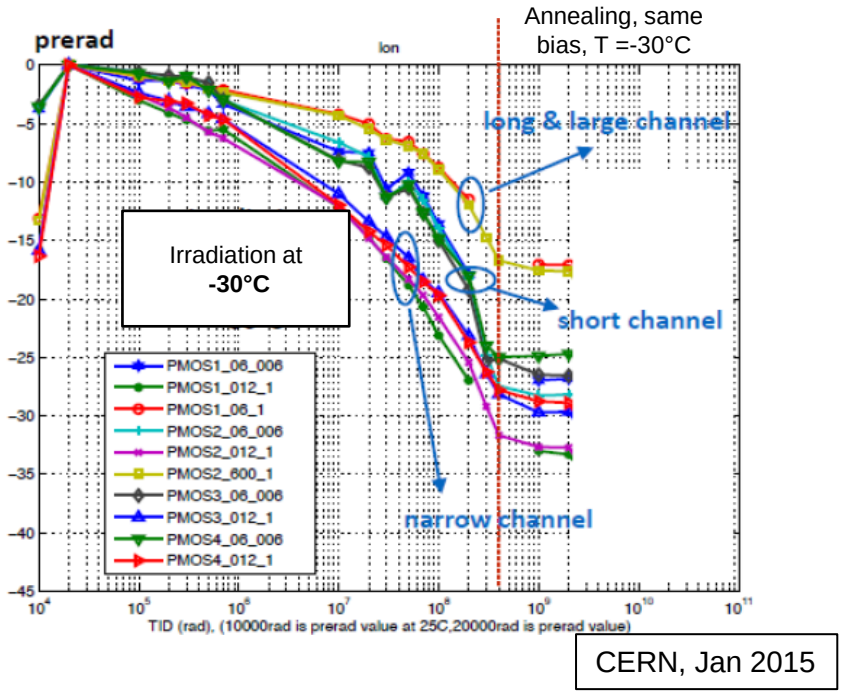


CPPM

- **Short channel devices (**L_{MIN} = 60nm) show **40% - 55% reduction of** I_{ON}
- **Only 10% for L = 120nm** after TID = 600 Mrad (compared to 46% for 240n/60n)
- Little effect of channel width (**W_{MIN} devices ok**)
- Low temperature (-15°C to -20°C) further reduces I_{ON} degradation
- Bias conditions are important, moderate effect of annealing
- **Moderate** increase of **leakage** current

Radiation Tolerance of PMOS Transistors





CERN, Jan 2015

- **Min. size PMOS are basically off at TID > 500 Mrad**
- **Strong dependence** of I_{ON} degradation on **channel width** and **bias conditions**, moderate effect on channel length
- **Low temperature reduces I_{ON} degradation**

Radiation Tolerance – Summary

- Lot of activity (CERN, CPPM, FNAL, Padova), characterization of sensitivity to various parameters (channel geometry, MOS type, temperature, bias, annealing)

➔ Recommendations (up to **500 Mrad**)

- **Cold** operation < -15°C
- For analog designs:
  - NMOS: **L ≥ 120nm**, any W Ok
  - PMOS: **W ≥ 300nm**, L ≥ 120nm

- Work in progress: Modelling of evolution of transistor parameters under radiation
  - Extraction of BSIM parameters for a new “radiation” corner
  - For **digital designs**: Timing characterization of standard digital library after radiation damage

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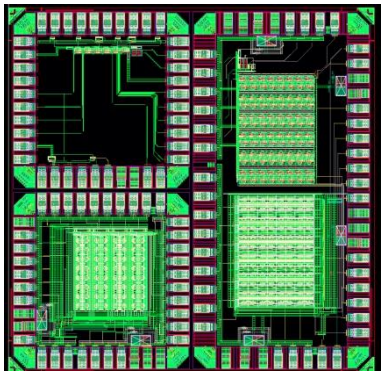
IP Development

IP Block Development

- Make IP blocks required to build pixel chips
- About 30 IP's defined and assigned to groups
- Defining how to make IPs ready for integration into digital design flow
- Common IP/design repository
- Prototyping/test of IP blocks ongoing
- IP blocks ready 2015/2016

Group	Bonn	CERN	CPPM	NIKHEF	Bari	Pav/ Berg	(Milano)	Padova	Pisa	Torino	LBNL	LPNHE	RAL	Santa Cruz	(Prague)
ANALOG:															
Temperature sensor.			O			(P)				(P)					(P)
Radiation sensor			(P)			(P)				O ?					(P)
HV leakage current sensor.			O							(P)					(P)
Band gap reference		O	O	(P)		O							(P)		
Self-biased Rail to Rail analog buffer	(P)		(P)	(P)									O		(P)
MIXED SIGNAL															
8 – 12 bit biasing DAC		(P)			O										(P)
10 - 12 bit slow ADC for monitoring		O	O		O										
PLL for clock multiplication	O	(P)		(P)				(P)	(P)	(P)			(P)	(P)	
High speed serializer (~Gbit/s)	O	(P)		(P)					(P)				(P)	(P)	
(Voltage controlled Oscillator)				(P)				O	(P)	(P)					
Clock recovery and jiter filter	O	(P)							(P)				(P)		
Programmable delay	O	(P)							(P)				(P)		
DIGITAL															
SRAM for pixel region	(P)	(P)					O							(P)	
SRAM/FIFO for EOC.	(P)	(P)					(P)		(P)					O	
EPROM/EFUSE	(P)	O	(P)												
DICE storage cell / config reg	(P)		O				(P)		(P)					(P)	
LP Clock driver/receiver	(P)					O							(P)		
(Dedicated rad hard digital library)	(P)	(P)	(P)						O			(P)	(P)		
(compact mini digital library for pixels)	(P)	(P)	(P)						O			(P)	(P)		
IO: Interface															
Basic IO cells for radiation	(P)	O													
Low speed SLVS driver (<100MHz)	(P)	(P)				O			(P)	(P)					(P)
High speed SLVS driver (~1Gbits/s)	(P)	(P)				O			(P)	(P)					(P)
SLVS receiver	(P)	(P)				O			(P)						(P)
1Gbits/s drv/rec cable equalizer															
C4 and wire bond pads	(P)	O													
(IO pad for TSV)	O		(P)									(P)		(P)	
Analog Rail to Rail output buffer	O		(P)									(P)		(P)	
Analog input pad	O											(P)			
POWER															
LDO(s)		(P)	(P)	O					(P)	(P)			(P)		
Switched capacitor DC/DC		(P)									O				(P)
Shunt regulator for serial powering				O											
Power-on reset															
Power pads with appropriate ESD	(P)	O													
SOFT IP:															
Control and command interface		(P)			(P)				O			(P)			
Readout interface (E-link ?)		(P)			(P)				O			(P)			

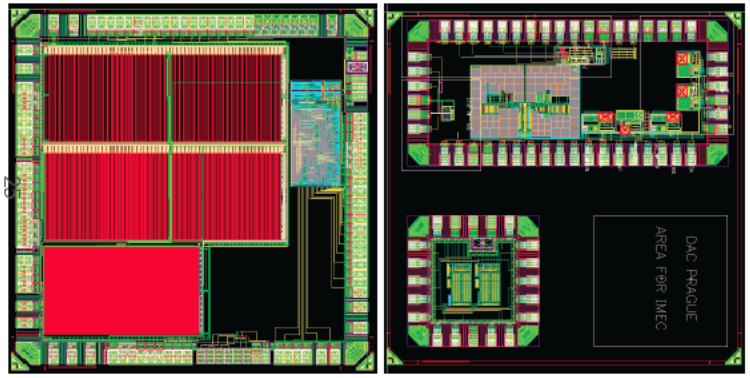
Example of IP Prototyping – CHIPIX Test Chips



INFN Torino, Pavia, Pisa

CHIPIX_1 (submitted Oct. 2014)

- Very Front-end test chip
  - Test Structures (CSA + Disc)
  - Pixel matrix (8x8) with analog readout
  - Pixel matrix (12x16) with simple digital readout
- IP blocks
  (various implementations per type)
  - Bandgap DAC
  - DICE memory cells
  - SER/DES



Torino, Pavia, Pisa, CERN, CPPM, Bari, Prague

CHIPIX_2 (submitted May 2015)

- Second version of VFE matrices (8x8)
- IP blocks
  - SLVDS
  - SERDES
  - ADC
  - POR

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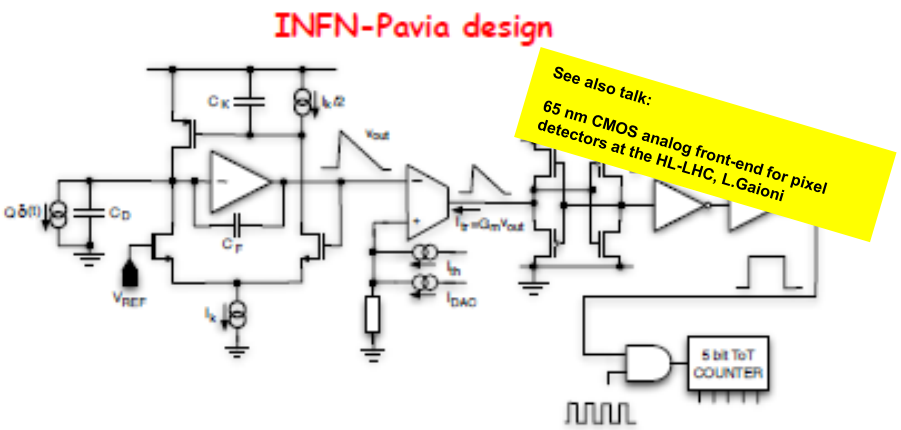
Analog Front-end Design

Analog Front-end Design

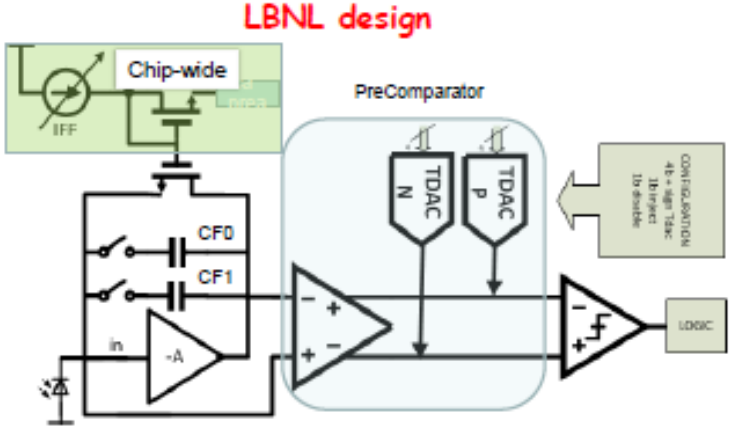
- Analog specs (preliminary):
  - Supply current per pixel: **4µA** (analog only)
  - Input capacitance: **<100fF** (200fF for edge pixels)
  - Leakage current comp.: <10nA (20nA)
  - Min. threshold: **600 e^-** (1200e^- in-time threshold) for 50fF load
    - Total noise < 130 e^- (including threshold dispersion and fluctuation)
  - Charge measurement resolution: ≥ 4 bit
  - Avg. hit rate per pixel: 75kHz (to allow < 1% hit loss)
  - Noise occupancy < 10^{-6}

- Evaluation of different implementations
  - Different time-over-threshold charge measurement front-ends
  - Non-linear digitization
  - Synchronous FE (switched-reset and/or dynamic comparator)

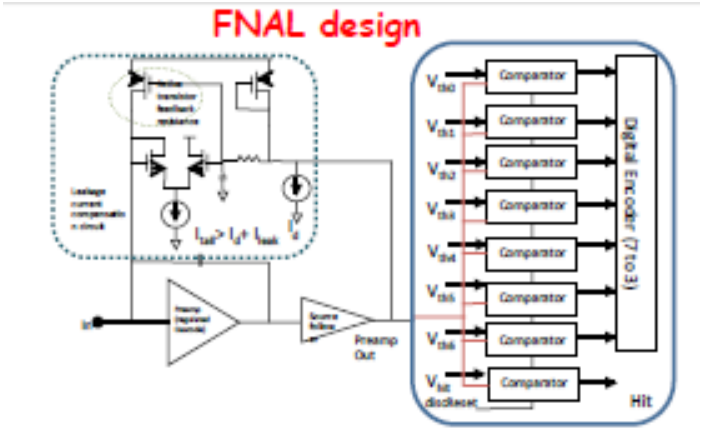
Analog Front-end Design



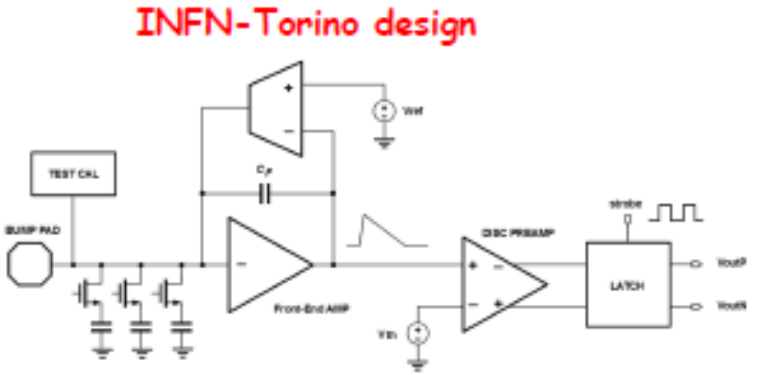
Single stage with current comparator and ToT counter



1 of 4 in quad “analog island” of FE65_P2



Synchronous: resets every bunch x-ing Flash ADC



Single stage with SAR-like ToT counter using synchronous comparator

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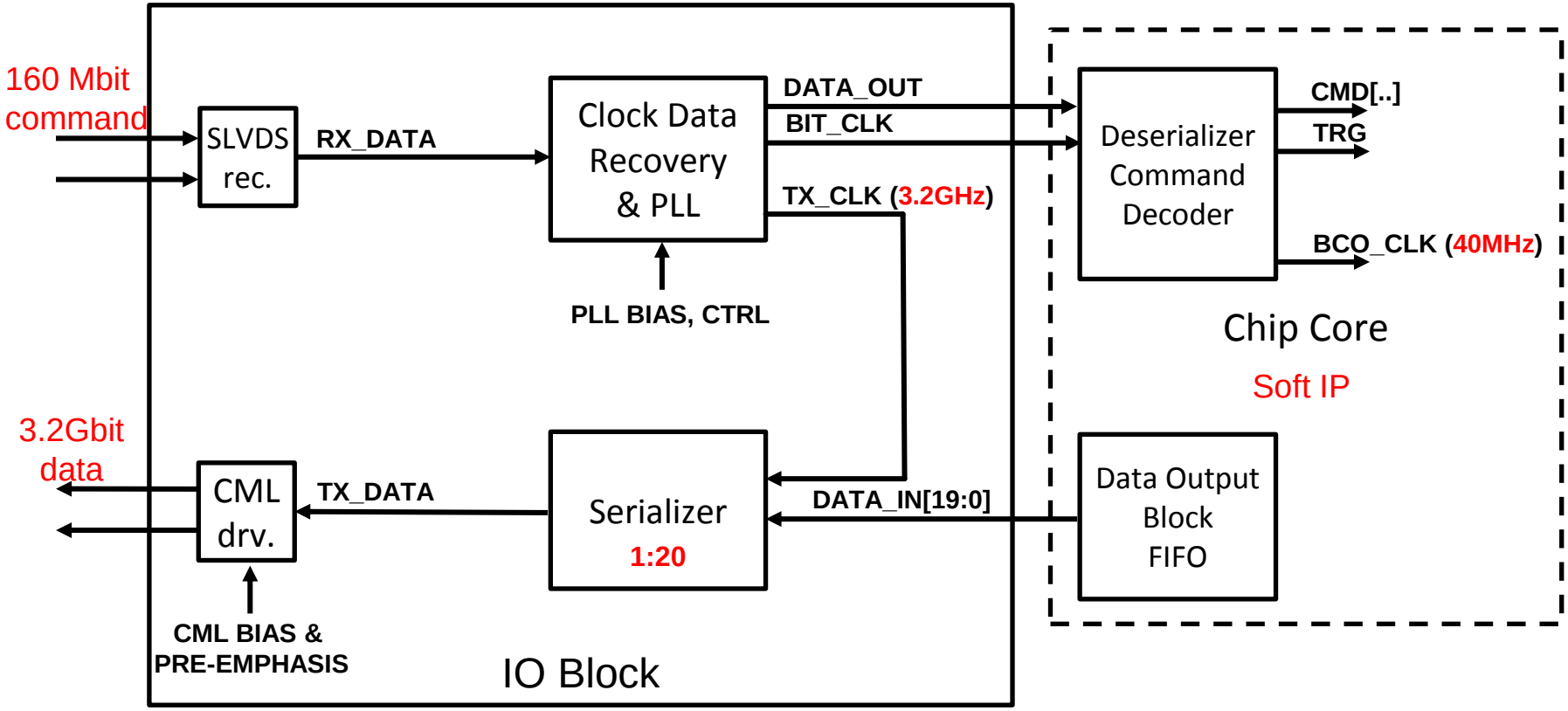
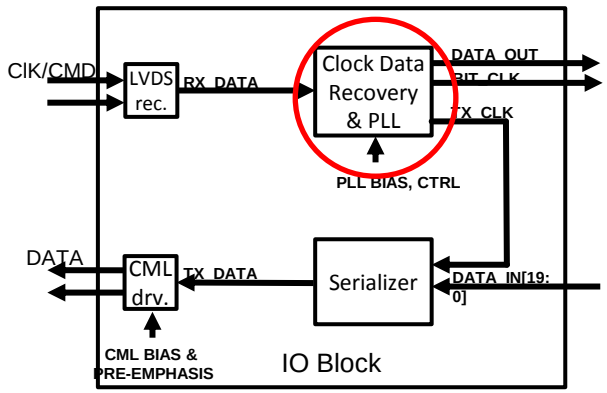
IO Interface

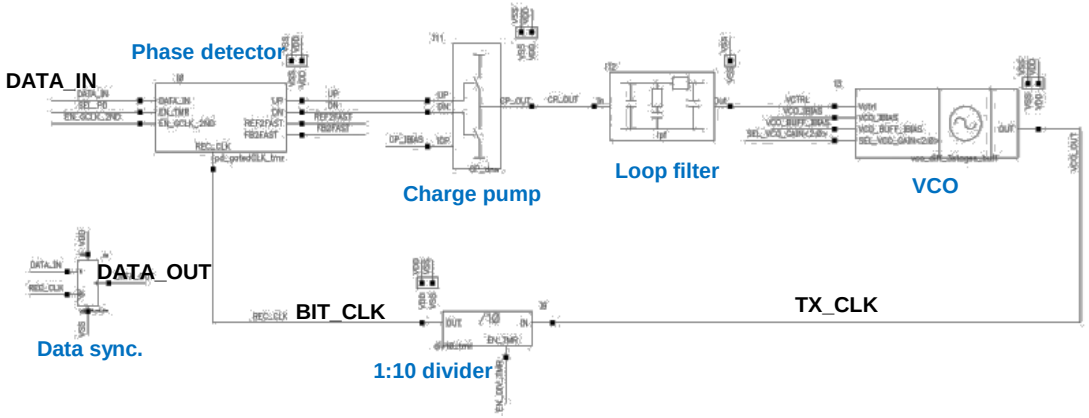
IO Interface

- Single input line: Decoding of clock, command and trigger data with CDR, custom 8b symbols, dc-balanced, fault tolerant (redundancy)
- High speed serial output link, dc-balanced (protocol tbd.)



CDR / PLL



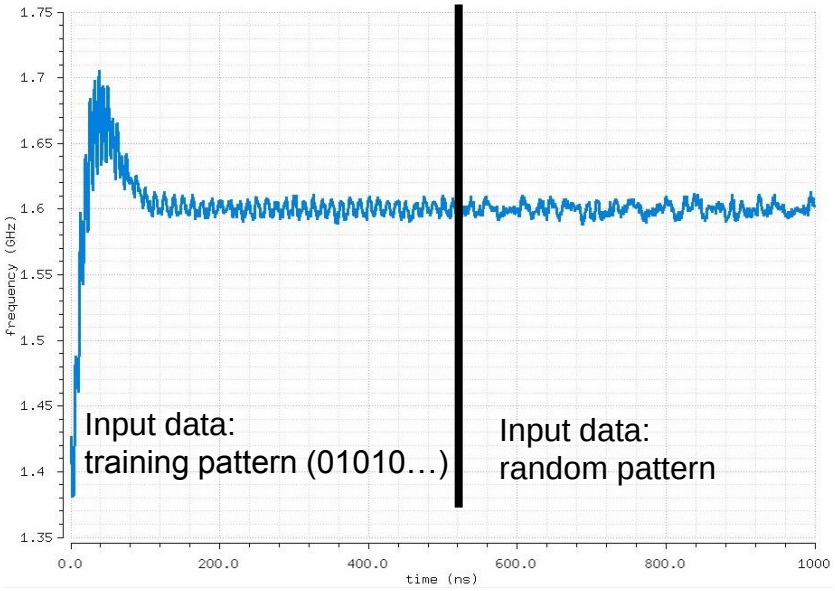


- Fixed input rate to 160 Mbps, maximum input symbol run-length < 5
- Phase detector and divider have few versions implemented:
  - Phase detector: 2 kinds (Hogge's and CLK-gating based) both in triplicated and non-triplicated forms
  - Divider: one non-triplicated and 2 triplicated versions
- Digital parts implemented with modified standard cells (W_pMOS≥500μm, W_nMOS ≥200μm, minimal L)
- Analog parts also avoid minimum sized transistors

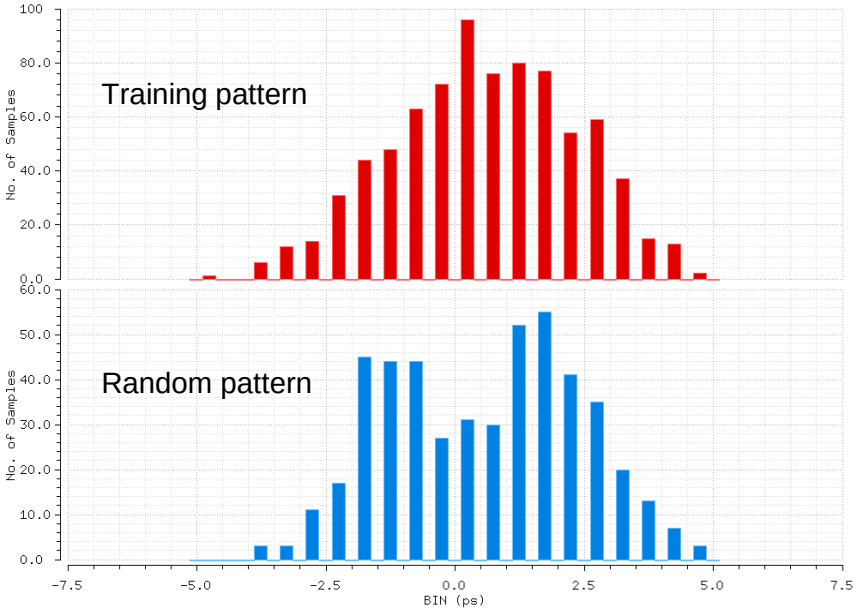
CDR/PLL Simulation

- Simulation was done using extracted view of most blocks, including thermal noise
- Reference frequency is the recovered clock from 160 Mbps input data, (LFSR-5 pseudo random data)
- Performance of 1.6GHz PLL:
  - Jitter (peak to peak): 10ps
  - Duty cycle: 49% (typical corner)
- Locking of CDR PLL aided with training pattern (010101…), < 200ns lock time

PLL Output Frequency vs. Time

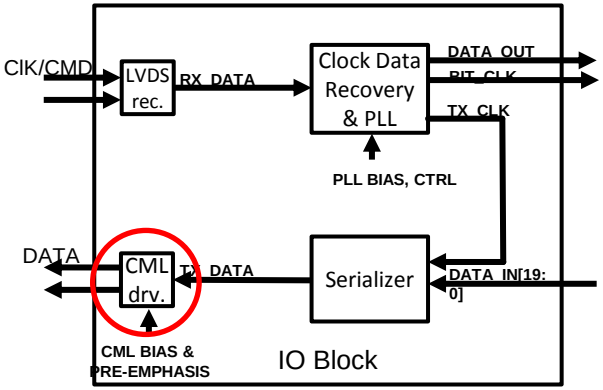


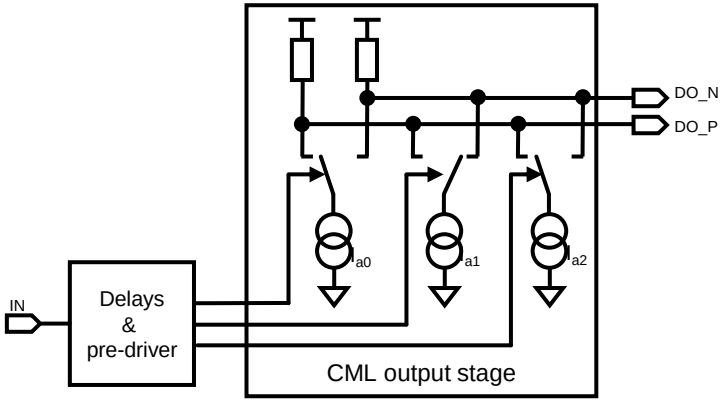
Phase Noise

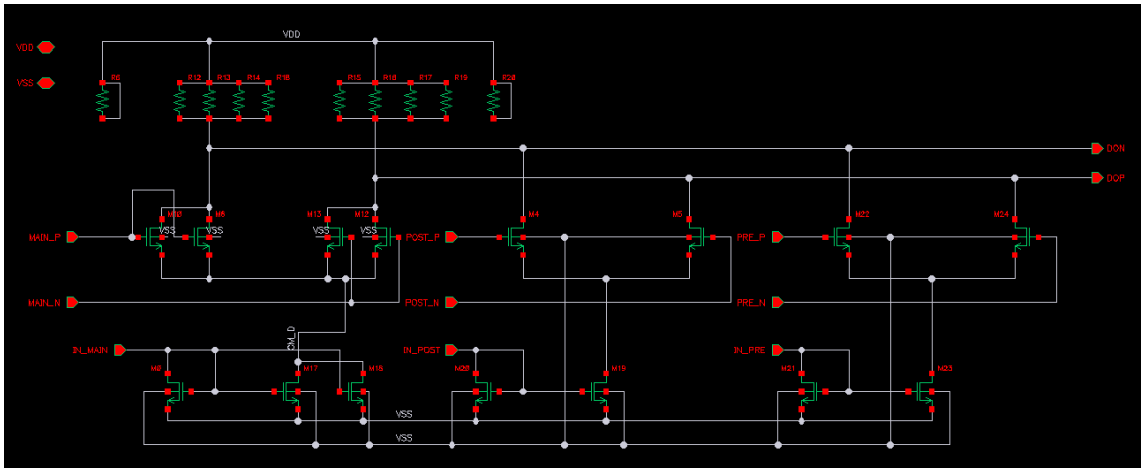


Driver Implementation

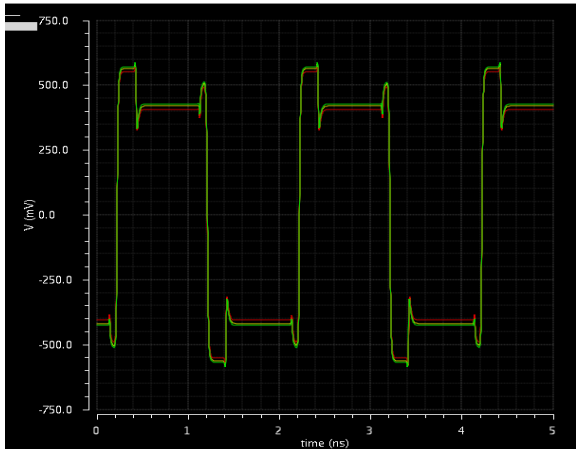
- **3 Gbps** (or higher) of hit data has to be transmitted over a **4 to 6 meters** of **low mass** cables ➔ Implementation of a 'Current mode logic' (CML) driver







CML output stage schematic with 3-tap pre-emphasis



Example of a transient simulation (driver output, no cable)

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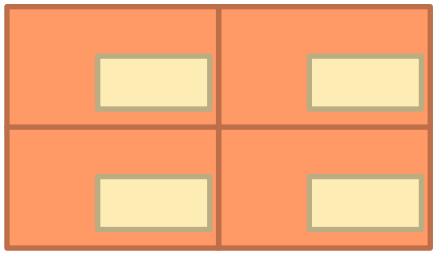
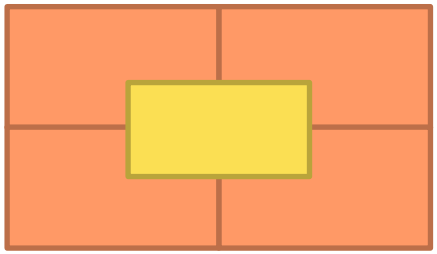
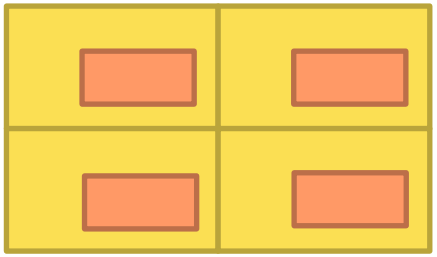
Top Level Integration

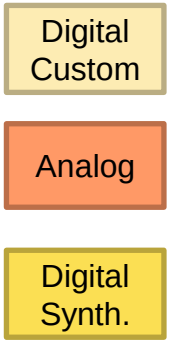
Top Level Integration

Evolution of pixel chip design flow concepts









Traditional full custom design

- Make one pixel
- Step and repeat identical copies
- Custom made digital
- Example: ATLAS FEI-3

More Recently

- Make few-pixel region
- Step and Repeat identical copies
- Synthesized digital
- Example: ATLAS FEI-4

New Approach (RD53)

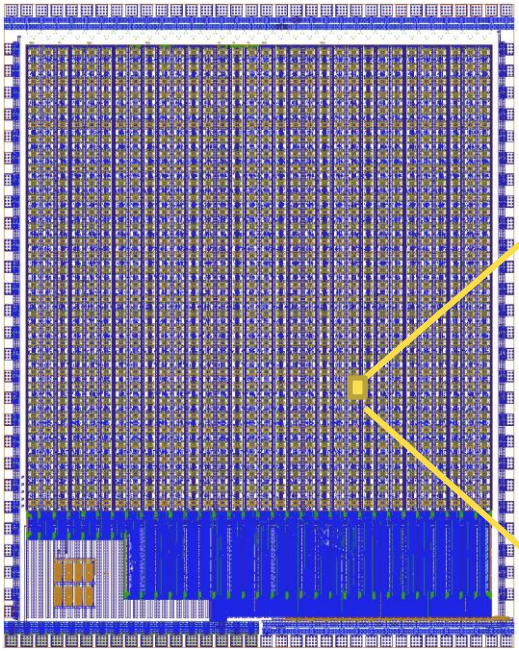
- Synthesized digital "core" containing a large number of analog pixels
- Example: FE65_P2

See poster: FE65_P2: Prototype Pixel Readout Chip in 65nm for HL-LHC Upgrades

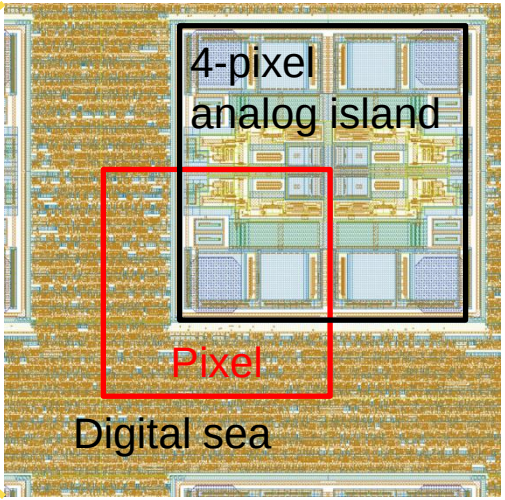
Top Level Integration

- Architecture and floor-planning concept
  - “Digital sea with analog islands”
  - Pre-routed power and global signal distribution
  - Analog-digital isolation with separate deep n-wells
  - Want low, constant power

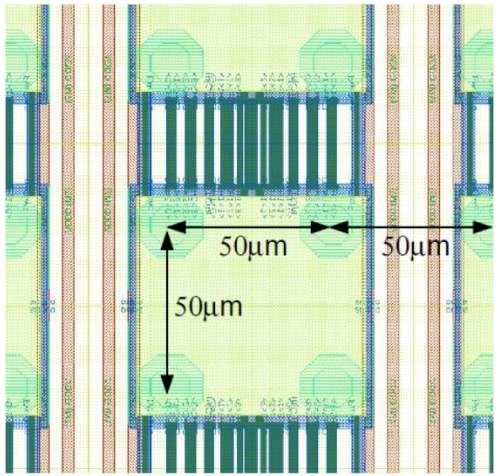
See poster:
FE65_P2: Prototype Pixel Readout Chip in 65nm for HL-LHC Upgrades



FE65_P2 prototype chip layout



Pixel region with digital sea and analog islands



Pre-routed bias and power busses with placed bump pads

Simulation & Verification

See posters:
FE65_P2: Prototype Pixel Readout Chip in 65nm for HL-LHC Upgrades

And

Simulation of Digital Pixel Readout Chip Architectures with the RD53 SystemVerilog-UVM Verification Environment Using Monte Carlo Physics Data

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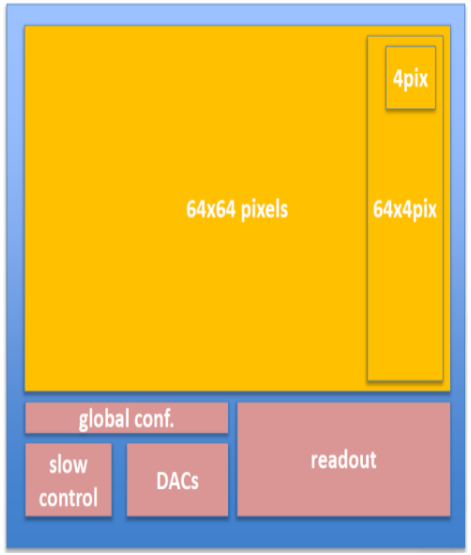
Prototype Matrix Chips

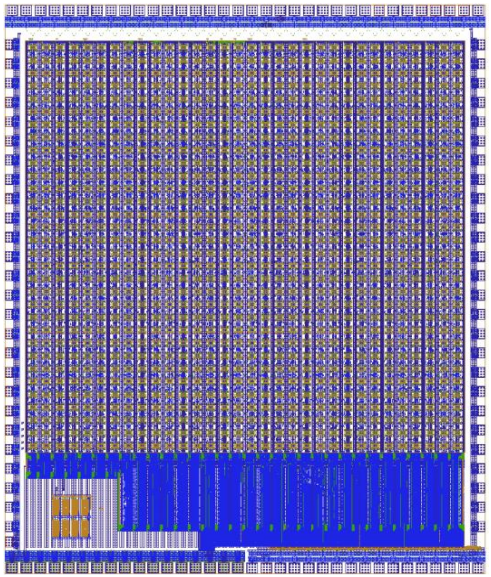
Prototype Chip FE65_P2

- 64 x 64 pixel matrix, (Bonn, LBNL)
- Validation of
  - “Analog islands on digital” sea concept
  - Digital top level design flow
  - Mixed signal isolation (both analog and digital regions in separate deep n-wells)
  - Performance of the 50µm x 50µm pixels, including the bump bonding to matching sensors
  - Senor R&D
- **MPW run** submission end of 2015
  - Requires **single chip** bump bonding (low volume only)

See poster:
FE65_P2: Prototype Pixel Readout Chip in 65nm for HL-LHC Upgrades



Floorplan



Layout after P&R

FE65_P2 Prototype chip

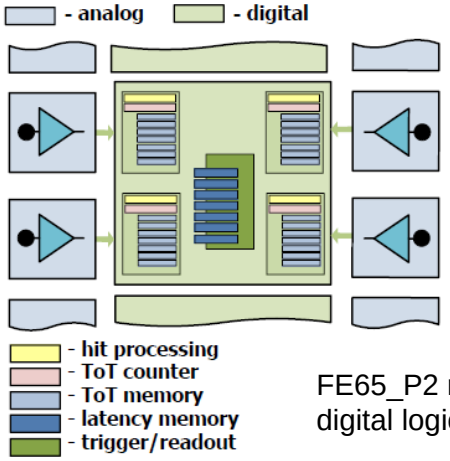
Prototype Chip FE65_P2 – Digital Core

- Code adapted from FE-I4,
  - 4 pixels per region
  - 4-bit ToT counting per pixel
- Optimized for higher hit rates
  - 7 Latency memories (stores up to 7 hit arrival times for the region)
  - Using latches to store distributed counter value, instead of individual counters as in FE-I4

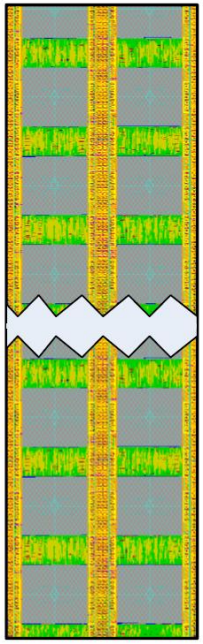
  ➔ Data loss < 1% at 10us latency with 50KHz/pixel hit rate

- Simulation of synthesized 64 x 4 pixel core
  - Density 85%
  - Digital power: 5.5µW per pixel (2GHz/cm^2 hit rate, 1MHz trigger rate)

See poster:
FE65_P2: Prototype Pixel Readout Chip in 65nm for HL-LHC Upgrades



FE65_P2 region digital logic



FE65_P2 synthesized 64 x 4 pixel core

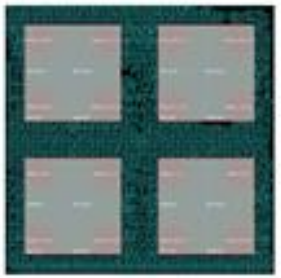
Prototype chip: CHIPIX65

- 64x64 matrix of 50x50 um^2 pixel
- Independent development from FE-I4, FE65_P2
- Choice of Pixel Region: 4x4
  - Development of new digital architecture with low hit-loss, low-buffer location
  - Using 4-pixel analog island in deep-n-well
  - Signal digitisation : 5-bit, ToT
- Analog Front End designs
  - INFN Torino (synchronous discriminator / NO-trim DAC);
  - INFN-Pavia (asynchronous) - See L.Gaioni on Tuesday
- Implementation of tested RD53 IP-block:
  - BandGap, DAC, sLVDS TX/RX, ADC, SER (more if available)
- Use of CERN RadTol I/O pads
- Design methodology based on digital top level hierarchical flow
- Core design team based on CHIPIX65 / INFN groups (To, Ba, Bg/Pv, Mi, Pd, Pg, Pi)
- Multi-Project run Submission: Q1/2016

See E.Monteil Wednesday

See L.Gaioni Tuesday

See F.Loddo Tuesday



4x4 PR, with 4 Analog-Islands

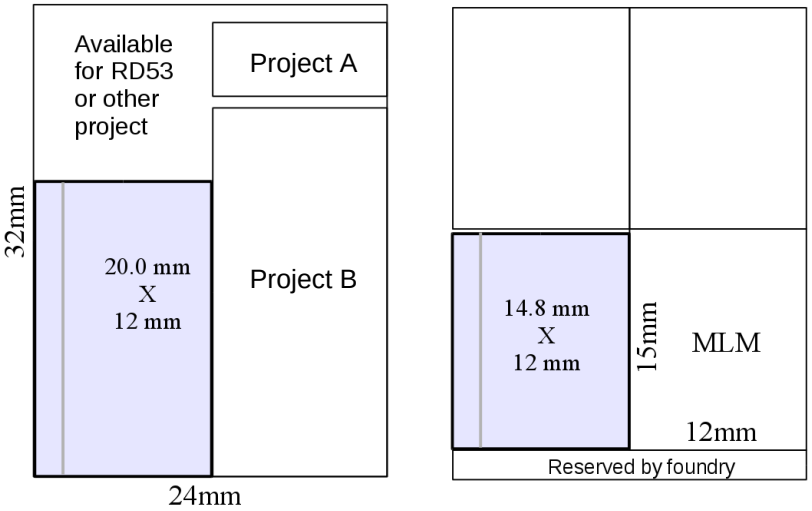
chip - layout exercise

RD53 Test Chips

Chip	Submitted	Area	Institutes	Contents
Proto65_V1	?? (pre- RD53)	??	LBNL, CPPM	Analog pixel front-ends, test structures
Proto65	June 2014	2 x 2 mm^2	CPPM	Test structure, ADC, BG, Buffer, Tsense, SEU latches
Chipix65_1	Oct. 2014	4 x 4 mm^2	INFN + Prague	Pixel front-ends, BG, SRAM, SERDES
FE_65_P2	End of 2015 (planned)	15 mm^2	Bonn, LBNL	Core layout demonstrator
Chipix65_2	May 2015	1-2 times 2 x 2 mm^2	INFN	Pixel front-ends, IP blocks
Proto65_V2	June 2015	2 x 2 mm^2	CPPM	IP Blocks
Chipix65_3	End of 2015 (planned)	MPW ~12 mm^2	INFN	Tbd.
CLICpix, bis	2015/2016 (planned)	MPW ~12 mm^2	CERN	CLIC compatible pixel chip, 128 x 128 pixels
Chipix65_4	Feb 2016 (planned)	1-2 times 2 x 2 mm^2	INFN	IP blocks
RD53_A	2016 (planned)	MLM (tbd)	all	RD53 full scale demonstrator pixel chip

Next Step: Demonstrator Chip RD53_A

- Large format chip (>1cm^2), full scale demonstrator
  - **Available in full wafers**
- Demonstration of essential features
  - 50 x 50µm^2 (or area equivalent) pixels, high rate, low threshold, high speed readout
  - 500Mrad radiation tolerance (to be tested also at higher dose)
  - SEU tolerance
  - Power management, serial powering
  - Yield
- Not a production chip
  - Multiple pixel variants (non-uniform array)
  - Not ultimate performance data output drivers data compression not required, no high volume test features, etc.
  - Necessary for RD53 and for sensor and bump bonding R&D efforts
- To be submitted in 2016



Reticle for **shared engineering run**

Multi-layer mask (MLM4) reticle

RD53_A production options

Conclusion & Outlook

- RD53 working group progress
  - **Recommendations** and design aides to improve the **radiation tolerance**
  - Definition of the IO interface converging
  - Prototyping and characterization of various **IP blocks** (incl. new analog FE concepts)
  - First implementation of a matrix prototype chip (FE65_P2) using **digital design flow** and a **UVM based verification** environment

- Outlook
  - Full characterization of custom IP blocks ➔ shared IP library
  - Prototype matrix chip submissions (FE65_P2, CHIPIX65) end of 2015/beginning of 2016
  - “Full scale” matrix chip demonstrator (RD53_A) by end of 2016

TWEPP 2015 contributions related to 65nm CMOS developments

- Design of a 10-bit segmented current-steering Digital-to-Analog Converter in CMOS 65nm technology for the bias of new generation readout chips in high radiation environment, Flavio LODDO (INFN-BARI)
- Design and results of a 65 nm digital readout Macro Pixel ASIC (MPA) prototype with on-chip particle recognition for the Phase II CMS Outer Tracker upgrade, Davide CERESA (CERN)
- FE65_P2: Prototype Pixel Readout Chip in 65nm for HL-LHC Upgrades, Tomasz HEMPEREK (University of Bonn)
- Towards a 65nm Pixel Readout Chip for ATLAS and CMS High Luminosity Upgrades, Hans KRÜGER (University of Bonn)
- A low jitter PLL frequency synthesizer for high resolution TDCs in 65nm CMOS technology, Jeffrey PRINZIE (KU Leuven)
- Library Characterization Techniques for 65nm and 130nm Technologies, Xavi LLOPART (CERN)
- TID Effects in 65nm Transistors: Summary of a Long Irradiation Study at the CERN X-rays Facility, Federico FACCIO (CERN)
- 65 nm CMOS analog front-end for pixel detectors at the HL-LHC, Luigi GAIONI (University of Bergamo)
- Pixel front-end with synchronous discriminator and fast charge measurement for the upgrades of HL-LHC experiments, Ennio MONTEIL (INFN Torino)
- Simulation of Digital Pixel Readout Chip Architectures with the RD53 SystemVerilog-UVM Verification Environment Using Monte Carlo Physics Data, Elia CONTI (CERN)

- Note: Not all talks related to RD53 (but most of them), no claim to be a complete list

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Thank you!