Contribution ID: **233** Type: **Plenary**

Towards a 65nm Pixel Readout Chip for ATLAS and CMS High Luminosity Upgrades

Friday, 2 October 2015 09:45 (25 minutes)

For the Phase II Upgrade of both ATLAS and CMS experiments, a new pixel read-out chip needs to be developed to meet the requirements in terms of spatial resolution, data rate, and radiation tolerance. The RD53 research collaboration will develop a large area mixed signal ASIC in a 65nm CMOS technology. Special working groups focus on major design tasks like radiation tolerant design, top-level architecture, IP block development, analog front-end design etc. The status of the development tasks will be shown, which includes the design flow and read-out concept, and the development of specialized IP blocks.

Summary

For the Phase II Upgrade of both ATLS and CMS Experiments, a new generation of pixel read-out chips has to be developed to meet the requirements in terms of spatial resolution, data rate and radiation tolerance. Therefore an advanced deep submicron technology (65nm) has been chosen to increase circuit density and digital performance. To meet the technical challenges realizing a complex and large area mixed signal design, ATLAS and CMS (and CLICpix) have established a research collaboration (RD53) to focus their effort in using an advanced 65nm CMOS technology. In the scope of RD53 a general design concept is being developed and implemented. The pixel chip will have to process high hit rates (1-2GHz/cm^2), high trigger rates (1-2MHz), and a long trigger latency (˜10µs). In addition it will have to stand extreme radiations levels in terms of ionizing dose (>5 MGy) and particle fluence (> 10^{16}n$_{eq}$ /cm^2).

The pixel chip will be implemented following a digital design flow which will include full-custom analog cells. The full chip, including the pixel region and the chip's periphery will be synthesized with regions left for the analog islands, in particular for the analog front-ends and other full-custom blocks. This strategy has been developed to optimize power and bias signal distribution and to minimize coupling for achieving a low threshold.

The chip's digital interface will use only two differential links for the communication with the back-end electronics: One down-link will carry the command, configuration, and trigger information –including the bunch crossing timing. To achieve this, the FE chip will make use of a clock-data-recovery (CDR) circuit to separate the encoded data stream and to regenerate the timing information. The up-link will transfer the event data at up to 4 Gbps to a repeater or optical converter. Since only low mass cables can be used within the active sensor volume, the high speed data drivers have to be carefully designed to compensate the expected high frequency damping of the low mass cables.

The status of the current development will be shown, which includes the digital read-out concept and the development of specialized IP blocks for the digital interface of the chip.

Primary author: KRUEGER, Hans (University of Bonn)

Presenter: KRUEGER, Hans (University of Bonn)

Session Classification: Plenary