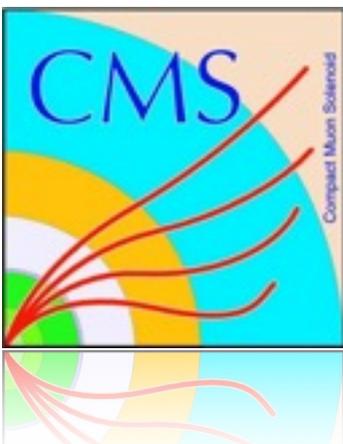
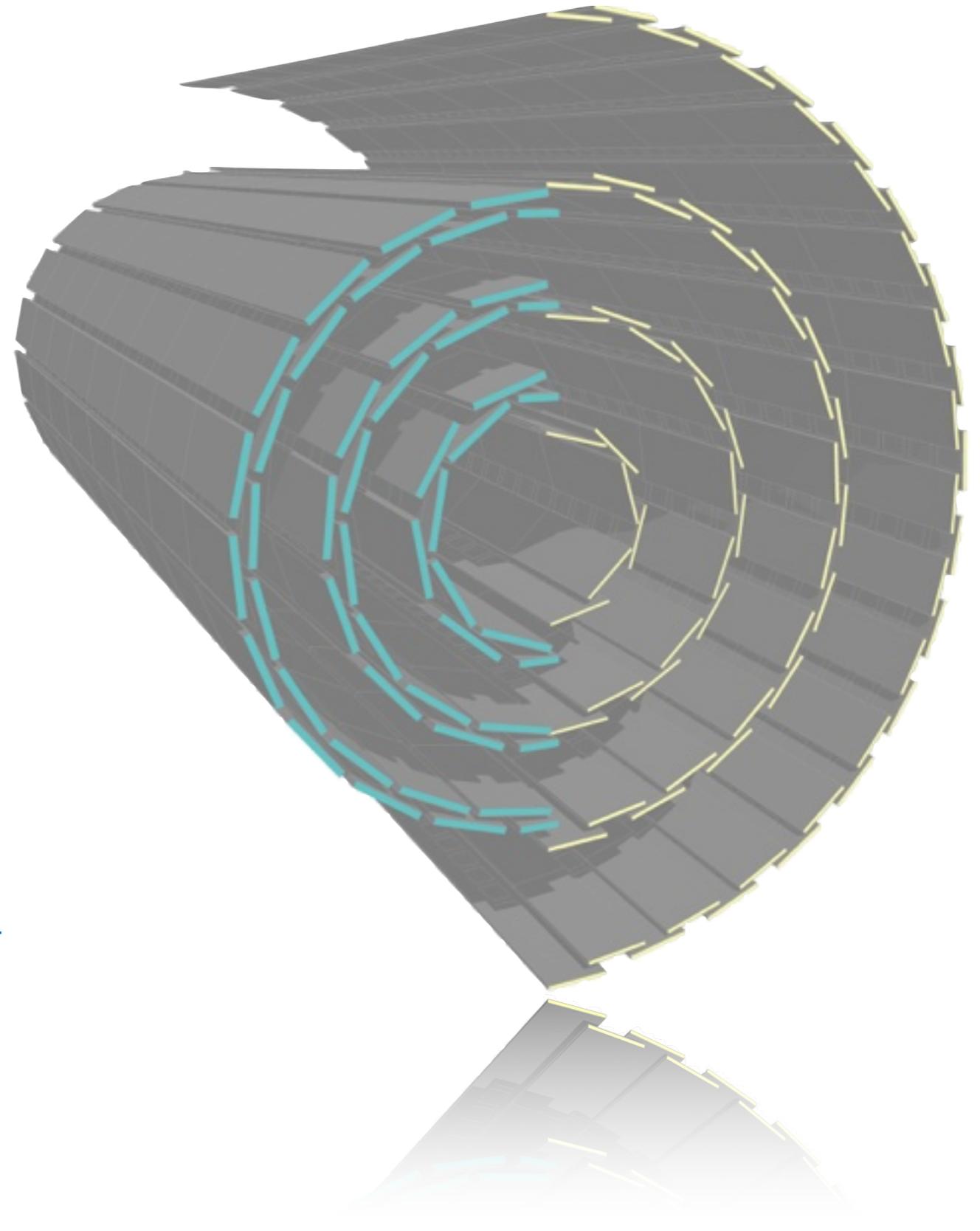


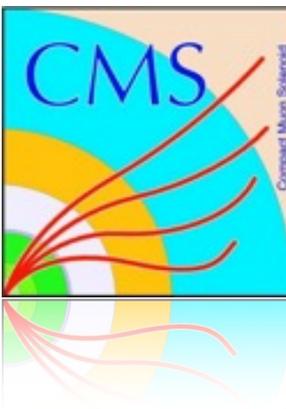
# Deployment of the CMS Tracker AMC (CTA) as Backend for the CMS Pixel Detector

G. Auzinger on Behalf of the  
CMS Pixel DAQ WG  
[georg.auzinger@cern.ch](mailto:georg.auzinger@cern.ch)



Topical Workshop on Electronics for  
Particle Physics,  
Lisbon, Sep. 28<sup>th</sup> - Oct. 2<sup>nd</sup> 2015

# Outline



## **1. Introduction**

- **The Phase1 Pixel Upgrade**
- **System Requirements**

## **2. CMS $\mu$ TCA System Architecture**

## **3. Ph1 Pixel FED**

## **4. FECs**

- **Tracker FEC**
- **Pixel FEC**

## **5. System Tests & Integration**

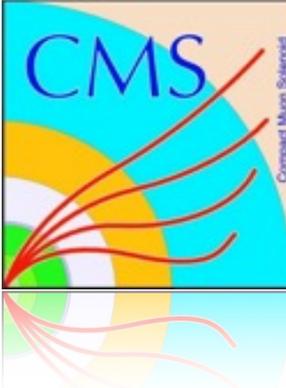
# Introduction: The CMS Phase 1 Pixel Upgrade

increase of **instantaneous luminosity** & **pile-up** during LHC Runs 2 & 3:

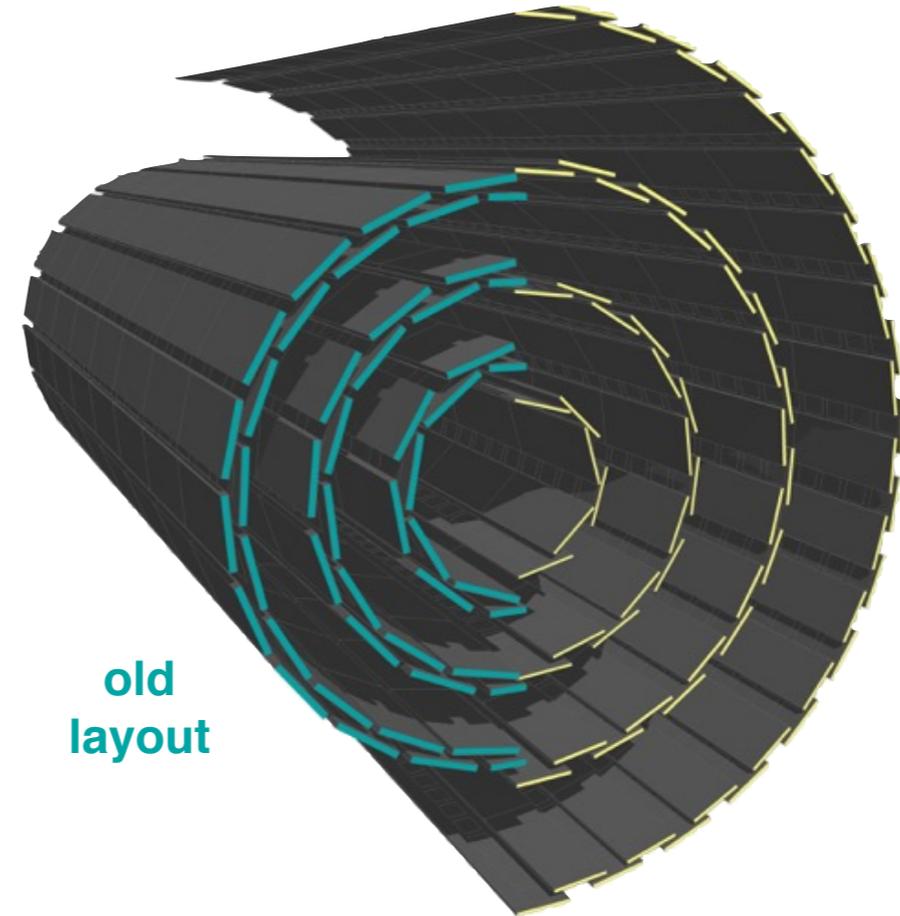
- much **higher track density** / higher occupancy in the pixel detector
- **higher data rates**

-> **CMS planning replacement of pixel detector during extended YETS 2016/2017:**

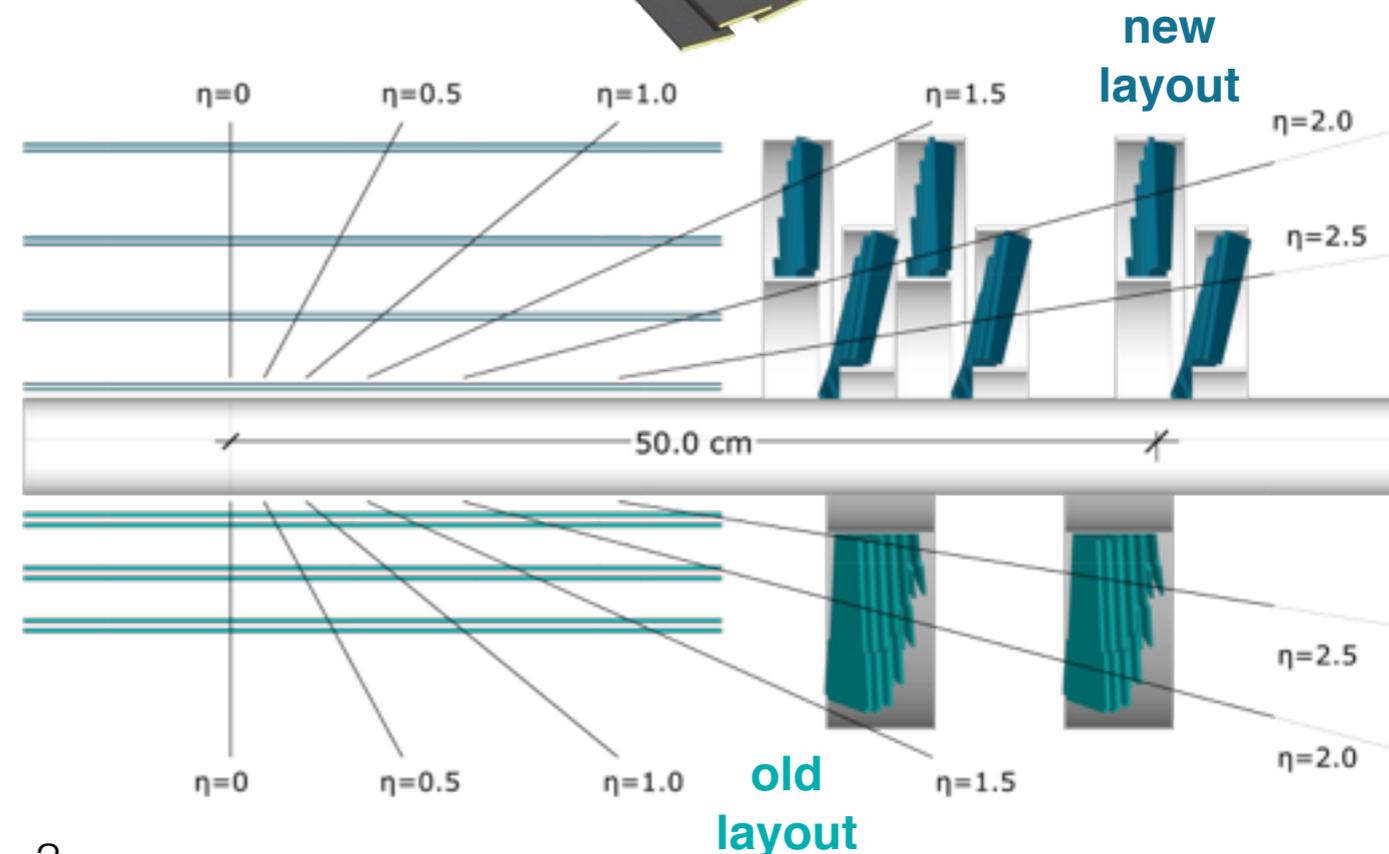
- **additional layers** of pixel modules:
  - 3->4 in the barrel (L1 @ 3cm),
  - 2->3 in the forward region
  - 66M -> 123M channels
- **analog -> digital readout**
- **C<sub>6</sub>F<sub>14</sub> -> CO<sub>2</sub> cooling system**
- **reduced material budget** -> better tracking efficiency & vertex resolution



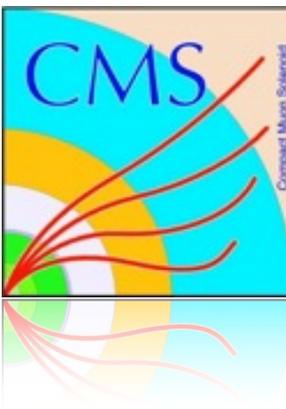
new layout



old layout



# Introduction: Backend Electronics - Requirements



## **Upgrade of FED** (Front-End Driver) **required:**

- adapt to new, **digital 400 Mbps readout** scheme
- **increased number of readout links** (960 -> 2368)
- **higher data rates** from detector front-end
- increased output bandwidth to CMS central DAQ required

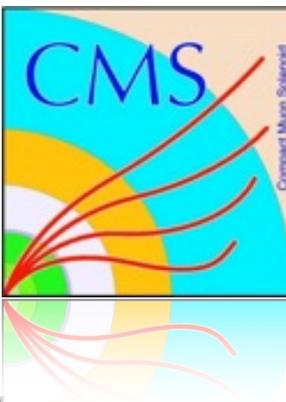
## **Upgrade of FEC** (Front-End Controller) / control system **planned:**

- **VME parts out of production & very few spares available**
- **increased number of control links**
- profit from new technology

**-> decided to implement both cards on  $\mu$ TCA AMC using different mezzanine cards**

**-> target replacement of complete backend-electronics for Phase 1 Pixel Upgrade**

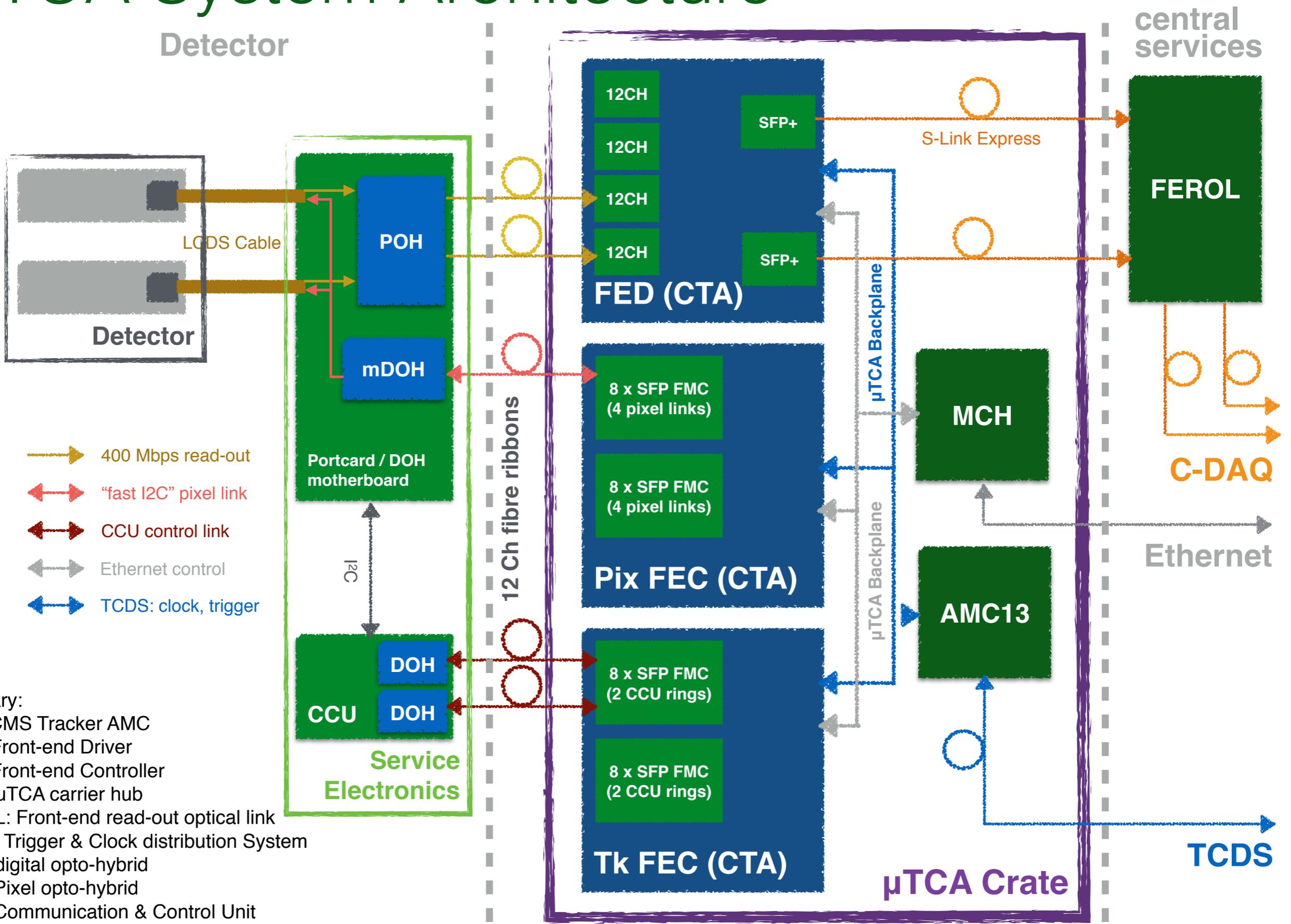
# Introduction: Backend Electronics - Requirements



Location	Links / Module	# of Modules	Data Rate @ 25ns [Mbps]	Data Rate @ 50 ns [Mbps]	Output Rate / 12 Ch: 25/50 ns
BPIX Layer 1	4	96	140	269	2.48/4.96 Gbps
BPIX Layer 2	2	224	78	137	1.14/2.28 Gbps
BPIX Layer 3	1	352	81	133	1.01/2.02 Gbps
BPIX Layer 4	1	512	57	85	0.54/1.08 Gbps
FPIX Inner Rings	1	264	129	231	1.99/4.04 Gbps
FPIX Outer Rings	1	408	68	107	0.78/1.55 Gbps

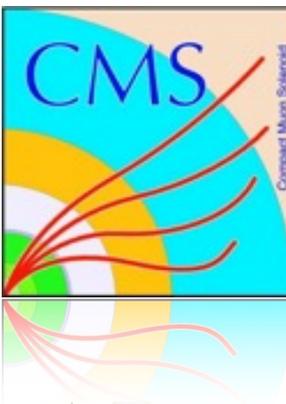
- data rates **estimated from simulations** (pythia & GEANT) @  $\mathcal{L} = 2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  with 25 / 50 ns & 100 kHz L1A rate
- **higher rates from inner layers / rings** requires load balancing by mixing high- & low BW links on same FED
- S-Link Express DAQ output on FED, grouping: **2 x 12 input channels** to **1 x 10 Gbps output**
- 48 input channels / FED (4 x12 Channel receivers)
- number of readout fibres yields: **56 FEDs for Ph1 pixel detector**: 112 DAQ links

# μTCA System Architecture



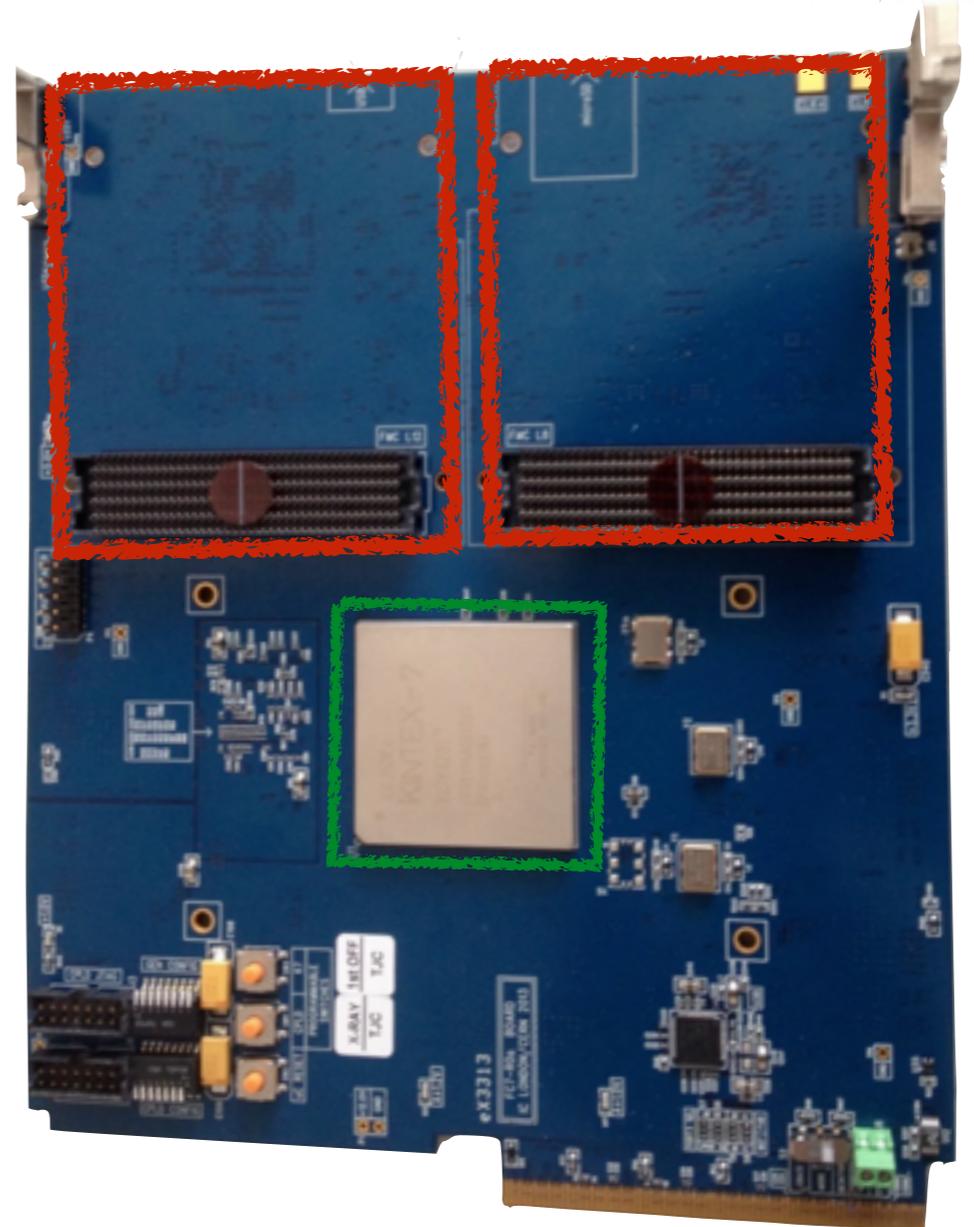
Glossary:  
 CTA: CMS Tracker AMC  
 FED: Front-end Driver  
 FEC: Front-end Controller  
 MCH: μTCA carrier hub  
 FEROL: Front-end read-out optical link  
 TCDS: Trigger & Clock distribution System  
 DOH: digital opto-hybrid  
 POH: Pixel opto-hybrid  
 CCU: Communication & Control Unit

# CMS Tracker AMC (CTA)



- variant of **FC7** board used in TCDS\*
- full-size, double-width AMC
- **Kintex 7 FPGA** (400k logic cells, 30Mb RAM, 400 IOs)
- **2 LPC-compatible FMC slots**
- FMCs support **20** high-speed **serial links** to FPGA (10 Gbps)
- **12** high-speed links to **backplane** (5 Gbps)
- **4 Gb DDR3 RAM** for data buffering

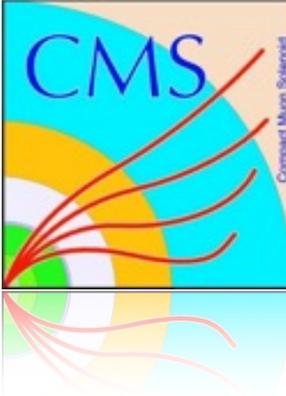
-> **base-board for FED/FECs**



\*see talk “The CMS TCDS Installation” by J. Troska, Thursday

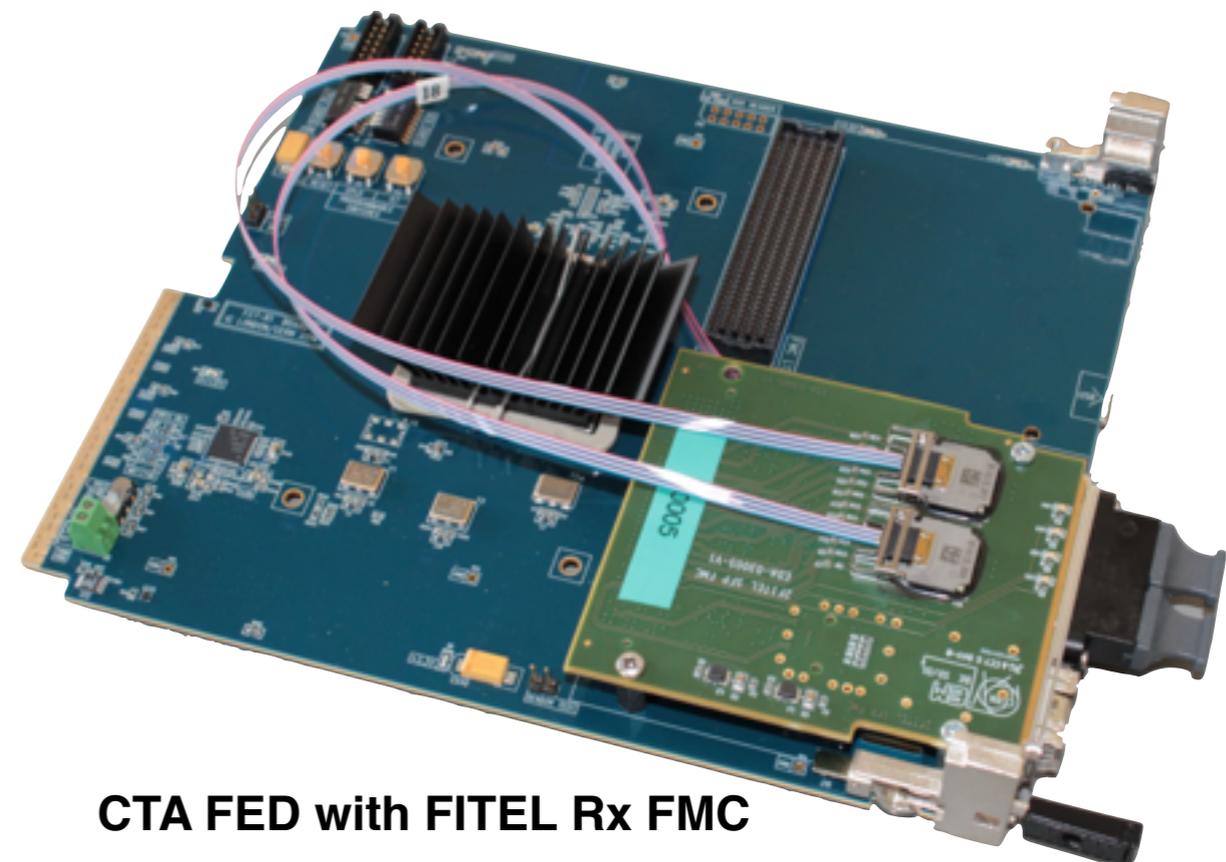
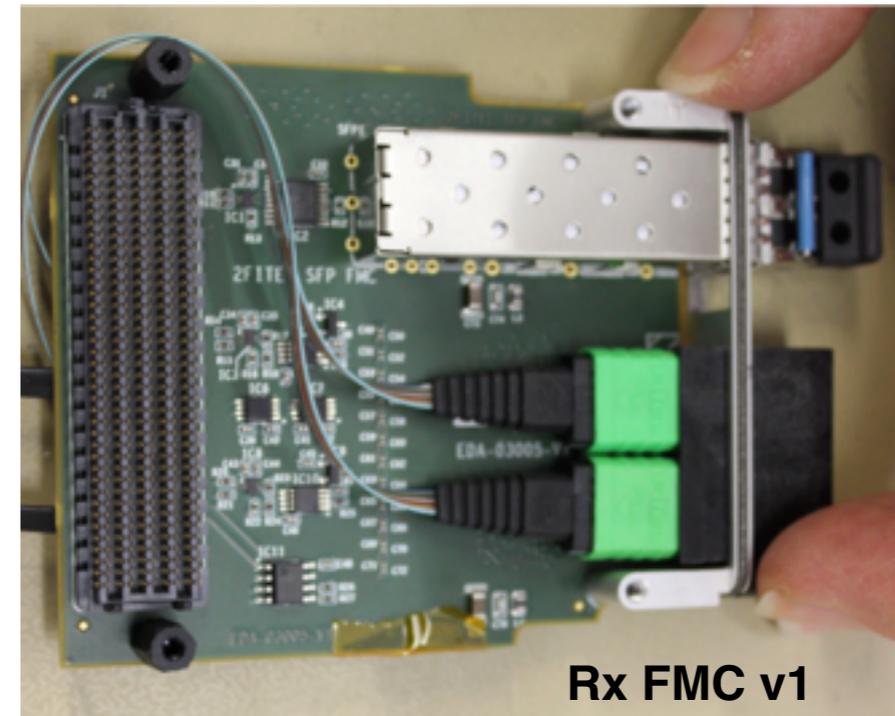
M. Pesaresi, M. Barros Marin, G. Hall, M. Hansen, G. Iles, A. Rose, F. Vasey, and P. Vichoudis. **The FC7 AMC for generic DAQ control applications in CMS.** *Journal of Instrumentation*, 10(03):C03036, 2015.

# Phase 1 Pixel FED: Hardware



Ph1 digital **FED** implemented on top of **CTA board**:

- **48 optical input** channels, **2 DAQ outputs**
- optical components on FMCs:
  - **2 FITEL 12 Channel optical receivers** qualified @ 400 Mbps & adapted to the POH & fibres **operating @ 1310 nm**
  - **1 SFP+ 10 Gbps** transceiver for S-Link Express DAQ output
  - **ADC** for monitoring of light levels
  - v2 prototype validation ongoing
- 1 physical FED = 2 logical FEDs



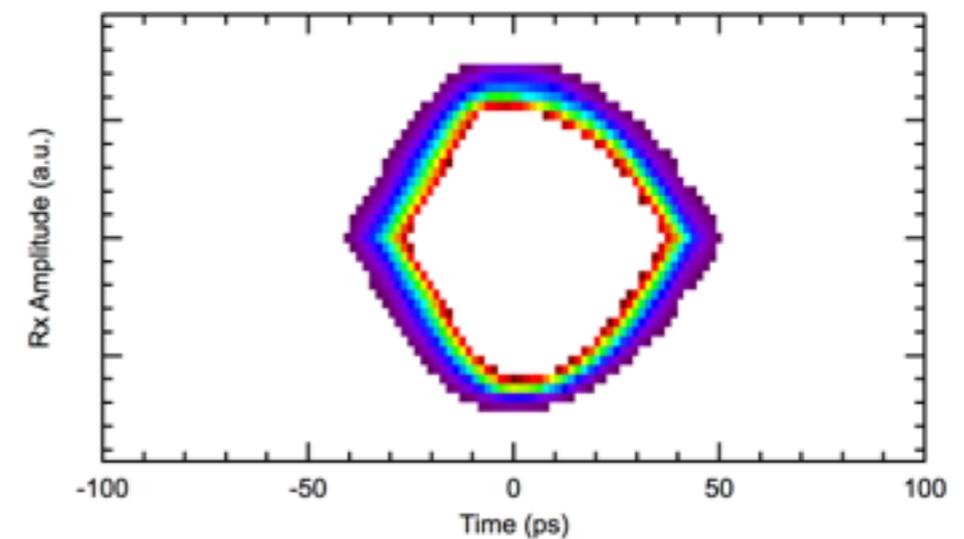
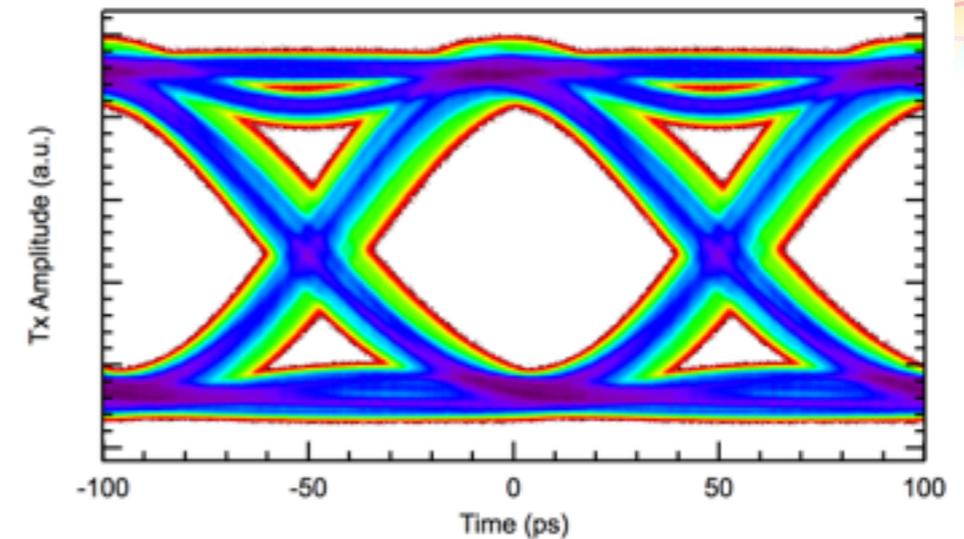
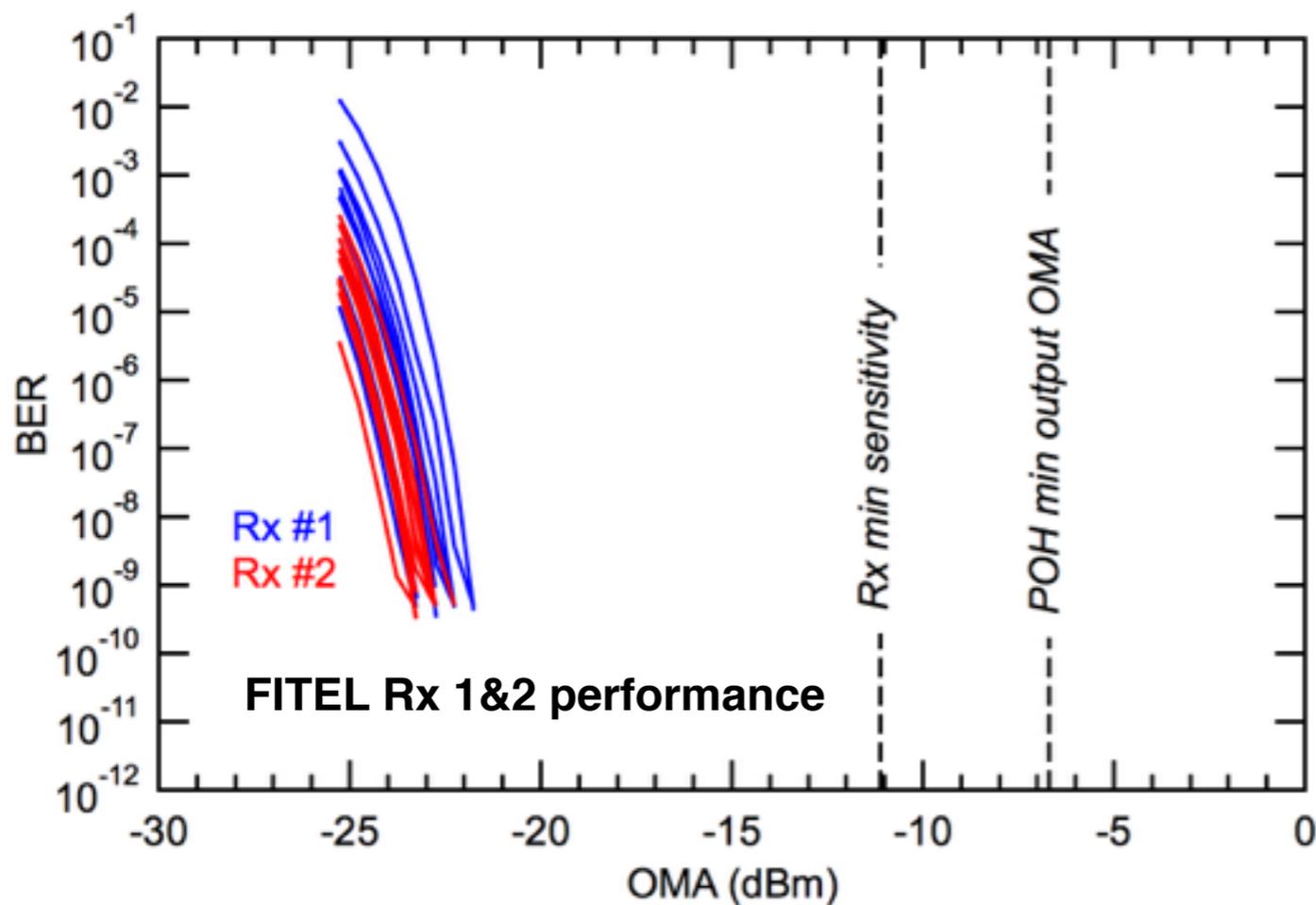
**CTA FED with FITEL Rx FMC**

# Phase 1 Pixel FED: FMC Test Results

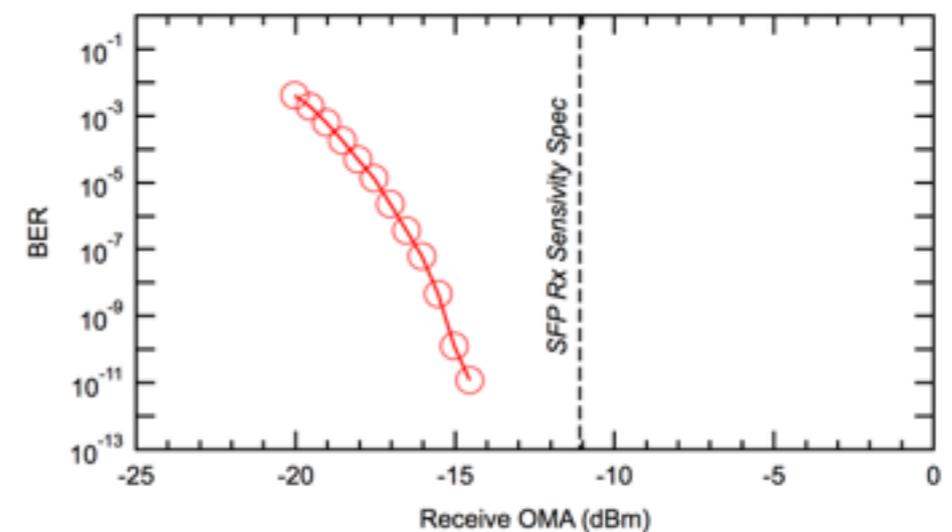


FMC validation using lab setup based on custom BERT on Xilinx Development board:

- Std. PRBS test patterns
- Programmable attenuator and optical switch allow automated testing of each FMC

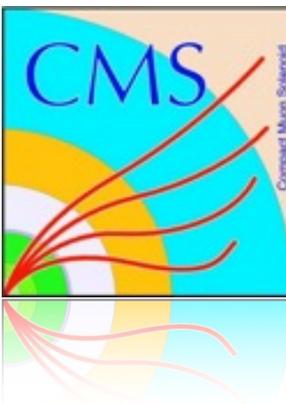


DAQ SFP+ performance



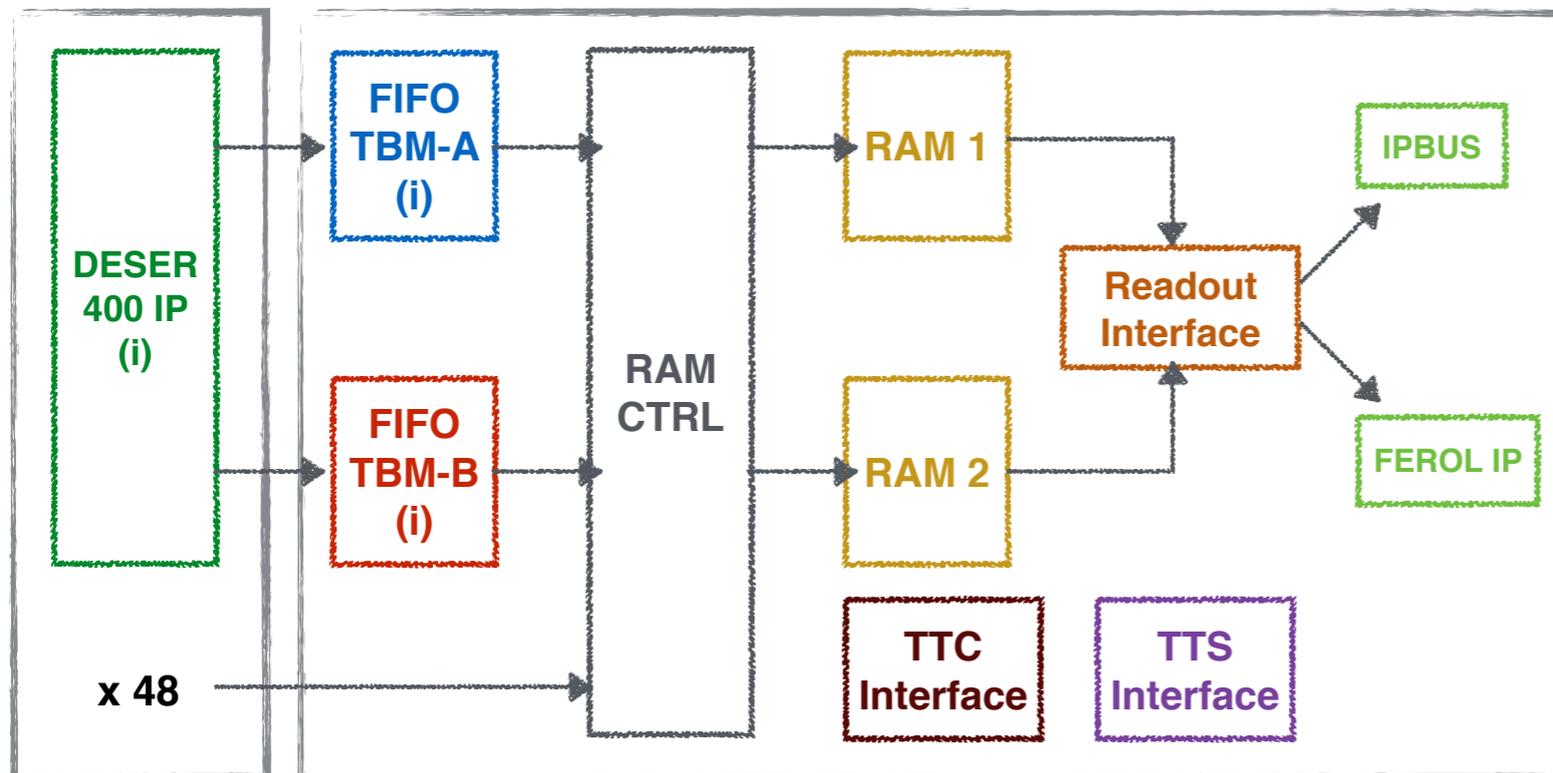


# Phase 1 Pixel FED: Firmware



- **BE IP** block (**IPHC Strasbourg**):

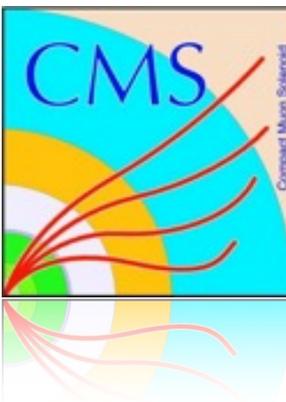
- handling of TCDS signals
- assembly of event fragments from 48 Channels, raw event buffer, DAQ link
- error condition management for all channels: buffer overflow, SEU, channel data missing, timeout, OOS -> **trigger-throttle system states**
- “operation” mode with event data output to C-DAQ
- “local” mode for testing & detector commissioning, readout via IPBUS



**Status:**

integration of FE- & BE IP ongoing

# Control System: FEC Hardware

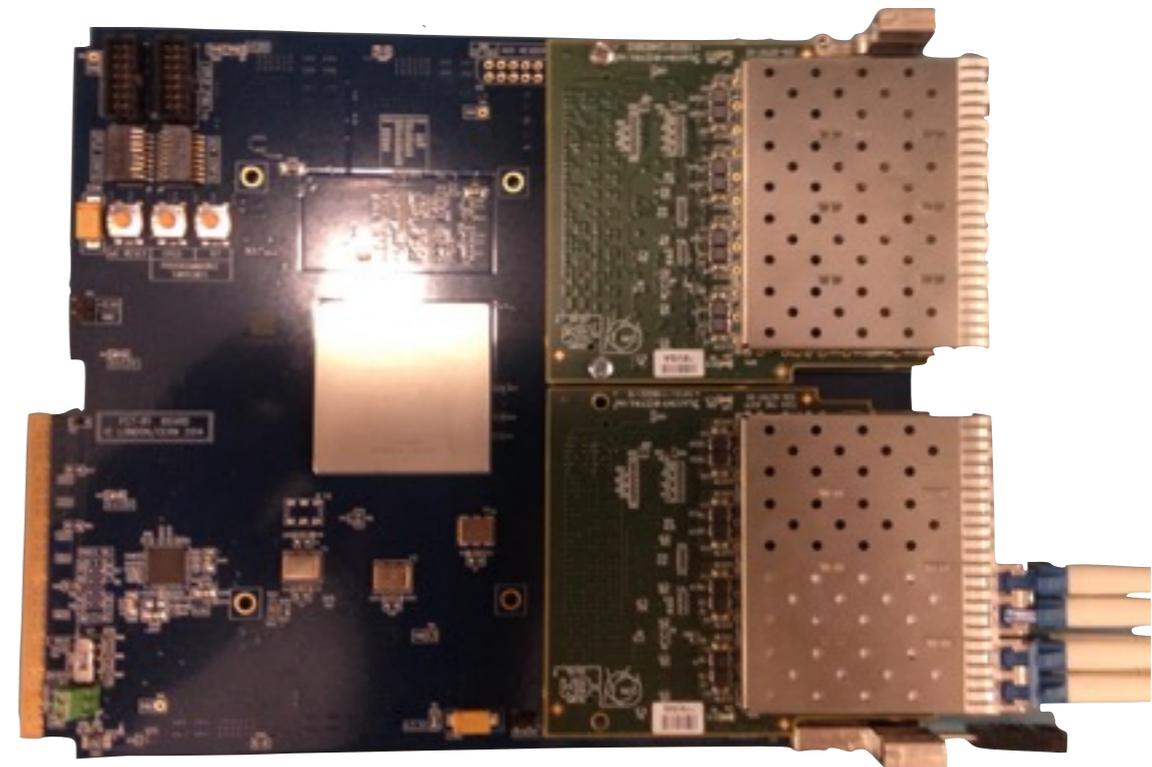


**Front-end Controllers (FEC)** also based on the **CTA board**

- add two **FMCs with low-speed (1 GbE) optical transceivers** to make FECs
- **FMC with 8 SFPs (FEC FMC)** adapted from TCDS, can serve 4 DOH; (8 DOH per CTA = 8 pixel control links or 4 redundant CCU rings)
- **fully qualified by TCDS** project, 56 pcs. available
- **2 flavours of FECs** in the pixel backend:
  - **hardware for pixel- & tracker FEC completely identical**
  - **FW determines FEC flavour**

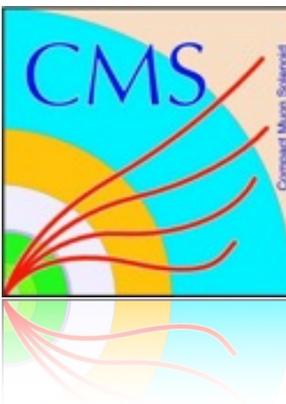
pixel detector requires **14** (8+6) **pixel-** & **2** (1+1) **tracker FECs**

**FEC FMC**



**CTA FEC w 2 x 8 SFP FMCs mounted**

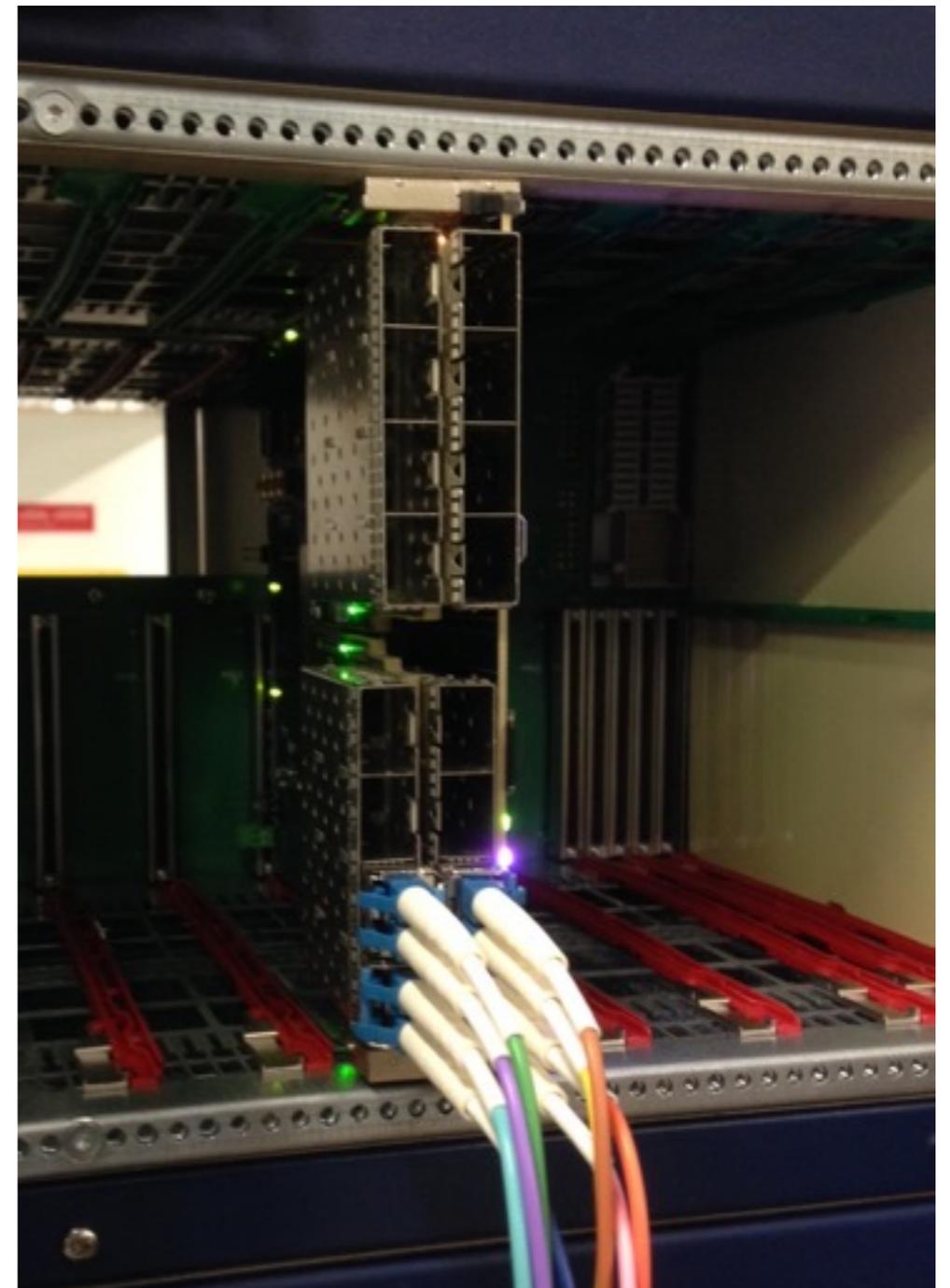
# Control System: Tracker FEC



- Tracker FEC\* drives redundant CCU token-ring\*\* used to program ASICS / opto-hybrids on pixel service electronics via I<sup>2</sup>C
- no functional difference w.r.t current VME part
- **4 redundant CCU rings / CTA**
- **TCDS signals** foreseen in the future for full Tracker FEC / CCS functionality (not required for pixel use)
- validation of FW on CTA ongoing
- control **SW library successfully adapted**

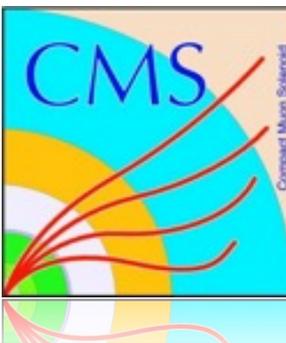
\* Kloukinas et al.. Kostas FEC-CCS: **A common front-end controller card for the CMS detector electronics.**

\*\* C. Paillard, C. Ljuslin, and A. Marchioro. **The CCU25: A network oriented communication and control unit integrated circuit in a 0.25- $\mu$ m CMOS technology.**

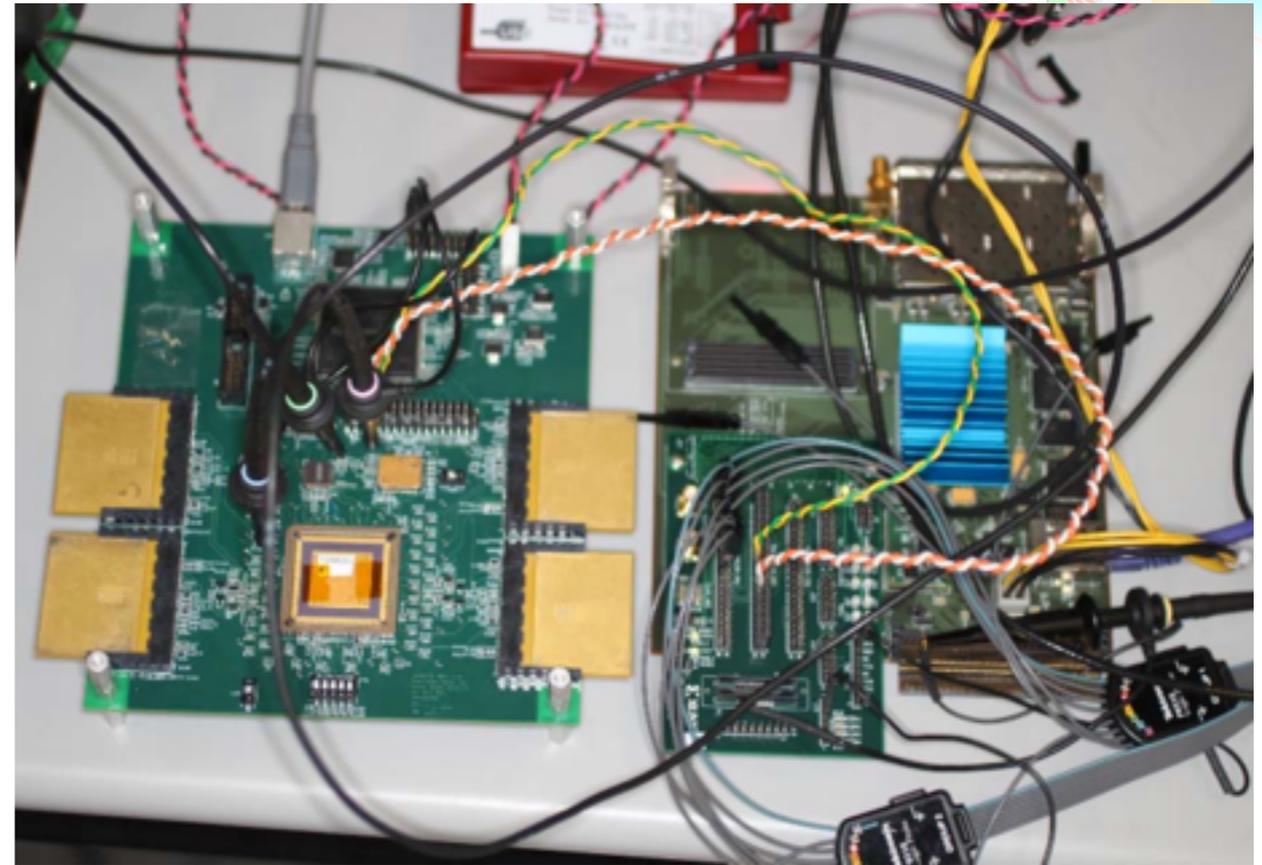


**CTA FEC with 1 redundant control-ring connected**

# Control System: Pixel FEC



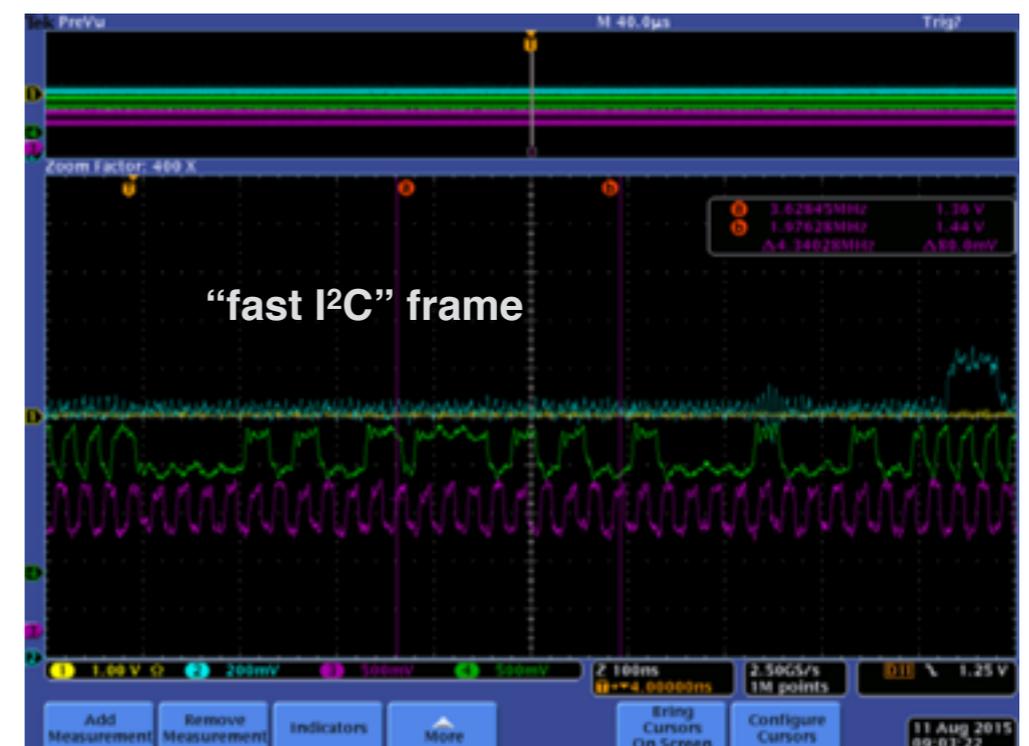
Development Bench w. TBM fixture & GLIB



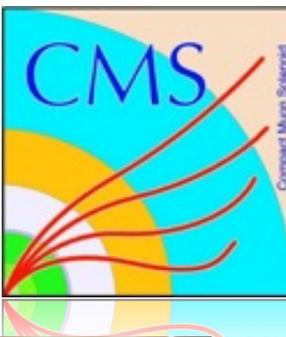
## Pixel FEC:

- **programming of FE** (TBM / ROC) **DAC** registers via **“fast I<sup>2</sup>C”** protocol (I<sup>2</sup>C-like; **CLK & DATA** lines; 80 Mbps)
- distribution of **clock, trigger** to modules & **fast command interpretation** (received via backplane)
- **8 pixel control links** per **CTA FEC** (non-redundant)
- functionality is the same w.r.t. present VME pixel FEC
- can profit from FW IP written for Tracker FEC

KANSAS STATE  
UNIVERSITY



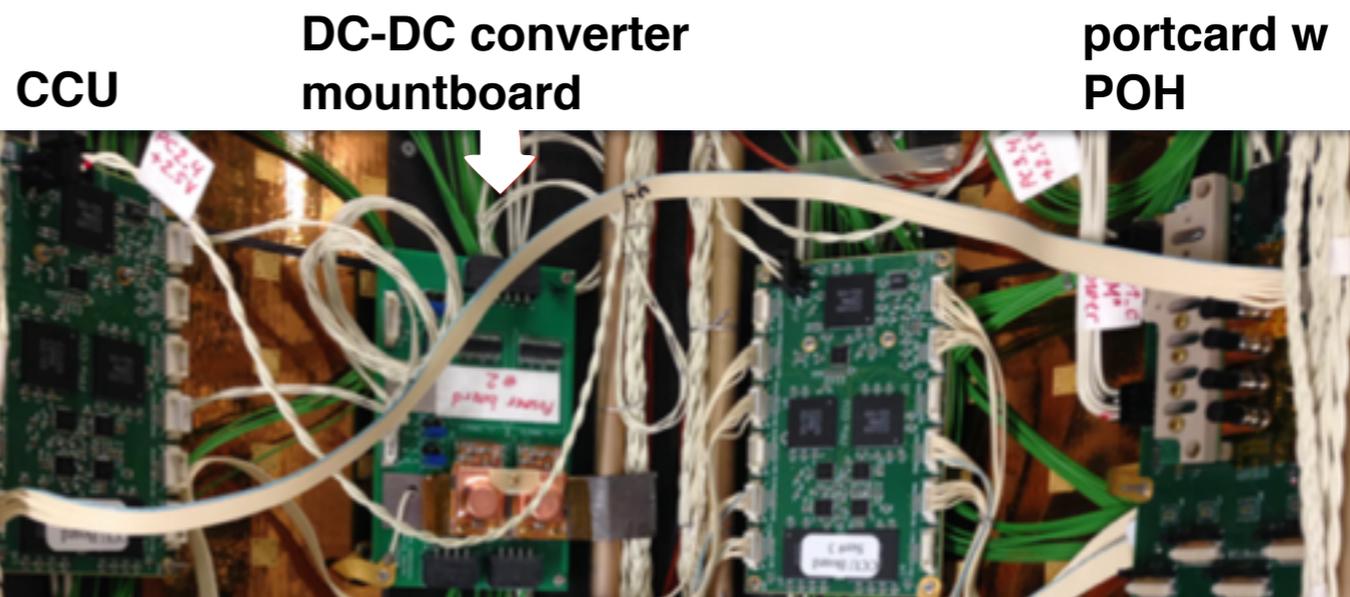
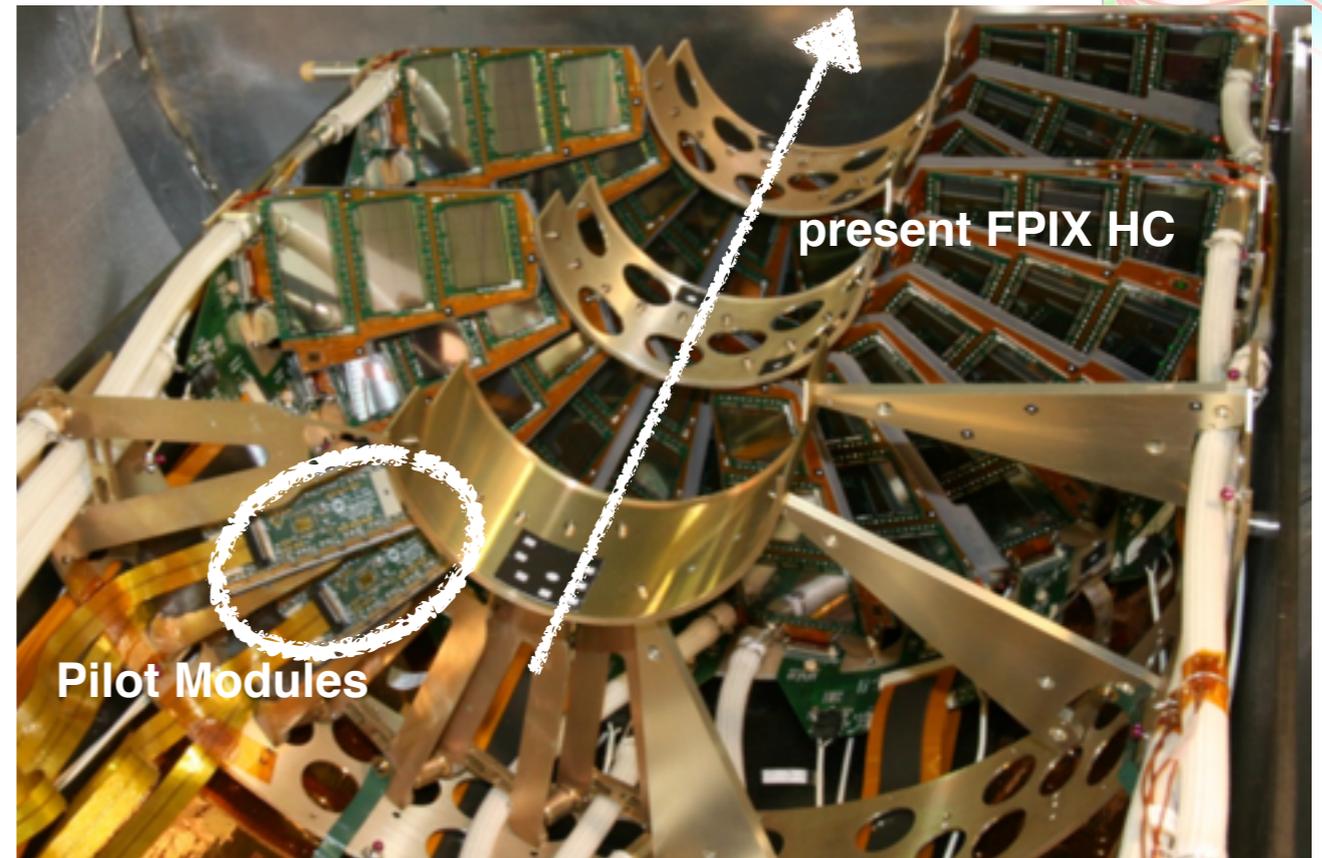
# System Tests: Pilot Blade



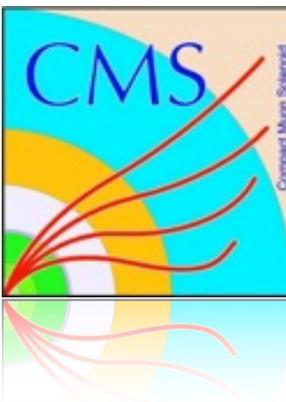
**Phase 1 Pilot Blade:** 8 digital modules (currently w. VME DAQ) installed inside CMS **FPIX** during **LS1**:

- fully integrated with CMS (TCDS, DAQ)
- now running in separate DAQ partition
- test of components / FE / BE (HW + FW) under *realistic operating conditions* inside CMS
- deploy & run  $\mu$ TCA parts as soon as validated in the lab
- $\mu$ TCA infrastructure recently installed in CMS

towards IP



# System Tests: Validation & Integration



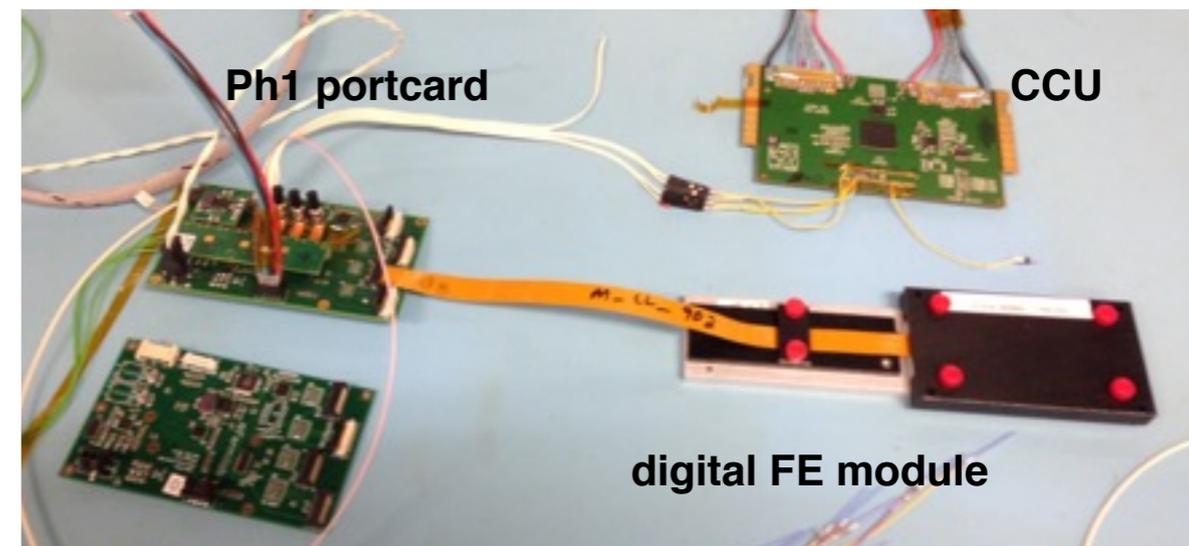
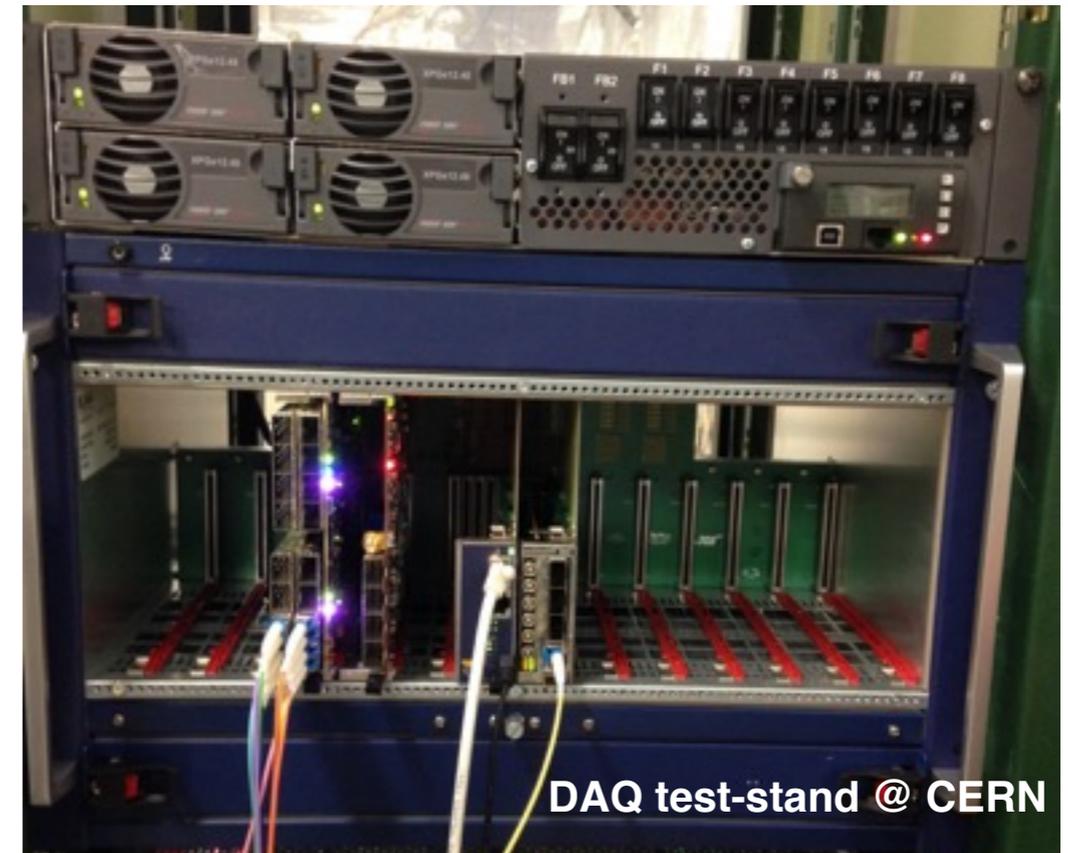
**validation of hardware, firmware & SW development**  
on small-scale test stands with complete FE chain

**evolution to larger-scale systems in 2016:**

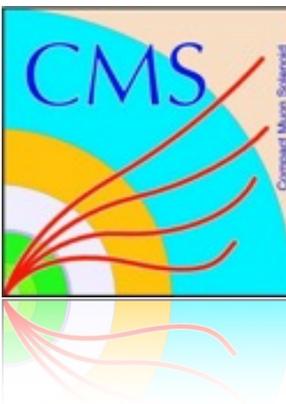
- FPIX Half-Disk test-stand: validation of FED HW
  - **1 full FED (48 channels)**
  - **are all channels working correctly (optical receivers,...)?**
- FPIX Half-Cylinder reception tests / BPIX commissioning test:
  - **test & verify functionality of FE** after shipping from US / assembly of BPIX sectors
  - HC reception test: **4 FEDs, 2 pxFEC & 1 tkFEC**
- DAQ Tests: participate in global CMS runs and send data to C-DAQ

**FED (&FEC) in-crate burn-in / long-term tests:**

- verify long-term stability of parts
- continuously operate FED with fake / internal data over long periods of time

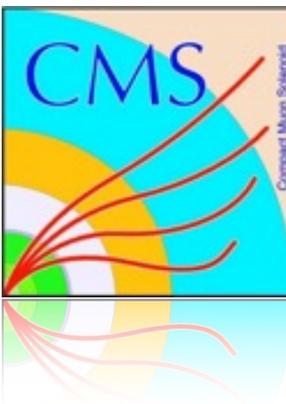


# Summary

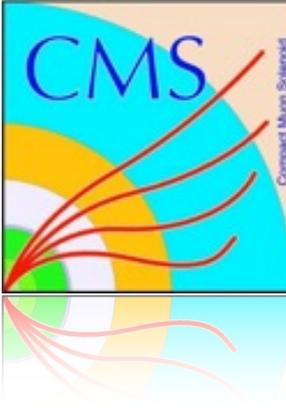


- new **μTCA DAQ system** under development for **CMS Phase 1 Pixel Detector**
  - new digital read-out scheme operating @ 400 Mbps to cope with higher data-rate
- **Pilot Blade system** installed **in CMS** during LS1, presently running with VME backend, deployment of μTCA components after lab-testing
- **FED / FECs based on CTA board** + various FMCs with optical components
  - HW validation & testing with pre-production parts ongoing
  - FW development well advanced
  - SW adaptation starting
  - series production in 2016
- extensive component- and system-level testing program ahead in 2016
- **installation** of full Ph1 detector during **extended YETS 2016 / 2017**

# References



- B Meier. CMS pixel detector with new digital readout architecture. *Journal of Instrumentation*, 6(01):C01011, 2011.
- R. Stringer. A digital readout system for the CMS Phase I Pixel Upgrade. *Journal of Instrumentation*, 10(04):C04037, 2015.
- M. Pesaresi, M. Barros Marin, G. Hall, M. Hansen, G. Iles, A. Rose, F. Vasey, and P. Vichoudis. The FC7 AMC for generic DAQ control applications in CMS. *Journal of Instrumentation*, 10(03):C03036, 2015.
- C. Paillard, C. Ljuslin, and A. Marchioro. The CCU25: A network oriented communication and control unit integrated circuit in a 0.25- $\mu$ m CMOS technology. *Proceedings of the 8th Workshop on Electronics for LHC Experiments*, Colmar, page 174, 2002.
- Kloukinas et al.. Kostas FEC-CCS: A common front-end controller card for the CMS detector electronics. *Proceedings of the 12th Workshop on Electronics for LHC and Future Experiments (LECC 2006)*, Valencia, page 179, 2006.
- PICMG. Micro Telecommunications Computing Architecture Short Form Specification. [https://www.picmg.org/wp-content/uploads/MicroTCA\\_Short\\_Form\\_Sept\\_2006.pdf](https://www.picmg.org/wp-content/uploads/MicroTCA_Short_Form_Sept_2006.pdf), September 2006.
- E Hazen, A Heister, C Hill, J Rohlf, S X Wu, and D Zou. The amc13xg: a new generation clock/timing/daq module for cms microtca. *Journal of Instrumentation*, 8(12):C12036, 2013.
- Robert Frazier, Greg Iles, Dave Newbold, and Andrew Rose. Software and firmware for controlling {CMS} trigger and readout hardware via gigabit ethernet. *Physics Procedia*, 37:1892 – 1899, 2012. *Proceedings of the 2nd International Conference on Technology and Instrumentation in Particle Physics (TIPP 2011)*.
- Gerry Bauer, Tomasz Bawej, Ulf Behrens, James Branson, Olivier Chaze, Sergio Cittolin, Jose Antonio Coarasa, Georgiana-Lavinia Darlea, Christian Deldicque, Marc Dobson, Aymeric Dupont, Samim Erhan, Dominique Gigi, Frank Glege, Guillermo Gomez-Ceballos, Robert Gomez-Reino, Christian Hartl, Jeroen Hegeman, Andre Holzner, Lorenzo Masetti, Frans Meijers, Emilio Meschi, Remigius K Mommsen, Srecko Morovic, Carlos Nunez-Barranco-Fernandez, Vivian O'Dell, Luciano Orsini, Wojciech Ozga, Christoph Paus, Andrea Petrucci, Marco Pieri, Attila Racz, Olivier Raginel, Hannes Sakulin, Matteo Sani, Christoph Schwick, Andrei Cristian Spataru, Benjamin Stieger, Konstanty Sumorok, Jan Veverka, Christopher Colin Wakefield, and Petr Zejdl. The new cms daq system for lhc operation after 2014 (daq2). *Journal of Physics: Conference Series*, 513(1):012014, 2014.



# BACKUP

# PSI46dig & digital TBM



analog CMS Pixel **ROC** (PSI46) loses efficiency at high rates

-> upgrade required: **PSI46dig** (evolution of analog version)

- 8-bit ADC
- increase buffer size for timestamp and data, added readout buffer
- digital data transmission
- digital readout at 160 MHz

digital ROC requires adapted **Token Bit Manager (TBM)** chip & read-out chain:

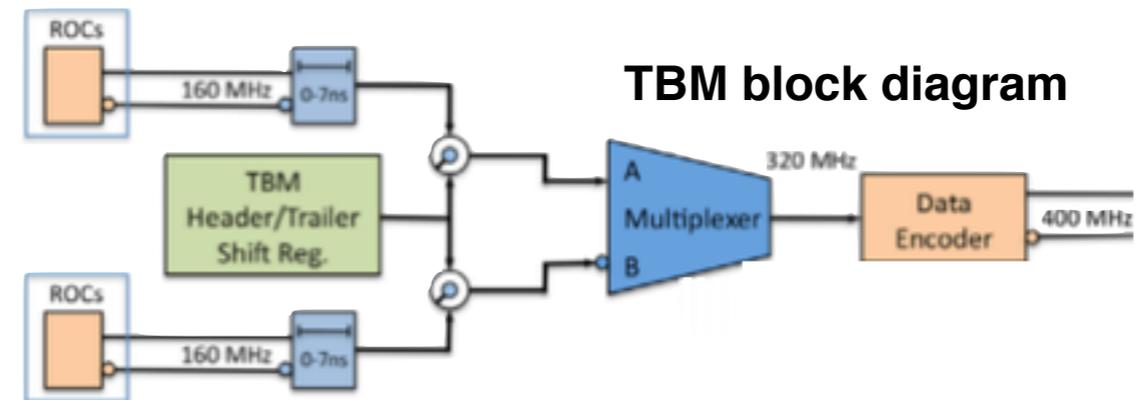
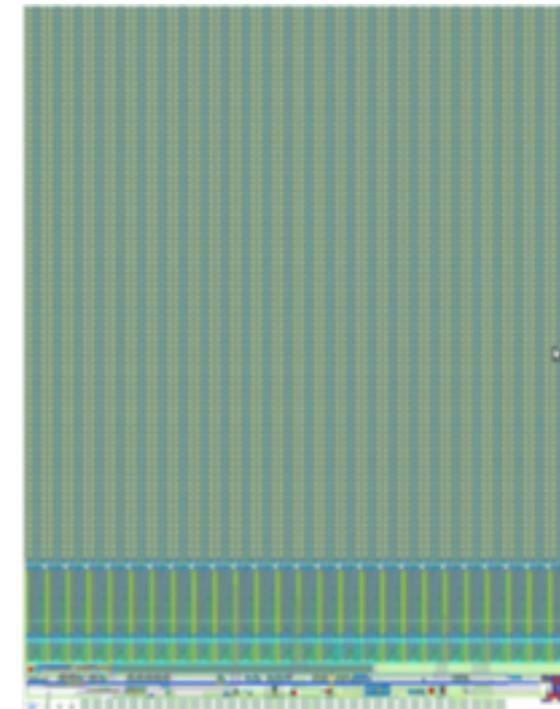
- adapted TBM from 40 MHz analog to 160 MHz digital token scheme
- 2:1 multiplexed, 4-to-5 bit encoded datastream
- 2 x 160 Mbps from TBM cores A & B -> 400 Mbps output
- 2 Versions:
  - TBM08 for layers 3 & 4
  - TBM09 for layers 1 & 2 (2 links / TBMs & 2 TBMs for L1)

new service electronics, opto-hybrids & ultimately backend electronics required to transmit & decode the digital signal

## PSI46dig:

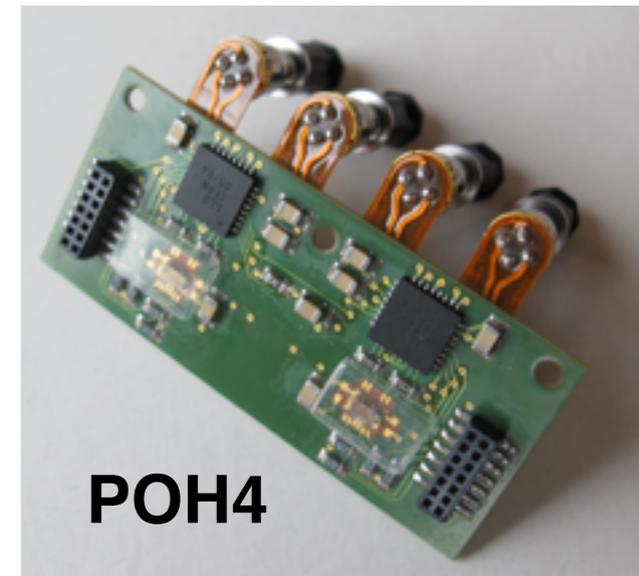
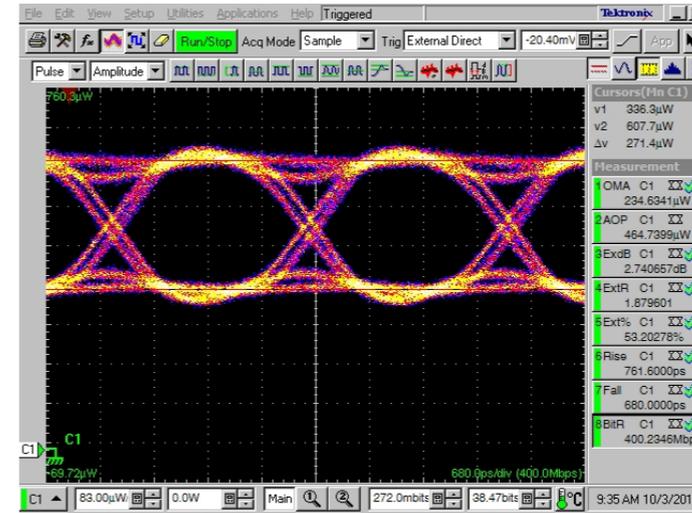
- 52x80 pixels of 150 x 100  $\mu\text{m}$
- 25 double columns with data buffer

PSI46dig floorplan

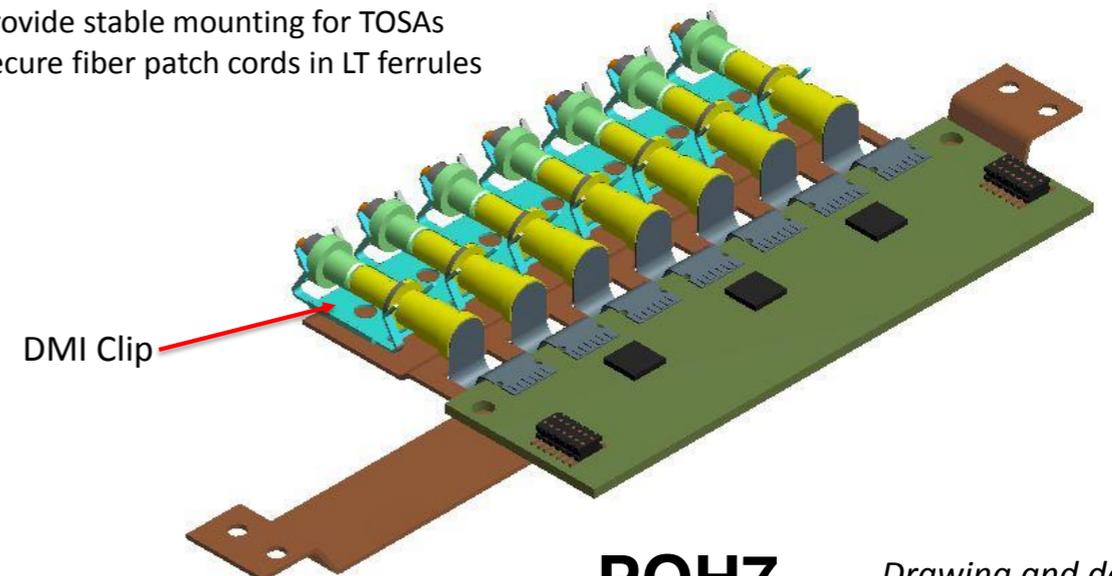


# Pixel-Opto-Hybrid

- new part adapted to 400 Mbps digital readout
- versions with 4 or 7 TOSAS (transmitter-optical-sub-assembly)
- much improved radiation tolerance
- based on Fabry-Pèrot laser diode @ 1310 nm (very similar to present AOH)
- tested with 4b5b NRZI encoding
- system-test with FE components & Rx module in progress
- 96 POH7 required for Ph1 FPIX



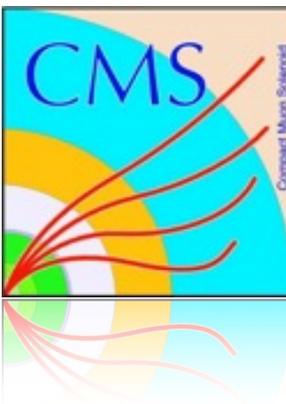
DMI Clips  
Provide stable mounting for TOSAs  
Secure fiber patch cords in LT ferrules



**POH7**

*Drawing and design  
courtesy of Kirk Arndt*

# μTCA Standard in CMS



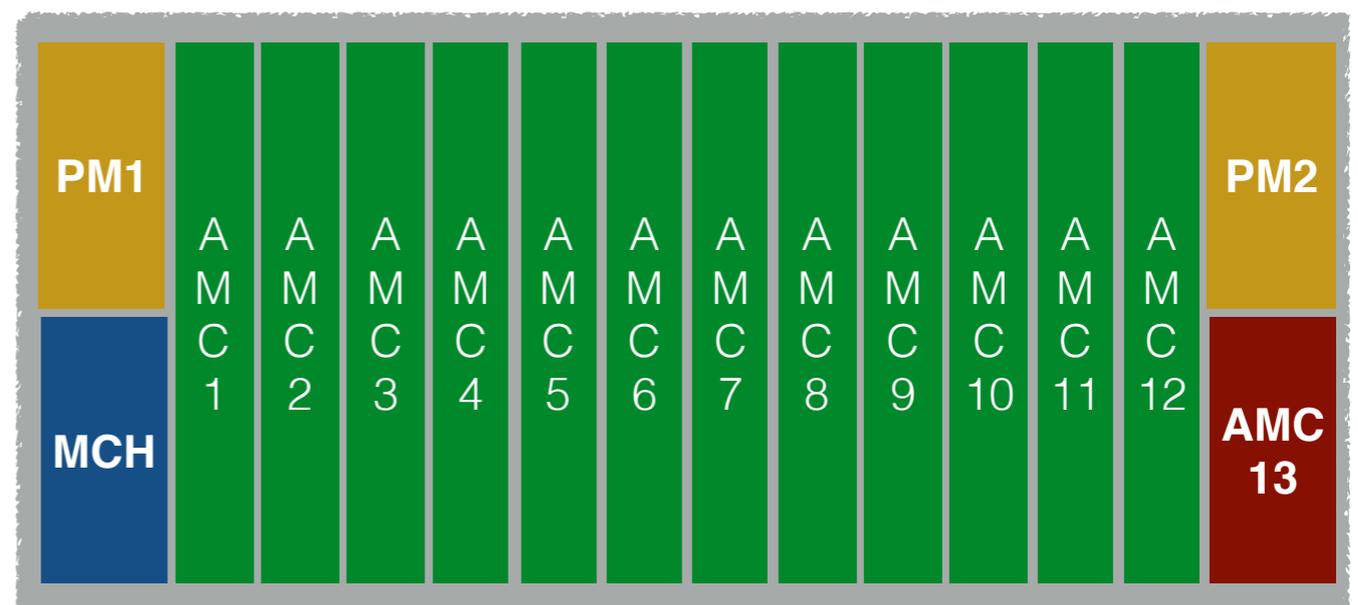
CMS has chosen to **replace existing VME** electronics with **μTCA systems** for the upcoming **upgrades**:

- flexible, high density backplane
- can use standard serial communication protocols like GbE or PCIe
- uses AMC (Advanced Mezzanine Card) standard

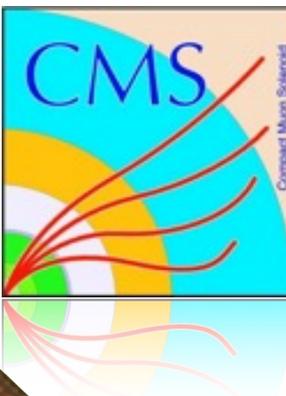
CMS adopted:

- **redundant dual-star backplane** configuration
- **GbE** communication protocol via commercial **MCH**
- **LHC clock, trigger & fast control** signal distribution via **custom** MCH-like module: **AMC13**

PM: power module  
MCH: microTCA carrier hub  
AMC: advanced mezzanine card



# $\mu$ TCA System: Auxiliary Components

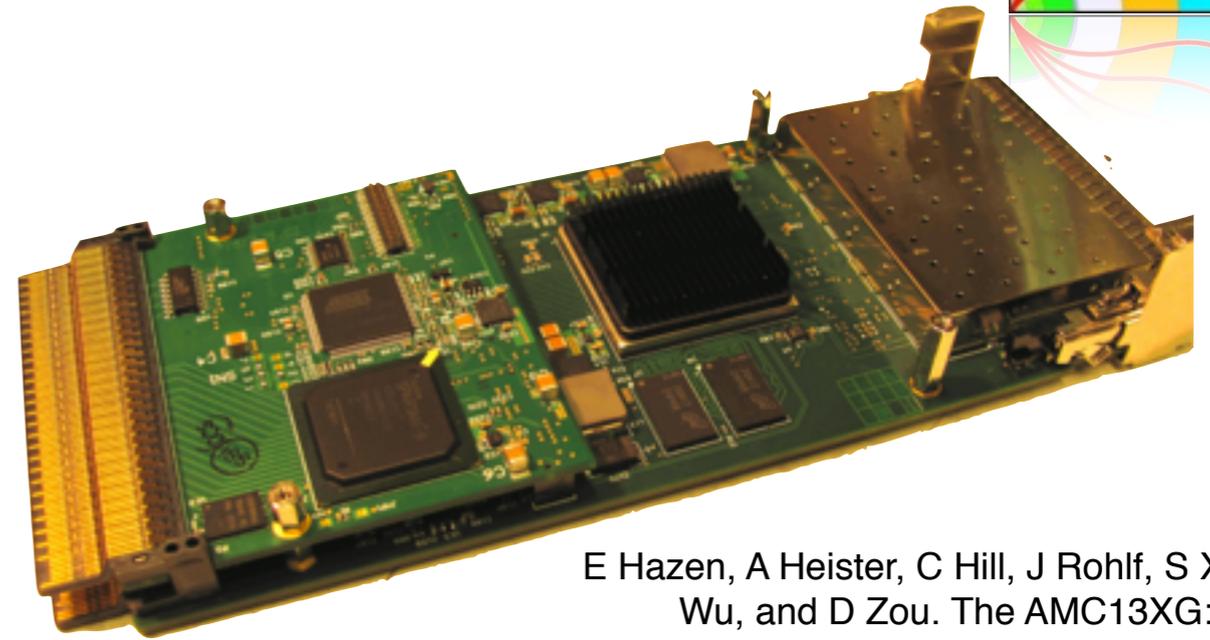


## **AMC13 XG: interface to the CMS TCDS** (trigger- & clock distribution system)

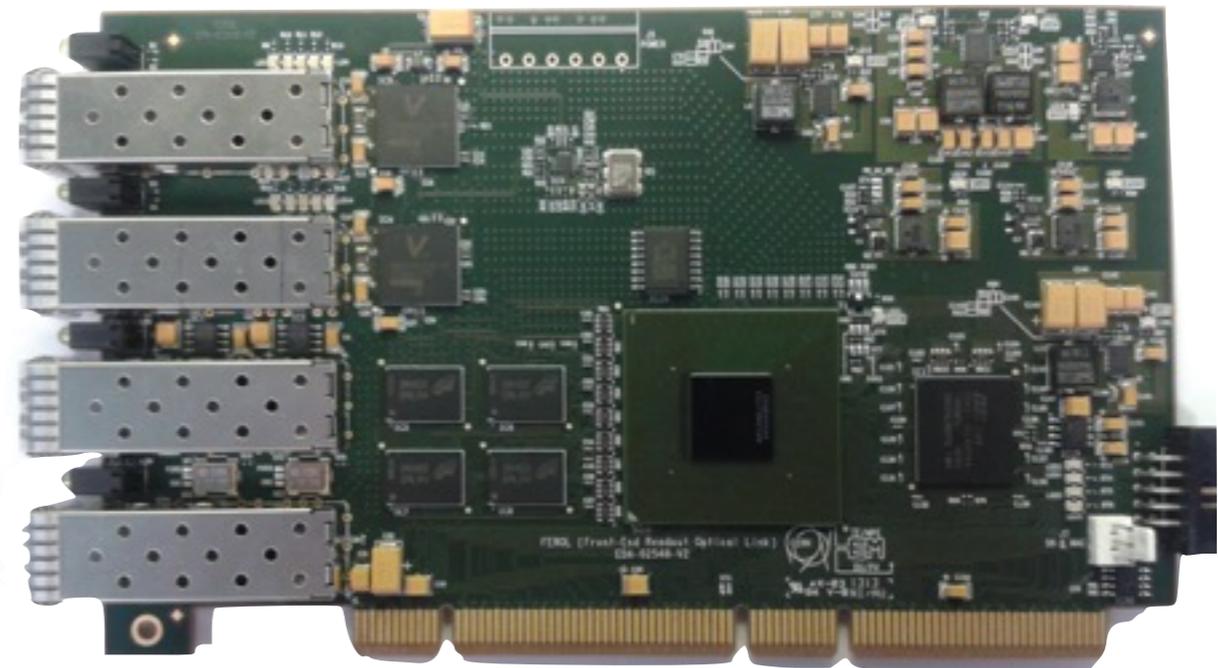
- TCDS replaces legacy TTC & TTS
- full duplex 160 Mbps optical fibre
- **distributes clock, triggers** and **fast commands** (B-Channel: reset, resynch, ...) to AMC's (downstream)
- forwards error conditions from FEDs to C-DAQ (upstream)
- supports up to 3 x 5 Gbps optical DAQ links (S-Link Express): not sufficient for the pixel data rates

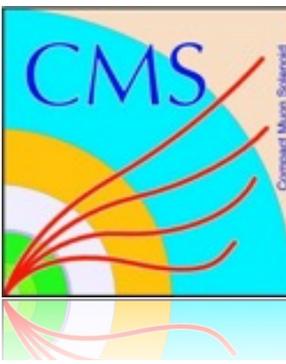
## **C-DAQ** Link: increased bandwidth requirements from AMC13 / FEDs to C-DAQ due to higher luminosity -> upgrade to **optical S-Link Express**

- new Front-End-Readout optical Link (FEROL) card developed
- up to **10 Gbps per link**
- compatible with legacy FRL system



E Hazen, A Heister, C Hill, J Rohlf, S X Wu, and D Zou. The AMC13XG: A new generation clock/timing/daq module for cms microtca. *Journal of Instrumentation*, 8(12):C12036, 2013.



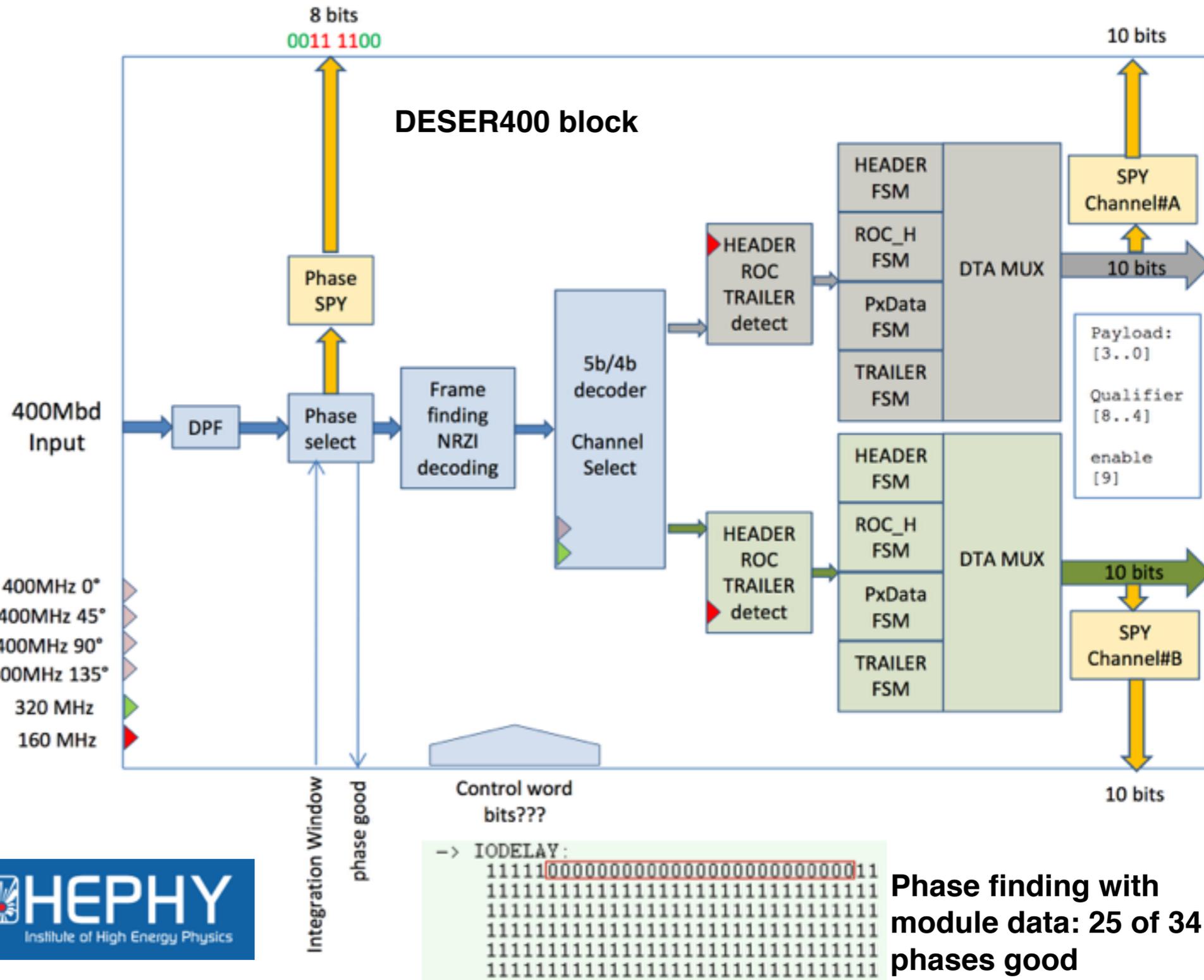


# Phase 1 Pixel FED: Firmware

**FED FW** development factorized in **2 components**:

- **FE DESER400** block (HEPHY Vienna):

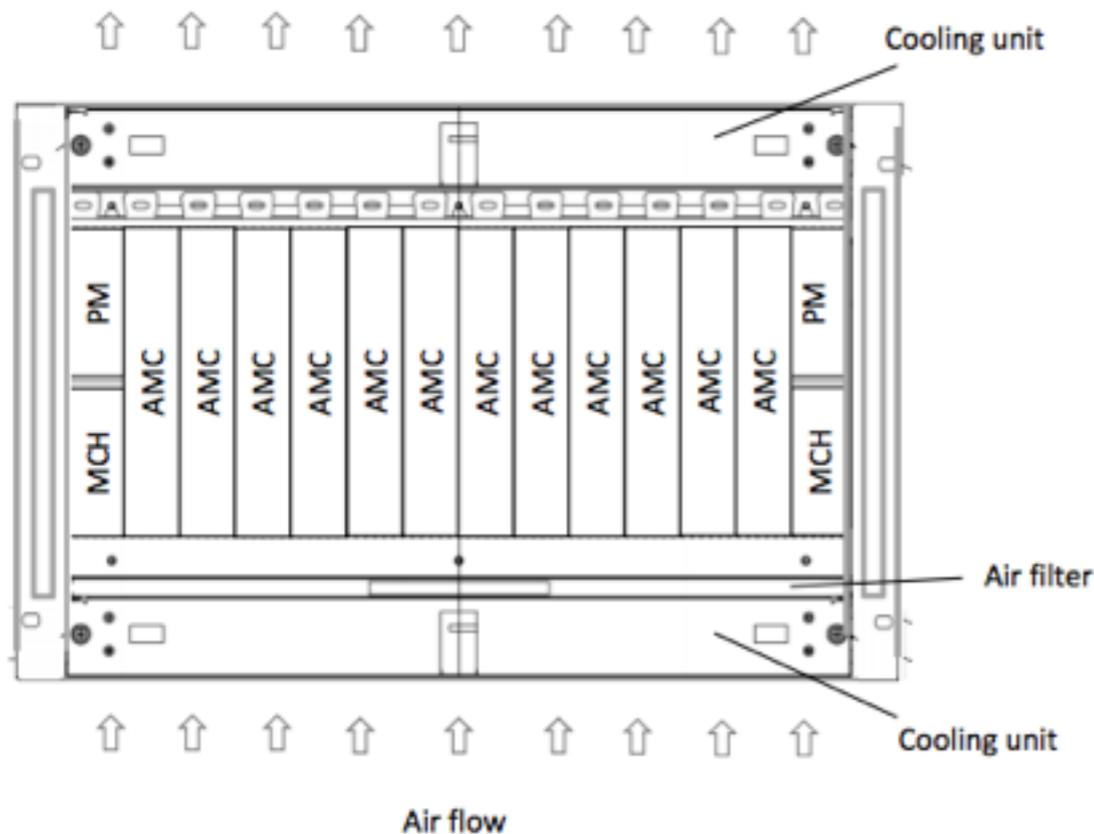
- **phase finding**: with Kintex7 IDELAY feature
- **deserialisation & decoding** of FE signals
- **FSM** for consistency check of incoming data
- IP block implemented **48 times per CTA**



# Integration



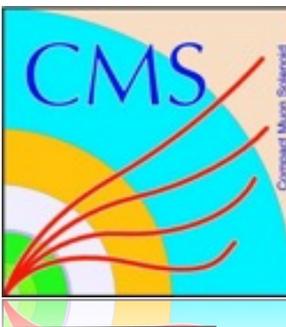
- “final” CMS  $\mu$ TCA crate currently under evaluation: dual-star backplane
- bulk AC-DC power supplies
- **8 crates** foreseen for **Ph1 pixel detector**: BPIX: 4, FPIX: 2 + TkFECs + spares
- additional 96 MPO patch-panels (PP2)
- to be installed during extended **YETS 2016 - 2017**



Last update: 07 August 2015 by JT

ID	Units	Contents S1Gxx - FPIX														RackWiz	ID	Units	Contents S1Gxx - BPIX														RackWiz		
		1	2	3	4	5	6	7	8	9	10	11	12	13	14				1	2	3	4	5	6	7	8	9	10	11	12	13	14			
56	4	Turbine															56	4	Turbine																
55																	55																		
54																	54																		
53																	53																		
52	1	Heat Exchanger															52	1	Heat Exchanger																
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44		Cable Organizer																	44	Cable Organizer															
43	1	Heat Exchanger															43	1	Heat Exchanger																
42	8	1 2 3 4 5 6 7 8 9 10 11 12														FPIX-1	42	8	1 2 3 4 5 6 7 8 9 10 11 12														BPIX-2		
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35		Cable Organizer																	35	Cable Organizer															
34	1	Heat Exchanger															34	1	Heat Exchanger																
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25	1	Heat Exchanger															25	1	Heat Exchanger																
24	8	1 2 3 4 5 6 7 8 9 10 11 12														CCU Ring FECs	24	8	1 2 3 4 5 6 7 8 9 10 11 12														BPIX-4		
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17		Cable Organizer																	17	Cable Organizer															
16	1	Heat Exchanger															16	1	Heat Exchanger																
15	2	Air Deflector															15	2	Air Deflector																
14	2	96x MPO patch panel															14	2	96x MPO patch panel																
13	2	96x MPO patch panel															13	2	96x MPO patch panel																
12	1	Cable Organizer															12	1	Cable Organizer																
11	2	96x MPO patch panel															11	2	96x MPO patch panel																
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9	2	96x MPO patch panel															9	2	96x MPO patch panel																
8	1	Cable Organizer															8	1	Cable Organizer																
7	2	96x MPO patch panel															7	2	96x MPO patch panel																
6	2	96x MPO patch panel															6	2	96x MPO patch panel																
5	1	Cable Organizer															5	1	Cable Organizer																
4	1	Cable Organizer															4	1	Cable Organizer																
3	4	Cable Feedthrough															3	4	Cable Feedthrough																
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# Phase 1 Pixel FED: FED Tester



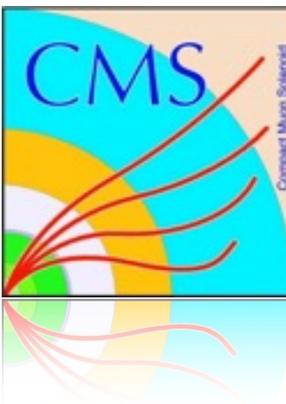
in parallel with FED development, work on a **FED tester / TBM emulator** ongoing (**RICE, IPHC Strasbourg**):

- based on SFP FMC, eventually FITEL Tx in future
- reproduce TBM behaviour without requiring FE chain (module, etc)
- allows to **stress-test FED (FW)** with variable rates, event sizes (fixed patterns, digitized events from simulations), phases, light levels
- **test FED FW w.r.t. error conditions** (buffer overflow, missing data, stuck channel, SEU etc.)
- **debugging** during FW development / production tests



**GLIB w. 2 x FITEL Tx module mounted on FMC (requires adapted Rx)**

# $\mu$ TCA System: Architecture



- pixel modules connect electrically to service boards mounted in supply tube / service cylinder
- service boards hold data- & control opto-hybrids for signal conversion & auxiliary devices (Delay25, PLLs, level translators, CCUs, DC-DC converters...)

- **3 devices** necessary to **control / readout pixel detector**:

1. **pixel FED** (Front-end Driver): receives, deserialises & decodes module data



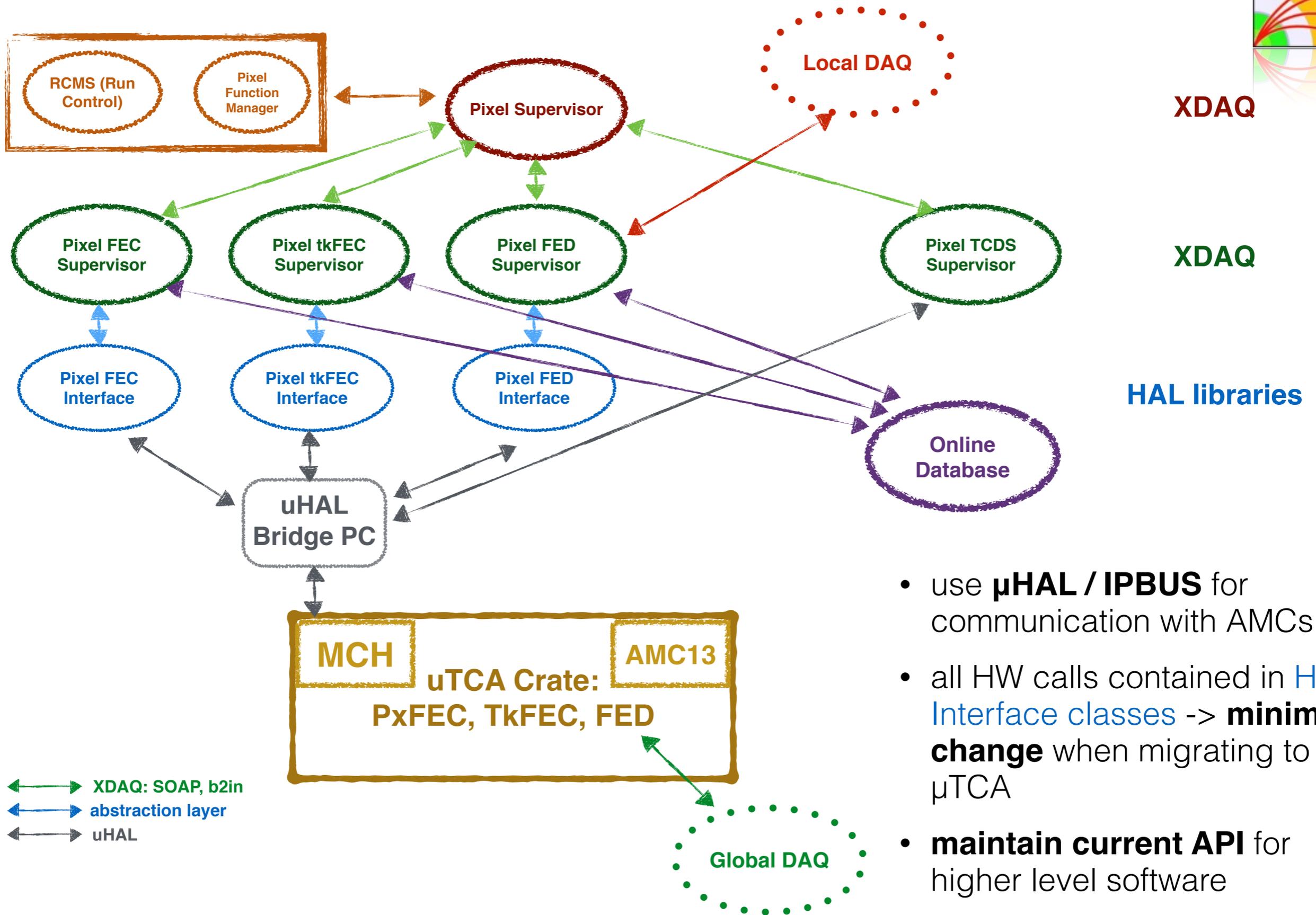
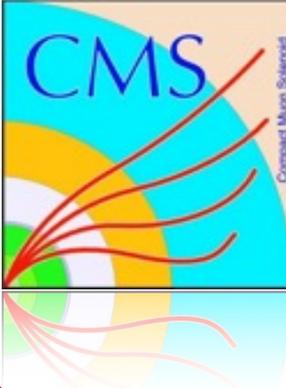
2. **pixel FEC** (Front-end Controller): responsible for programming of pixel modules via “fast I2C” protocol, distributes CLK, TRG & fast signals to front-end via mDOH



3. **tracker FEC**: used to program the service electronics via DOH & I2C & PIA interfaces of CCU boards



# Pixel Online Software $\mu$ TCA



- use  **$\mu$ HAL / IPBUS** for communication with AMCs
- all HW calls contained in **HW Interface classes** -> **minimal change** when migrating to  $\mu$ TCA
- **maintain current API** for higher level software

