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Alice CTP upgrade

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The ALICE Central Trigger Processor (CTP) has been upgraded for LHC Run 2, amongst other motivations in order to improve the data-taking efficiency for the Transition Radiation Detector (TRD).
There is also a new CTP interaction record with a new DDL link , a 2 GB SODIMM DDR3 memory, an extension of the number of clusters and an extension of functionality for classes. The CTP switch has been incorporated directly onto the new LM0 board. A design proposal for an ALICE CTP upgrade for LHC Run 3 will also be presented. A part of development is a low latency high bandwidth interface in order to minimize an overall trigger latency

Summary

The ALICE CTP has been upgraded for LHC Run 2 needs, mainly through an additional trigger level “LM”, which will precede the L0 trigger and wil improve the data-taking efficiency for the Transition Radiation Detector (TRD). In addition there is a new DDL link for the CTP interaction record, a 1 GB snapshot memory and 1 GB random generator memory based on a 2 GB SODIMM DDR3 memory, an extension of the number of clusters and an extension of functionality for classes. The former external CTP switch has been incorporated directly into the FPGA logic of the new LM0 board.
Progress in the design for the upgrade of the ALICE CTP for LHC Run 3 will also be presented. The connection between the CTP boards is based on a custom link design which was tested on two boards populated with a Kintex-7 FPGA and a Samtec FireFly twinax cable (twelve differential links). General purpose IO pins, together with custom input/output logic have been used to obtain a lower latency than that obtainable from high-speed dedicated pins on the FPGA. One link is used to transfer the LHC clock and the other 11 links are used for data transfer at up to 13.75 Gbit/s. This bandwidth is sufficient for the requested maximum trigger data rate of 11.2 Gbit/s.

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