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The Level-0 Trigger Processor for the NA62 experiment

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In the NA62 experiment at CERN-SPS, the communication between detectors and the Lowest Level (L0) trigger processor is performed via ethernet packets, using the UDP protocol. The L0 trigger processor handles the signals from sub-detectors that take part to the trigger generation and, in order to chose the best solution, two different approaches have been implemented.
The first approach is fully based on an FPGA device while the second one joins an off-the-shelf PC to the FPGA.
The performance of the two systems will be discussed and compared.

Summary

The main purpose of the NA62 experiment at the CERN - SPS is to measure the branching ratio of the(ultra) rare decay $K^+ \to \pi^+ \nu\bar{\nu}$ with a precision of 10 % in order to verify the predictive power of the Standard Model. The expected branching ratio has been theoretically estimated to be of the order of 10^{-10} thus requiring a high intensity kaon beam.
The intense flux of particles requires a high-performance trigger and data acquisition system.

In particular, the lowest level (L0) trigger processor represents a crucial component in reducing the event rate. The incoming data rate is estimated to be ~ 10 MHz for most of the sub-detectors which will form the trigger, and after a first selection it should be reduced of a factor 10. The maximum latency admitted to take the decision at the level of L0 trigger is 1 ms.

NA62 adopts an innovative architecture to construct the L0-trigger. In fact, trigger information, namely time, topology, and physical quantities, are digitised by each sub-detector and then delivered to the trigger processor. Data are sent via Gigabit ethernet using the UDP protocol to an off-the-shelf development commercial board on which is mounted an FPGA module to acquire the information of the detector signals, and to route selected triggers to the Timing Trigger and Control (TTC) system of the experiment.

For the realisation of the trigger selection two different approaches were developed and will be presented and compared.

A first project is fully based on the FPGA, and the whole logic for data selection is hardware programmed, while the second one joins a commodity PC to the same tool.

In the latter case, data are immediately stored, via PCI-express, into the DDR memory of the PC, which performs the event selection.

The first approach is characterised by a fully real-time processing with guaranteed constant latency, but limitations appear in the limited FPGA available resources, concerning algorithm implementation and memory depth.
On the other hand, in the PC-based trigger processor, the implementation of complex algorithms is much simpler and any maintenance operation does not imply to re-configure the FPGA. Anyway, relying on a CPU, the system loses the full synchronisation inside L0 because the PC does not respond as a real-time device.

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