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Prototype active silicon sensor in LFoundry 150nm HV/HR-CMOS technology for ATLAS Inner Detector Upgrade

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The LHC Phase-II upgrade will lead to a significant increase in luminosity, which in turn will bring new challenges for the operation of the inner tracking detectors. A possible solution is to use active silicon sensors taking advantage of commercial HV/HR-CMOS technologies. Current ATLAS R&D programme is qualifying a few commercial technologies it terms of suitability for this task. During this talk a prototype designed in one of them (LFoundry 150nm process) will be discussed –the chip architecture will be described, including different pixel types incorporated into designed, followed by simulation and measurement results.

Summary

Following the advances of commercial semiconductor manufacturing technologies there has recently been an increased interest within experimental physics community in applying CMOS manufacturing processes to developing active silicon sensors. Possibility of applying high voltage bias combined with high resistivity substrate allows for reasonably large depletion of sensor and quick charge collection. Additionally first amplification and shaping stages can be implemented within the sensor itself. This makes such devices an interesting alternative for currently used passive sensors. Because ATLAS Inner Detector will be replaced by a purely silicon based one after Phase-II LHC upgrade (due to increased luminosity) a cost reduction coming from using a standard, large-volume CMOS production is also a strong argument in favour of proposed active sensors. Within ATLAS CMOS Pixel Collaboration a "CMOS demonstrator"initiative has started with the goal of evaluating the suitability of available HV/HR-CMOS processes for the HL-LHC environment. This talk describes a prototype fabricated in one of those technologies –LFoundry 150nm CMOS.

Chip size is 5mm $\times$ 5mm and pixel size is 33μm $\times$ 125μm, which allowed to use a matrix of 114 pixels $\times$ 24 pixel. Two versions of chip were developed differing by pixel architecture and biasing scheme. Additionally each of the versions is composed of few flavours of pixels, bringing total number of pixel variations to 15. Each pixel has a collection well and readout electronics (charge sensitive amplifier, comparator and digital circuitry for configuration). Although the final goal is to connect (via bump-bonding or gluing) this sensor chip to a digital readout ASIC (e.g. FEI4) for easier characterization this prototype provides a possibility of simple stand-alone readout and a wide range of pixel tuning options. Chip was fabricated on 2kΩcm wafer and measurements are on-going. First results show a good behaviour of chip (noise $\approx$150 e^-, uniform gain spread across the matrix) and are consistent with simulations.

During this talk the prototype will be described in detail starting with results of a TCAD simulations of the sensor behaviour, followed by an explanation of chip and pixel architectures. Chip simulation results will be presented together with the latest results from measurements. The talk will conclude with plans for the next prototype.

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