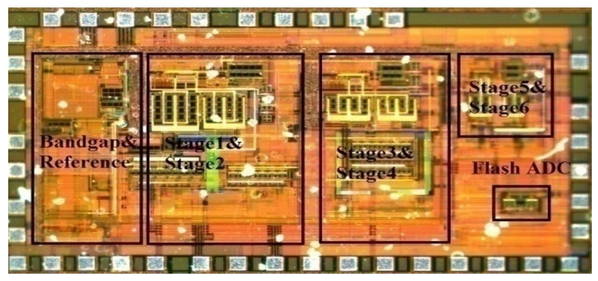
A 12-bit 60 MS/s 36 mW SHA-less Opamp-Sharing Pipeline ADC in 130nm CMOS

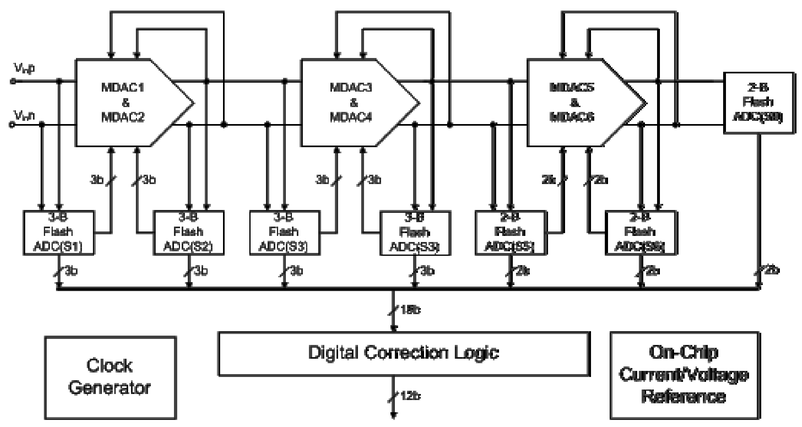
Xiaoke Wen,[a,] Jinghong Chen,[a,b] Yang You,[a] Yulang Feng,[b] Yuxuan Tang,[b] Zhiheng Zuo,[b] Bozorgmehr Vosooghi,[b] Datao Gong,[c] Tiankuan Liu,[c] and Jingbo Ye,[c]
[a] *Department of Electrical Engineering, Southern Methodist University, Dallas, TX 75275, USA*
[b] *Department of Electrical and Computer Engineering, University of Houston, Houston, TX 77004, USA*
[c] *Department of Physics, Southern Methodist University, Dallas, TX 75275, USA*
xwen@mail.smu.edu, jinghong@uh.edu

Introduction

- High-speed low-power and radiation-tolerant A/D converters are critical for the LHC upgrade and other collider developments.
- A 12-bit 60 MS/s low-power pipeline ADC is developed in a 0.13μm CMOS technology.
- To improve the pipeline ADC power efficiency, a SHA-less (without the use of sample-and-hold amplifier) front-end and a switch-embedded opamp-sharing MDAC with a three-phase non-overlapping clocking scheme is developed.
- The ADC achieves a maximum SNDR of 64.9 dB and a peak SFDR of 77.1 dB at 60 MS/s.
- The ADC occupies an area of 2.3 mm^2 and consumes 36 mW of power under a 1.2-V power supply.

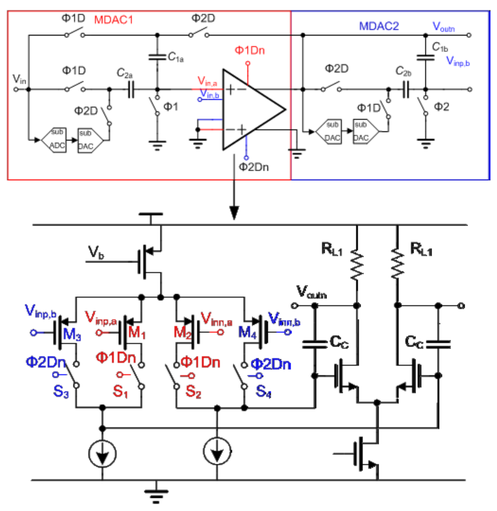


Architecture

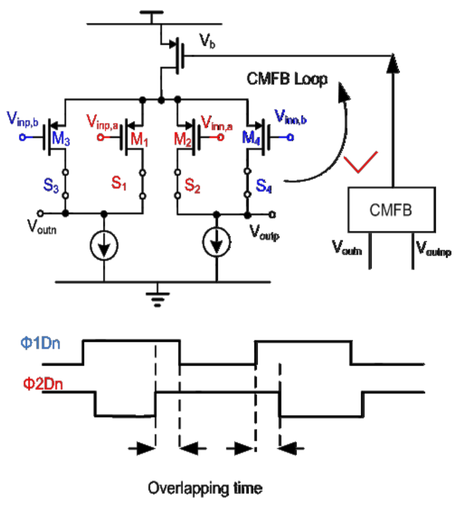


- Seven pipeline stages including four 2.5-bit per stage MDACs, two 1.5-bit per-stage MDACs and a 2-bit flash ADC.
- Two adjacent stages share an opamp based on the proposed dual-input opamp-sharing MDAC to improve the ADC power efficiency.

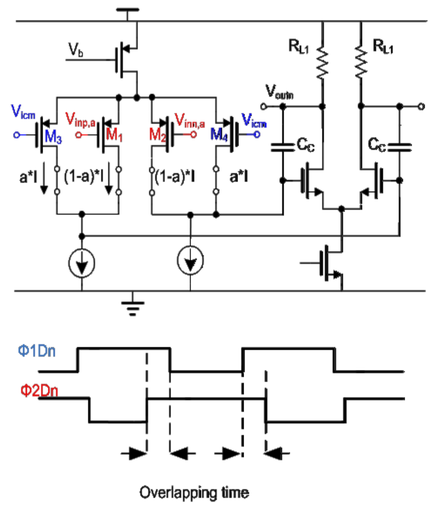
Opamp-Sharing MDAC



The proposed opamp-sharing MDAC

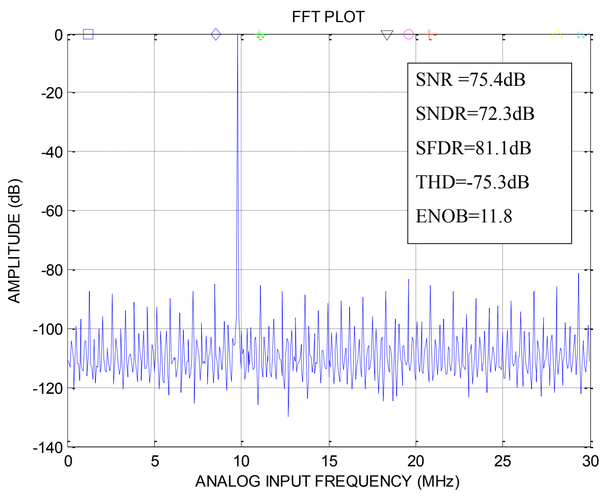


CMFB loop under the proposed overlapping clock

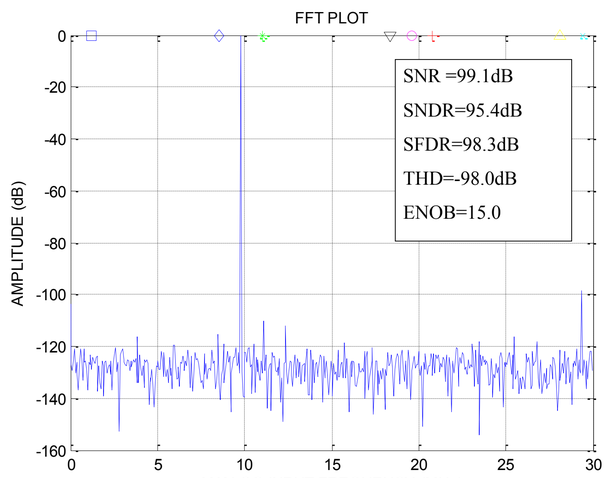


Differential signal under the proposed overlapping clock

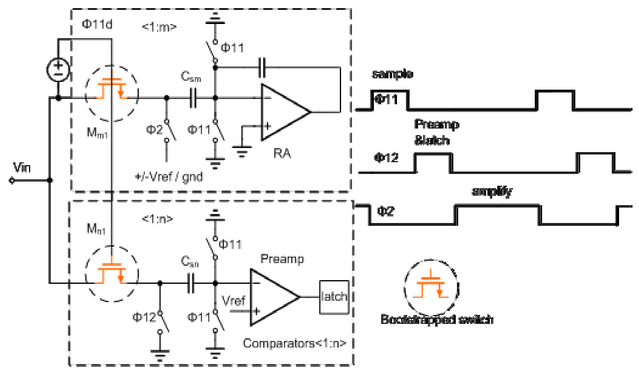
Performance Improvement



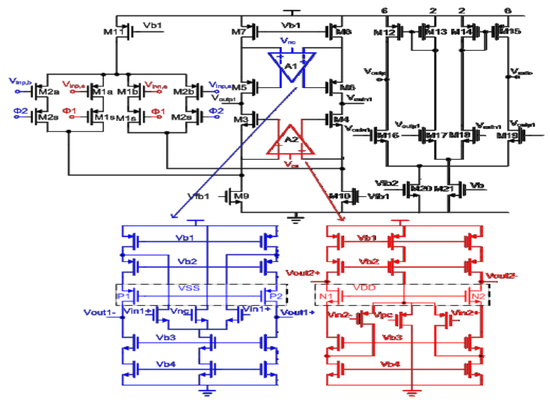
FFT of the 1st MDAC with non-overlapping clock



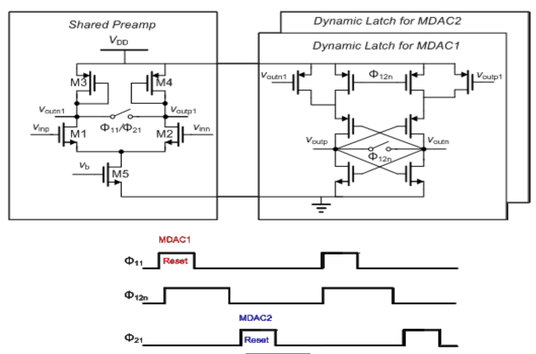
FFT of the 1st MDAC with the proposed overlapping clock



Input sampling network in MDAC1



Two-stage push-pull amplifier

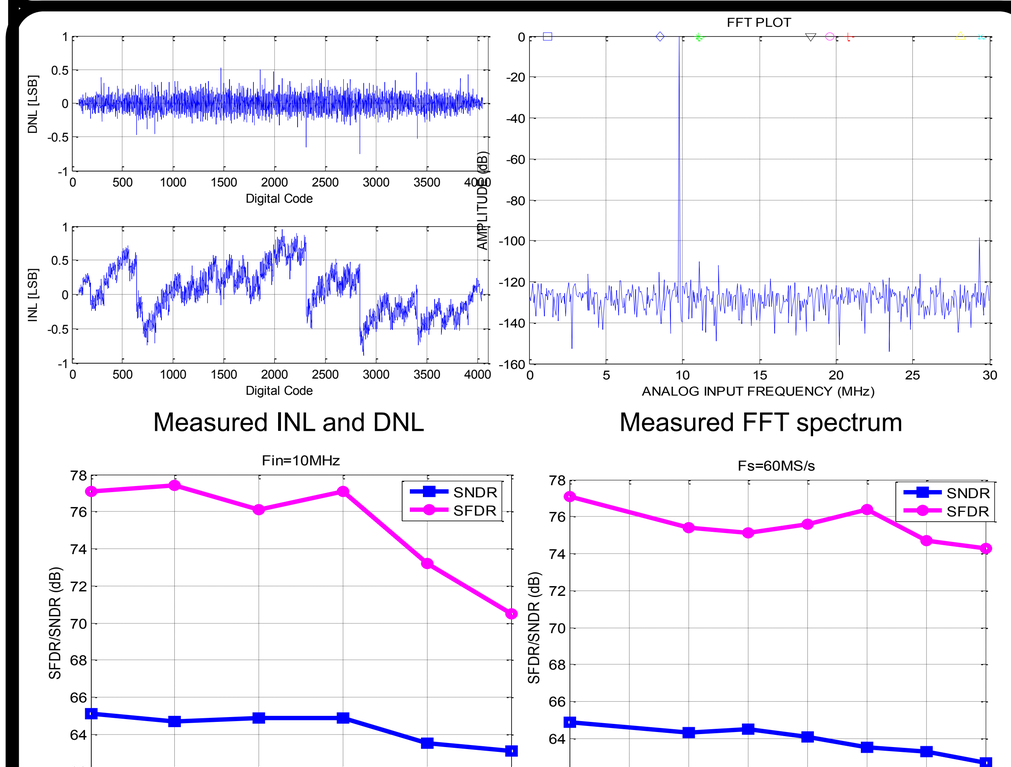


Sub-ADC comparator

ADC PERFORMANCE SUMMARY

Technology	0.13-μm CMOS
Conversion Rate	60 MS/s
SNDR	64.9 dB @10 MHz input 64.3 dB @30 MHz input 63.5 dB @60 MHz input
SFDR	77.1 dB @10 MHz input 75.4 dB @30 MHz input 76.4 dB @60 MHz input
DNL /INL	-0.7/+0.53 LSB / -0.9 /+0.97 LSB
Power Consumption	36 mW
FOM (P/2^ENOB/Fs)	0.42 pJ/step

- 0.13μm CMOS
- Conversion rate of 60 MS/s
- Maximum SNDR of 64.9 dB
- Peak SFDR of 77.1 dB
- Die area of 2.3 mm^2
- Power consumption of 36 mW under 1.2V supply



Measured INL and DNL

Measured FFT spectrum

Performance vs sampling frequency

Performance vs input frequency

PERFORMANCE COMPARISON

Ref	VDD (V)	Fs (MS/s)	SFDR (dB)	SNDR (dB)	Power (mW)	FOM1 (pJ/step)	FOM2 (pJ/step)
[1]	1.2	160	76	58.5	82	0.75	1.2
[2]	1.8	50	69.4	60.6	21.6	0.49	0.37
[3]	1.8	40	N/A	62	72	1.70	3.1
[4]	1.8	40	70	56.9	18	0.8	-
This work	1.2	60	77.1	64.9	36	0.42	0.26

Conclusion

- A 12-bit 60MS/s SHA-less pipeline ADC with a new switch-embedded opamp-sharing MDAC is designed in a 0.13μm CMOS technology.
- The opamp-sharing technique and the SHA-less front-end improve the ADC power efficiency.
- The pipeline ADC achieves an ENOB of 10.5 bits with a SFDR of 77dB at 60MS/s and consumes 36mW of power under 1.2V supply.

References

[1] Y. Kim et al, A 9.43-ENOB 160 MS/s 1.2-V 65-nm CMOS ADC based on multi-stage amplifiers, IEEE CICC'2009.
[2] K. Lee et al, A 12b 50 MS/s 21.6 mW 0.18-μm CMOS ADC maximally sharing capacitors and opamps, IEEE Transactions Circuits and Systems I, Sept. 2011.
[3] K.Chandrashekar et al, A 20-MS/s to 40-MS/s reconfigurable pipeline ADC implemented with parallel OTA scaling, IEEE Transactions Circuits and Systems II, Aug. 2010.
[4] S. Ryu et al, A 10b 50 MS/s pipelined ADC with opamp current reuse, IEEE ISSCC'2005

TWEPP 2015 - Topical Workshop on Electronics for Particle Physics,
September 28 - October 2, 2015, Instituto Superior Técnico, Lisbon, Portugal