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A 12-bit 60-MS/s 36-mW SHA-less Opamp-Sharing Pipeline ADC in 130nm CMOS

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This paper presents a 12-bit 60-MS/s SHA-less opamp-sharing pipeline analog-to-digital converter implemented in a 0.13-µm CMOS technology. A switch-embedded dual-input current-reused operational transconductance amplifier with an overlapping two-phase clocking scheme is proposed to achieve low power and eliminate memory effects. The ADC achieves a signal-to-noise and distortion ratio of 64.9 dB and a spurious-free dynamic range of 77.1 dB at 60 MS/s. It occupies 2.3 mm2 area and consumes 36 mW power under a 1.2-V supply.

Summary

The development of high-speed, low-power, radiation-tolerant analog-to-digital data converter is critical for the LHC upgrade as well as other collider detector developments. Among various ADC structures, the pipeline ADC offers a good tradeoff among speed, resolution and power consumption and is particularly suitable for medium- to high-speed and high-resolution applications. The pipeline ADC, however, often consumes a large amount of power due to the large number of opamps used in the sample-and-hold amplifier (SHA) and the multiplying-DACs (MDACs).

This paper proposes a switch-embedded dual-input opamp-sharing MDAC to reduce the pipeline ADC power consumption without sacrificing its performance. The proposed opamp-sharing technique utilizes a dual-PMOS differential input stage controlled by a two-overlapping clock to eliminate the memory effect and minimize the crosstalk between adjacent pipeline stages. Meanwhile, due to the use of the overlapping clocking scheme the switch turn-on delay can be avoided, which is desired in low-voltage and high-speed pipeline ADC designs. To further reduce the power consumption, the front-end sample-and-hold amplifier is eliminated and a three-phase non-overlapping clocking scheme is adopted in the first pipeline stage to reduce the preamplifier and the residue amplifier speed requirements.

The proposed 12-bit 60 MS/s pipeline ADC has seven pipeline stages including four 2.5-bit per stage MDACs, two 1.5-bit per-stage MDACs and a 2-bit flash ADC. It also has a digital correction logic block, a reference buffer and a clock generator. Two-stage opamps with gain-boosting are adopted in MDAC1 to MDAC4 to achieve high gain and large swing, while MDAC5 and MDAC6 use regular two-stage opamps to save the power consumption. Two adjacent stages share an opamp based on the proposed dual-input opamp-sharing MDAC to improve the ADC power efficiency.

The ADC is designed and fabricated in a 0.13-µm CMOS technology. It occupies an area of 2.3 mm2 and consumes 42 mW of power at 60 MS/s sampling rate under a 1.2-V power supply, including the power consumption of the bandgap and biasing circuits as well as voltage buffers, which is about 6 mW. The measured signal-to-noise and distortion ratio (SNDR) and peak spurious-free dynamic range (SFDR) are 64.9 dB (ENOB = 10.49) and 77.1 dB, respectively, and achieved a figure-of-merit (FOM) of 0.42 pJ/step. Compared with recently published 10 to 12-bit and a few tens of MS/s pipeline ADCs, the prototyped SHA-less opamp-sharing pipeline ADC with the proposed switch-embedded dual-input OTA achieves the best FOM.

The ADC will be irradiated under X-ray with a total dose over 10 Mrad for rad-hard testing. The radiation testing results will be presented at the conference.

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