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Development on CMOS MAPS devices for the ATLAS Phase-II Strip Tracker Upgrade

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ATLAS is currently studying the use of CMOS MAPS devices as a replacement for the baseline silicon strip sensors for the Phase-II Strip Tracker Upgrade. One of the key aspects is to establish whether the radiation hardness is suitable for the HL-LHC environment. Two different technologies are being studied: High-Voltage CMOS and High-Resistivity CMOS. Several test chips have already been manufactured. We present the latest results from non-irradiated and irradiated sensors including test beam results and give an outlook on the next steps.

Summary

ATLAS is currently studying the use of CMOS MAPS devices as a replacement for the baseline silicon strip sensors for the Phase-II Strip Tracker Upgrade. In order to minimize the impact on the overall tracker design, a CMOS alternative sensor has to result in minimal changes to the rest of the detector. Hence ATLAS is investigating devices with long pixels which are grouped to form a virtual strip with binary-encoded z-information. Key requirements are to establish whether the radiation hardness is suitable for the HL-LHC environment, that the charge collection speed is sufficient for 25 ns bunch crossing operation, and whether the encoded z-hit design can be compatible with full-reticule size sensors.

Several test chips have been submitted using two different CMOS technologies. The AMS HV-CMOS 350 is a special process, which makes it possible to bias the sensor with up to 120 V, while the TowerJazz 180 nm HR-CMOS process uses a high resistivity epitaxial layer to speed up the charge collection. Several groups have taken part in understanding the performance of these sensors including charge collection, output signal timing, gain and noise. We present these results and also results from the irradiation campaigns with photons, neutrons and protons, which strongly support the radiation tolerance of these devices to radiation dose of the HL-LHC (60 Mrad and 2x10ˆ15 neq/cmˆ2). We also show first test beam results of these devices .

Our next chip features a full-reticle length sensor. It is designed for prototyping the readout architecture and to assess large-chip effects, such as common mode noise. The hit encoding engine is capable of reading out up to 8 hits from a pre-defined region. The hits are then transferred for off-sensor readout via 320 MHz bus that runs at 8 times the bunch crossing frequency. Placement of the comparators and the bulk wafer resistivity will be varied to optimize the performance.

To conclude we give an overview of the upcoming plans for ATLAS strip CMOS detectors, including a detailed description of the first large-size chip which is going to be available for fall 2015.

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