Contribution ID: **205** Type: **Poster**

SALT, a dedicated readout chip for strip detectors in the LHCb Upgrade experiment

Wednesday 30 September 2015 16:39 (1 minute)

Silicon strip detectors in the upgraded Tracker of LHCb experiment will require a new readout 128-channel ASIC called SALT. It will extract and digitise analogue signals from the sensor, perform digital processing and transmit serial output data. SALT is designed in CMOS 130˜nm process and uses a novel architecture comprising of analog front-end and ultra-low power (<0.5˜mW) fast (40˜MSps) sampling 6-bit ADC in each channel. A prototype of first 8-channel version of SALT chip, comprising all important functionalities, was submitted. Its design and possibly first tests results will be presented.

Summary

The Large Hadron Collider beauty (LHCb) detector, operating at the Large Hadron Collider (LHC), has finished its Run I period, accumulating a large amount of valuable data. Despite its superb performance, it is clear that the LHCb experiment is statistically limited by readout electronics and data acquisition architecture, allowing it to collect data at the top rate of 1.1 MHz at the instantaneous luminosity close to $4{\cdot}10^{32}$ cm^{-2}s^{-1}. The LHC machine is already capable of delivering more than one order of magnitude higher luminosity than presently used by the LHCb detector. This fact led the LHCb Collaboration to prepare a proposal of an upgrade of the LHCb spectrometer that would allow to exploit higher luminosities (up to $2{\cdot}10^{33}$).
To achieve this goal various detectors will need a new faster front-end electronics with the read-out running at the bunch-crossing rate of 40 MHz.

Silicon strip detectors in the upgraded Tracker of LHCb experiment will require a new readout ASIC. A project of a 128-channel ASIC called SALT (Silicon ASIC for LHCb Tracking), is ongoing. SALT extracts and digitises analogue signals from the sensor, performs digital processing and transmits a serial output data. It is designed in CMOS 130 nm technology, and uses a novel architecture comprising an analog front-end and an ultra-low power (<0.5˜mW) fast (40˜MSps) sampling 6-bit ADC in each channel. The front-end comprises a charge preamplifier and a fast shaper (T_{peak}=25ns and fast recovery) required to distinguish between the LHC bunch crossings at 40˜MHz. To achieve this, a specific non-standard shaper is required. The front-end should work with sensor capacitances between 5–35˜pF. Ultra-low power (<1˜mW) DLL is used to control precisely the ADC sampling phase.

Digitised data from each ADC channel are processed in a DSP block which first subtracts pedestals and calculates mean common mode (MCM), as an average over channels without signal. The MCM is also subtracted in each channels. The last DSP step is zero suppression (ZS) compression. After ZS the data are buffered in SRAM, then the packet is formed and sent to DAQ via a number of serial DDR e-links.
Ultra-low power (<1˜mW) PLL is used in data serialization and fast data transmission circuitry.

Prototypes of all important SALT blocks, i.e. 8-channel analog front-end, 8-channel 6-bit ADC, PLL, DLL and, SLVS I/O were designed in CMOS 130˜nm, fabricated and tested, showing very good performance. The design and the results of measurements of these blocks will be presented.
A prototype of first 8-channel version of SALT chip, comprising all important functionalities, was submitted to fabrication. Its design and possibly first tests results will be also presented.

Primary author: SWIENTEK, Krzysztof Piotr (AGH University of Science and Technology (PL))

Presenter: SWIENTEK, Krzysztof Piotr (AGH University of Science and Technology (PL))

Session Classification: Poster

Track Classification: ASICs