FE65_P2: Prototype Pixel Readout Chip in 65nm for HL-LHC Upgrades

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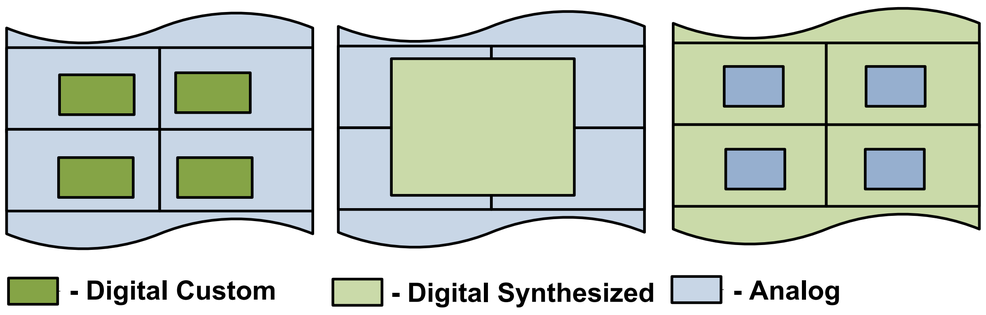
FE65_P2 and RD53

- Work done in the context of RD53 Collaboration (cern.ch/RD53)
- RD53 was established to design the next generation pixel readout chip for ATLAS and CMS Phase 2 upgrades
- FE65_P2 is a test chip with several goals:
  1) Validate the concept of "analog islands in a digital sea" (see below)
  2) Test a 50µm x 50µm pixel matrix including bump-bonding pads
     - Plan to bump bond chips to matching test sensors
  3) Validate substrate isolation strategy. Both analog and digital isolated.
  4) Exercise digital top level flow for this kind of design
  5) Measure performance vs. radiation dose

Analog Islands in a Digital Sea

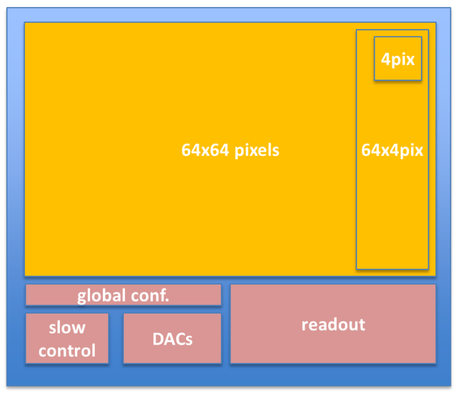


Traditional Design
- Make 1 pixel
- Step and Repeat identical copies
- Custom made digital

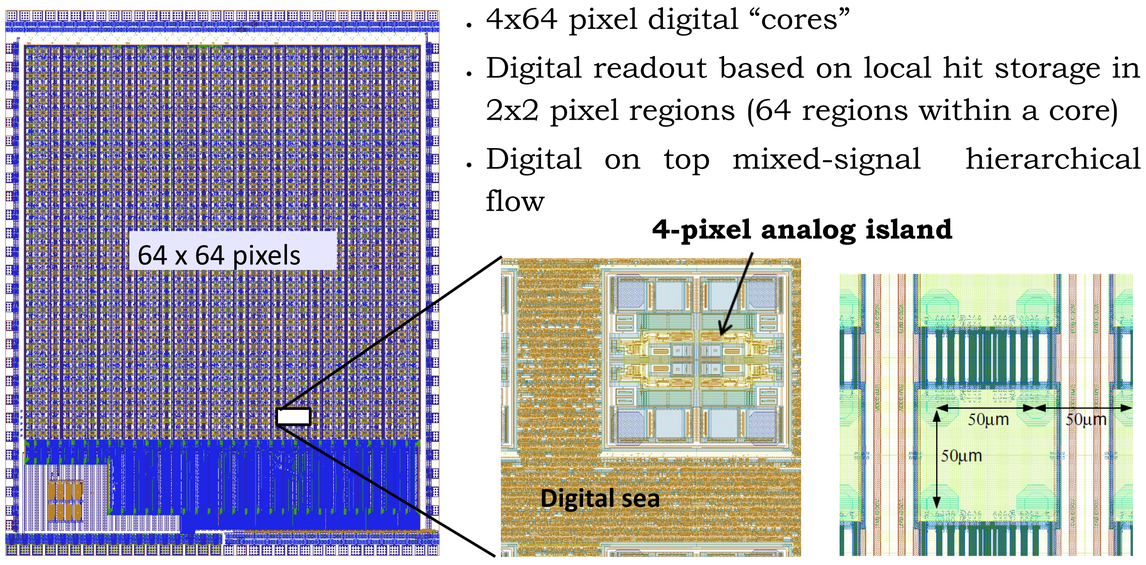
More Recently
- Make few-pixel region
- Step and Repeat identical copies
- Synthesized digital

New Approach
- Synthesized digital "core" containing a large number of analog pixels (256 in FE65P2)

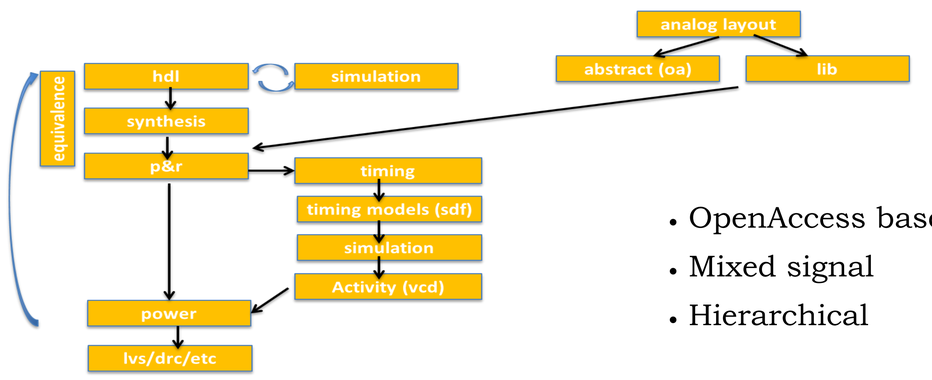
Top Design



- 65nm CMOS technology
- 3.5mm x 4.4mm
- 64x64 pixels with 50µm pitch square grid bump pattern
- Analog organized in 4-pixel "islands"
- Column-based distribution of analog biases and power
- On-chip DACs for all biases
- 4x64 pixel digital "cores"
- Digital readout based on local hit storage in 2x2 pixel regions (64 regions within a core)
- Digital on top mixed-signal hierarchical flow

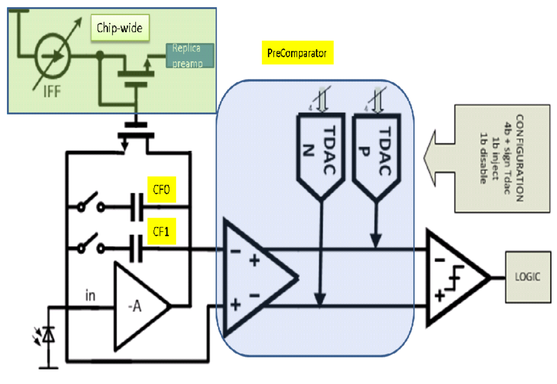


Design Flow

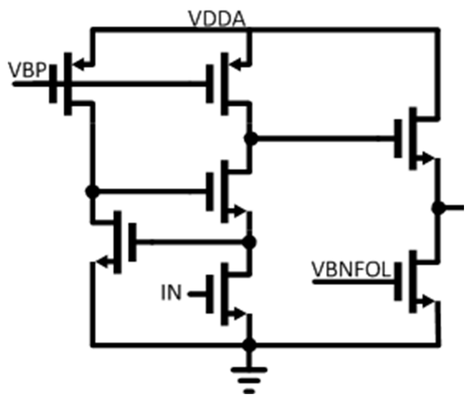


- OpenAccess based
- Mixed signal
- Hierarchical

Analog Pixel

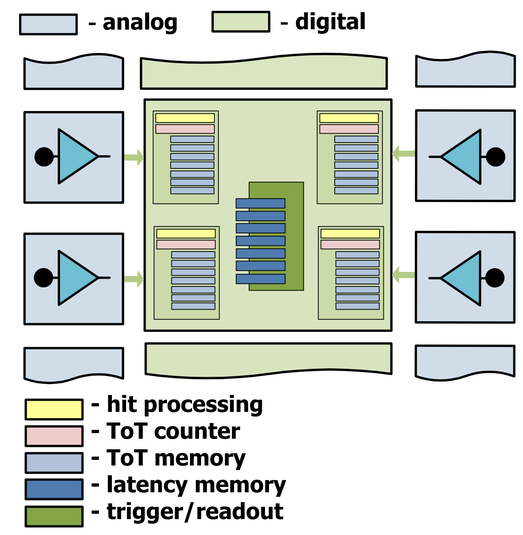


- No memory latches, flip-flops, or counters here
- Configuration comes from digital
- ADC function (ToT) is in digital part
- Continuous reset (current source) integrator first stage with adjustable gain
- DC-coupled "pre comparator" stage with differential output to classic comparator

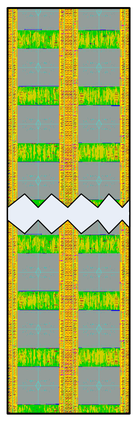


- Threshold adjusted by unbalancing differential output
- Cascode architecture of integrator amplifier
- Designed for 500e- threshold operation with 5uA/pixel current consumption at 50fF detector load and 5uA leakage current.
- Designed to operate up to 100fF load and 10uA leakage (resulting in higher threshold and/or higher power)

Digital Core



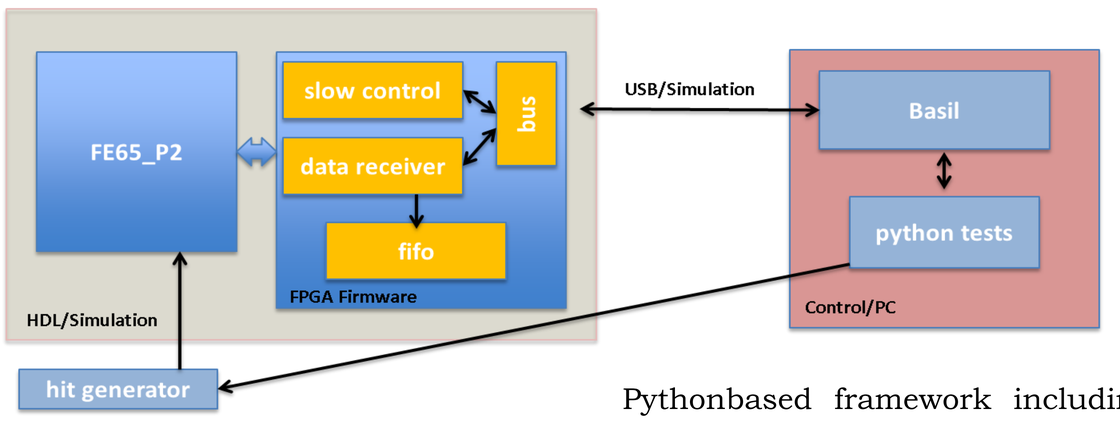
- 4 pixels per region
- 7 Latency memories (stores up to 7 hit arrival times for the region) allows to reach 10µs latency with 50kHz/pixel hit rate with <1% loss
- 4-bit ToT (Time over Threshold) counting per pixel
- Code adapted from FE-I4
- Note 7 latency buffers compared to 5 in FE-I4, but 1/5 the area! (Thanks Moore's Law)
- Using latches to store distributed counter value, instead of individual counters as in FE-I4



- Synthesized 4x64 pixel "core"
- Density 85%
- Power 5.5µW/pixel at
- 2GHz/cm² hit rate and
- 1MHz trigger rate

trigger latency [µs]	hit rate [GHz/cm²]	memory locations	ineffiency [%]	avr. mem occupancy
10	2	7	**0.2**	1.4
10	3	7	**2.3**	1.9
10	3	8	**0.9**	1.9
20	2	7	**6.4**	2.3
20	2	9	**1.1**	2.4

Test Bench




```
self.chip['global_conf']['InjEnLd'] = 0
self.chip['global_conf']['TDacLd'] = 0
self.chip['global_conf']['PixConfLd'] = 0
self.chip['global_conf'].set_wait(200)
self.chip.write_global() #send some test hit

while not self.chip['trigger'].is_done():
    pass

print 'fifo_size', self.chip['fifo'].get_fifo_size()
data = self.chip['fifo'].get_data()
```

Pythonbased framework including full FPGA readout system.

Test bench software can then be run on physical test system, so that exact same tests can be performed on real chip and model used for functional verification of digital design.