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# FE65_P2: Prototype Pixel Readout Chip in 65nm for HL-LHC Upgrades

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The LHC Phase-II upgrade will lead to a significant increase in luminosity, which will bring new challenges for the operation of the inner tracking detectors. To handle those requirements, a new pixel readout chip is being developed, within the RD53 collaboration taking advantage of the reduced feature size of 65nm technology. A 64x64 pixels (50 um pitch) prototype chip, introducing the concept of analog “islands” surrounded by a “sea” of digital gates, is being presented. The new analog frontend, isolation strategy, readout architecture and digital on top mixed-signal design flow will be discussed in detail.

## Summary

The largest and most technically demanding environment for a pixel detector is that of the LHC operation planned after 2024 (LHC Phase 2). Extremely high luminosity and particle rates pose great challenges to pixel detectors to resolve tracks in jets, resulting in much higher hit rates (1-2 GHz/cm2), high trigger rates (1-2 MHz), and longer trigger delay times (10us latency). The LHC Phase 2 Upgrade introduces unprecedented radiation levels in terms of ionizing dose (>5 MGy) and particle fluence (>1016 neq/cm2).

A new hybrid pixel readout integrated circuit is being developed by the RD53 collaboration to fulfil the requirements of LHC Phase 2. The test chip described in this talk, called FE65_P2, is part of the RD53 activities. FE65_P2 has been developed in 65nm CMOS technology, measures 3.5x4.4 mm^2 and includes a 64x64 pixels array with bump pads on a 50um x 50um grid. It includes a small-area low-power charge-sensitive frontend with comparator and threshold tuning circuit achieving (in simulation) 1000e- in-time threshold and 50e- noise. A new mixed-signal isolation strategy based on small analogue islands surrounded by a sea of digital gates has been developed which incorporates optimized power and bias signal distribution to minimize coupling and achieve low threshold. A digital readout based on local regional hit recording (>2GHz/s/cm2) provides hit storage (up to 10us), triggering and readout with 25ns time resolution, and 4-bit charge information. The prototype includes, on-chip biasing circuit, simple serial programming interface and output serial link allowing continuous triggering and data taking. The chip has been assembled in a digital on top mixed-signal hierarchical flow. Using digital tools and methodologies allowed fast iterative development and usage of advanced verification tools for signal integrity, power integrity and timing. A simple python-based test-bench that incorporates full readout and final test software has been used for functional verification, structured in such a way that the same code can be later run on an FPGA for testing real devices.
During this talk the test chip design will be described in detail starting with simulation results, followed by an explanation of chip and pixel architectures and design flow. First measurement results are expected in time for the workshop. Results from this test chip will inform the RD53 chip design regarding isolation strategy, low threshold performance, analog/digital integration and design flow. RD53 plans to submit a first large format prototype (wafer run) in 2016.

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