Comparison of two fast, ultra-low power 10-bit SAR ADCs in CMOS 130 nm A and B technologies

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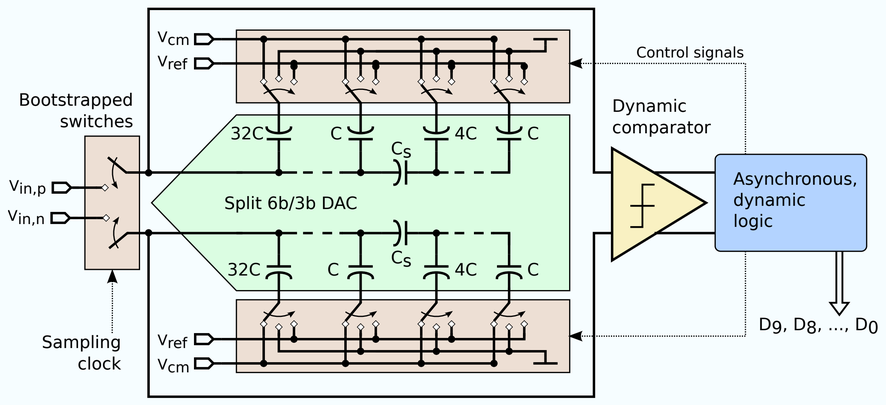
Design

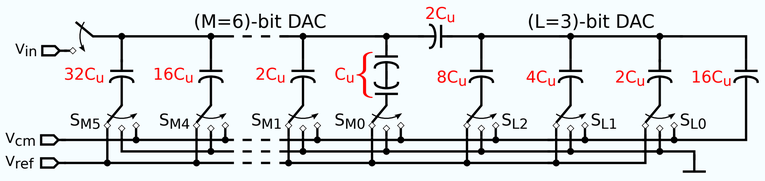


Main features:

- 10-bit resolution
- 40 MSps maximum sampling rate
- merge capacitor switching (MCS) scheme
- capacitive DAC with 6b/3b split
- dynamic comparator
- dynamic asynchronous logic
- bootstrapped input switches

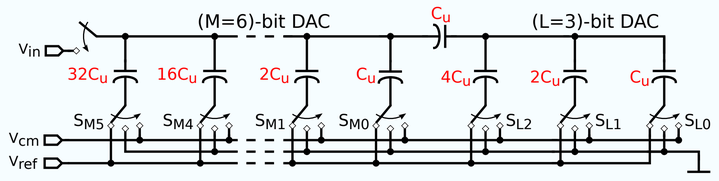
Minimal unit capacitance C_u for M-bit / L-bit split DAC optimized for best matching.

CMOS 130 nm process A



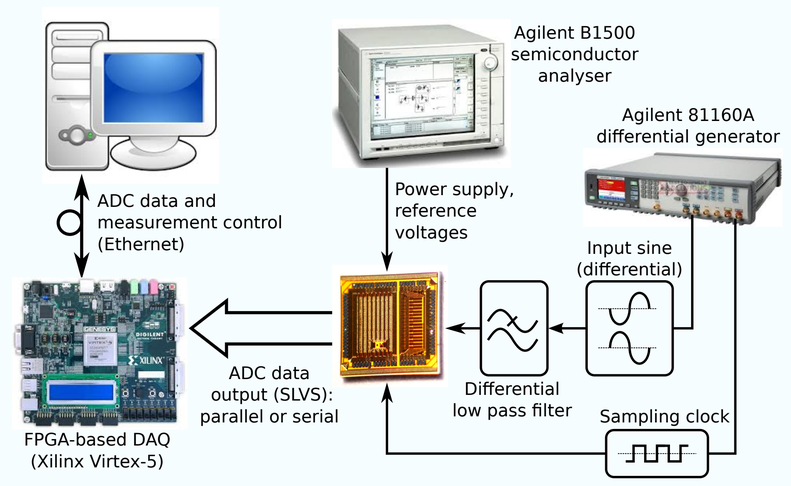
- capacitance density K_c=2.05 fF/µm^2
- matching parameter K_σ=4.12 %·µm
- technology limit C≥60 fF
- used effective C_u=40 fF
- total input capacitance = 2.86 pF

CMOS 130 nm process B

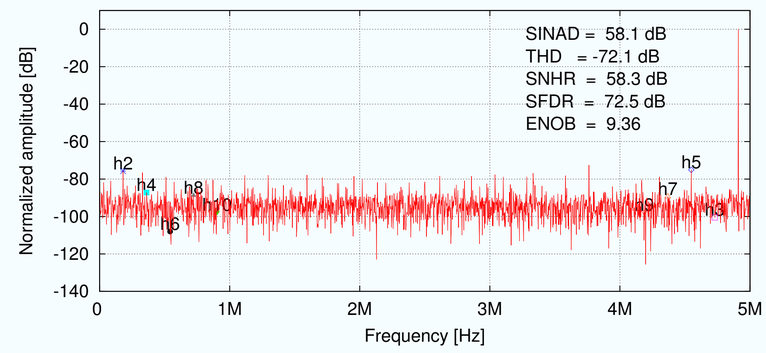


- capacitance density K_c=1.55 fF/µm^2
- matching parameter K_σ ∼1.2 %·µm
- technology limit C≥26 fF
- used effective C_u=26 fF
- total input capacitance = 1.68 pF

Measurement setup



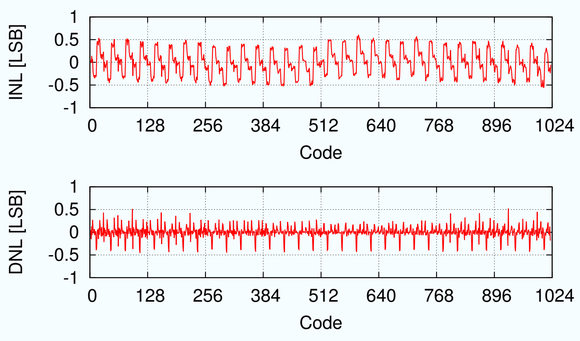
Exemplary spectrum for 10 MSps and Nyquist input frequency. Dynamic parameters obtained from DFT of output samples (IEEE Std 1241-2000).



Static results

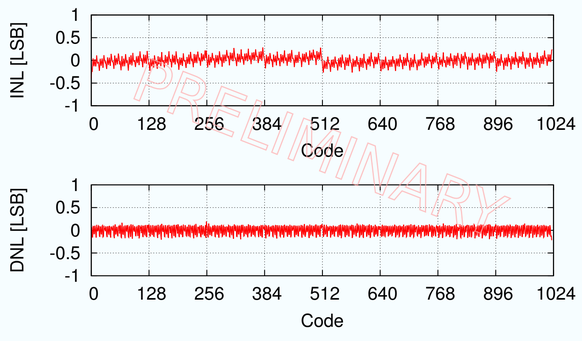
Exemplary static results at 10 MSps

CMOS 130 nm process A



Very good INL, DNL $\lesssim$ 0.5 LSB

CMOS 130 nm process B

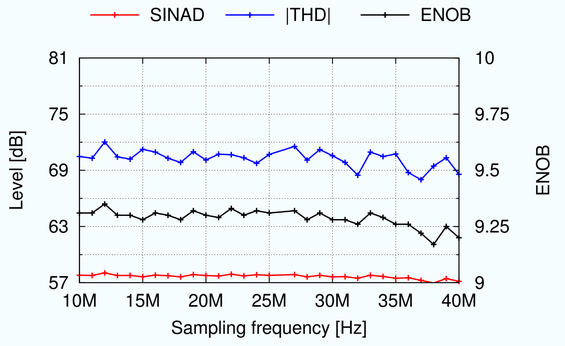


Excellent INL, DNL < 0.3 LSB

Dynamic results

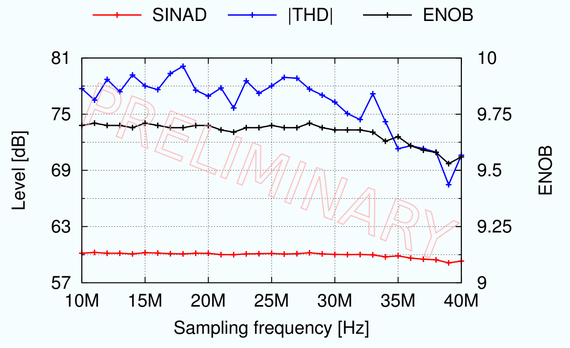
Dynamic parameters versus sampling rate at 0.1 Nyquist input frequency

CMOS 130 nm process A



Very good ENOB ∼ (9.2 – 9.3)

CMOS 130 nm process B

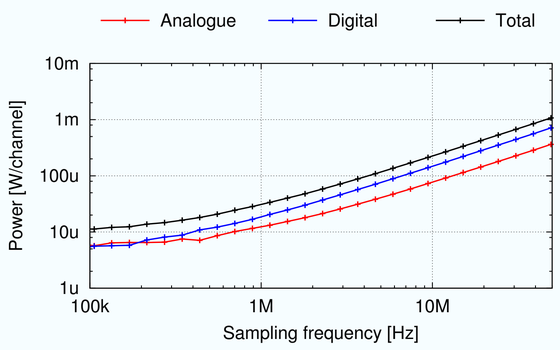


Excellent ENOB ∼ (9.6 – 9.7)

Power consumption

ADC power consumption versus sampling rate

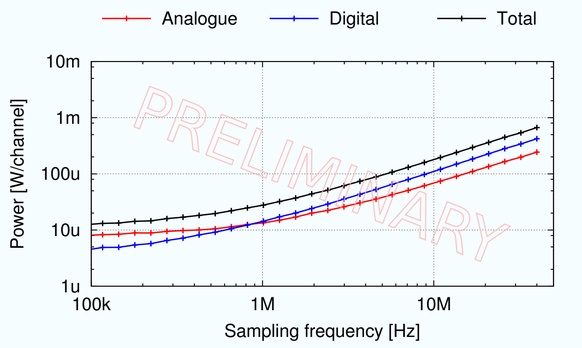
CMOS 130 nm process A



Power consumption at 40 MSps
880 µW/channel

Leakage negligible since thick-oxide decoupling devices were used

CMOS 130 nm process B



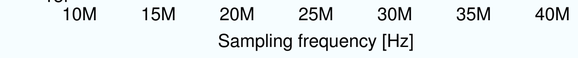
Power consumption at 40 MSps
660 µW/channel

Constant leakage of 72 µW/channel, due to thin-oxide decoupling devices, subtracted from measurement results

Figure Of Merit

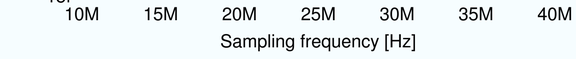
FOM (at 0.1 Nyquist input) versus sampling rate

CMOS 130 nm process A



FOM ∼ 35 fJ/conv. – among the best State of the Art[a]

CMOS 130 nm process B



FOM ∼ 22 fJ/conv. – the best ever published[a]

[a]For similar specifications and technology, to authors knowledge.

Conclusions

Both ADCs give excellent Figures of Merit, the second one the best ever published (to authors knowledge) for CMOS 130 nm and similar specification

- Excellent performance, power scalable with frequency, for both ADCs up to 40 MSps
- Ultra-low power consumption in both processes, in process B reduced by 33 %
- Excellent effective resolution and linearity in process B and very good ones in process A
- Matching in process B substantially better than in process A → INL, DNL significantly improved even at lower unit capacitance C_u
- Thin-oxide decoupling devices were used in process B – substantially higher leakage in process B – need to be replaced by thick-oxide devices, similarly as in process A

Acknowledgements

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