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Comparison of two fast, ultra-low power 10-bit SAR ADCs in CMOS 130 nm A and B technologies

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The design and the preliminary measurements results of two ultra-low power 10-bit Successive Approximation Register (SAR) Analog to Digital converters (ADC) fabricated in two CMOS 130˜nm technologies (process A and B) are presented and compared. Both prototypes are fully functional achieving a good linearity, with INL and DNL below 1˜LSB, and a good effective resolution, with ENOB above 9 bits. The power consumption of both prototypes is below 1˜mW at nominal sampling rate of 40 MS/s. For both ADCs the power consumption scales linearly with sampling rate.

Summary

Fast and good resolution digitization of pulses from ionizing particles is essential for the modern and future detector systems of particle physics experiments. Multichannel readout systems require a power and area-efficient analog to digital converters (ADC), particularly in the context of continuously growing number and density of readout channels. The Successive Approximation Register (SAR) ADC architecture allows to meet these two fundamental requirements offering additionally other features highly requested in readout systems, such as power pulsing and the possibility of avoiding a high frequency clock tree.

In this work we discuss the development of two prototypes of 10-bit SAR ADC for readout system of the luminosity detector at the future linear collider (ILC/CLIC). We have designed a prototype ADC in two 130 nm CMOS technologies A and B. The ADC layouts were prepared to target a multichannel implementation.

A fully differential architecture was chosen for the ADC design. It contains a pair of bootstrapped switches, a pair of capacitive Digital to Analog converters(DAC) which also perform the sample and hold task, a dynamic comparator, and an asynchronous dynamic control logic. Almost identical design, despite of technology differences in minimum capacitance for the DAC array, was developed in both processes in order to allow their comparison. To lower the power consumption the Merge Capacitor Switching (MCS) scheme was used in the DAC allowing to reduce its switching energy up to 93˜\%, compared to the conventional SAR ADC switching scheme. The dynamic architecture was chosen both for the comparator and the control logic to eliminate a static power consumption and to obtain the power pulsing feature without any additional effort. The asynchronous control logic requires only a sampling clock avoiding a fast clock distribution across the whole ASIC, for bit cycling. The ADC layout occupies 146 um x 600 um and 80
um x 560 um in process A and B respectively. The preliminary static measurements of ASICs fabricated in process A and B show a good linearity, with both DNL and INL below one. Also the dynamic measurements of both prototypes show a good ENOB above 9 bits. The maximum sampling rate of the tested prototypes is around 40 MS/s in agreement with simulations. For the default 1.2 V power supply and at 40 MHz sampling frequency the measured power consumption is below 1 mW for both the A and B processes. Such ultra-low power performance corresponds to the Figure of Merit of around 35 fJ for the best prototype, what places the design within the State of the Art designs. The sampling frequency is variable up to above 40 MHz and the power consumption scales linearly with it. The detailed comparison of all measured parameters for ADC prototypes fabricated in the CMOS 130 nm process A and B will be given in this talk.

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