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Common Readout Unit (CRU) –A new readout architecture for ALICE experiment

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To cope up with the increasing luminosity of the Large Hadron Collider (LHC) at CERN, the ALICE experiment is planning for a major upgrade of the detectors, which is at present foreseen to start in 2018. The high interaction rate and the large event size results in an experimental data flow traffic of about 1 TB/s from the detectors to the on-line computing system. A dedicated Common Readout Unit (CRU) is proposed for data concentration, multiplexing and trigger distribution. We discuss the firmware design and implementation of CRU on the LHCb PCIe40 board.

Summary

The ALICE experiment is going for a major upgrade of the detectors, readout electronics and data acquisition systems in order to be ready for high-rate data taking for the Pb-Pb, pp and p-Pb collisions at the LHC. For Pb-Pb collisions, the present data-taking rate of 500Hz is anticipated to be 50kHz. The data rate for pp and p-Pb collisions will be of few hundred kHz. The CRU is envisaged as the interface between the front-end electronics, trigger, detector control system (DCS) as well as the online farm. The CRU will be located in the counting room, and thus allows the use of non-radiation hardened, commercial electronics with reconfigurable technology.

The major functionalities of the CRU are to unpack the raw data received from the front end detector links, perform specific detector tasks like sorting, clustering, compressing or time slicing; and then finally to forward the data to the online-offline(O2) computing system in a specified format. The CRU also plays a pivotal role in trigger and timing information distribution received from the Central Trigger Processor(CTP). The CRU is interfaced with the Detector side using CERN proprietary GBT (Gigabit Transceiver) interface link. For interfacing to the online-offline computing via the Detector Data Link version 3(DDL3), the PCIe Gen 3 link standard is chosen, which eases possible future up-grades.

The CRU firmware will be using PCIe40 hardware. The PCIe40 is a custom board based on ultra-low power 20 nm Altera Arria 10 FPGA solution, also used by LHCb as their common read-out board. For the development a joint venture between LHCb and ALICE has been formed. In extended configuration, the board supports 48 bidirectional GBT links and PCIe Gen3 x16 lanes with a bidirectional 10 Gigabit link.

As the CRU is commutated by multiple interface links, for each link there is a specific frame format and protocol layer. Multiple data packet format specifications need to be defined. The upgraded ALICE trigger system supports two types of detector read-out architectures, triggered read-out and continuous read-out. For non-upgraded sub-systems triggered readout will be used. Those detectors will be read out whenever they are not busy. The upgraded detectors with continuous read-out will use non-physics heartbeat trigger for time frame demarcation at the online system. This highest priority heartbeat trigger scheduled by CTP allows fragmentation of the data stream for event building. Detailed discussions of each interface link topology and its implementations are mentioned. Throughput measurement and performance measurements including eye diagrams, and bit error rates for each interface link are presented. A special section on framework architecture of high speed data concentration, data management, data queue and data flow topology is included. Different test setups used in the process of evolution of the firmware will also be discussed. The CRU specifications are

compared with similar boards already in operation or under design like ALICE RCU, RCU2 and LHCb-Tell40 boards.

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