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A fast multichannel, ultra-low power 10-bit ADC for readout of future particle physics detectors

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The architecture, design, and preliminary measurements of multichannel 10-bit SAR ADC developed in CMOS 130˜nm technology for readout systems of particle physics experiments, are presented. Other design issues like data serialization and high speed transmission are also discussed. The results of static and dynamic measurements, power consumption, crosstalk, etc., performed in multichannel operation of the ADC prototype are discussed. The measurements show a good effective resolution with ENOB above 9 bits, together with a good static linearity. The power consumption scales linearly with sampling frequency and at nominal sampling rate of 40MS/s it is below 1mW/channel.

Summary

Future high energy physics experiments, like the ones at LHC or ILC/CLIC, set more and more challenges for detector readout systems. One of such challenges, which have not yet been solved, is to develop a multichannel readout system containing a fast low power ADC in each channel. This would allow to use a very simple and elegant readout architecture. By now the bottleneck in solving this issue has been an excessively high power consumption of the ADC.

We have developed a multichannel, ultra-low power fast sampling 10-bit SAR ADC. The ASIC was designed and fabricated in 130 nm CMOS technology. The Successive Approximation Register (SAR) architecture allows to obtain a power and area-efficient ADC, highly required by multichannel readout systems for modern and future detectors of particle physics experiments. The use of asynchronous logic results in additional qualities such as power pulsing and absence of fast clock distribution circuitry.

The serializer block provides various modes of data serialization, including a test mode with a readout of selected channel (parallel output bits), a partial serialization mode in which each ADC channel is serialized into dedicated data link and a full serialization mode in which all channels are serialized into single output. The data serialization, based on ultra-low power internal PLL together with a high speed transmission through a fast SLVS I/O differential interface, allows to simplify the interface between the multichannel ADC ASIC and the back-end electronics. A dedicated subcircuits such as fast SLVS differential driver and an ultra-low power ($<$1 mW) PLL were developed. The PLL was designed to generate clock in wide frequency range from tens of MHz to few GHz, while the SLVS interface was designed for data rates beyond 1 GHz.

The die area of complete ASIC, comprising 8 ADC channels, digital control and serializer with PLL, and SLVS drivers, is 2 mm x 2.2 mm, while the single ADC channel layout occupies 150 um x 600 um. The preliminary static measurements show that the ADC prototype works well with DNL and INL below 1 LSB. The ENOB obtained from dynamic measurements remains above 9 bits. Both static and dynamic parameters are uniform between channels and do not vary between single and multichannel operations. The ADC power consumption scales linearly with sampling frequency in large frequency range with the scaling factor of about 23 uW/channel/MHz. At nominal 40 MS/s sample rate the ADC consumes around 900 uW per channel. The Figure of Merit changes between 35-70˜fJ/conversion, placing the ADC within the State of the Art designs. Moreover, for the first time in particle detector readout systems, such excellent results were obtained for multichannel operation.

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